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Simulation & Experimental Implementation of Multi Level Inverter Topology with Reduced Components

Hemanth Kumar. T

Lecturer & Head of the Department, Department of EEE, Hanagal Sri Kumareshwara Polytechnic (H.S.K Polytechnic), (Formerly V. V. Sangha's Polytechnic), Ballari, Karnataka, India

ABSTRACT: In this paper I would like to present, an improved sensorless thirteen level inverter topology with reduced number of components. It is formed by cascading a three-level T-type neutral point inverter with a floating capacitor (FC) fed two-level converter unit. Additionally, two line-frequency switches are appended across the dc-link. A simple logic-form equations-based pulse width modulator is designed which is in-charge of maintaining the FC voltage at its reference value without any aid of voltage and current sensor. Thus, the complexity in control of the proposed topology is very minimal. The working principle of the proposed inverter and formulation of logic-form equations is deliberated in detail. Further, experimental results obtained from the developed prototype are presented to validate feasibility and operability of the proposed topology. Finally, a comprehensive comparison with some of the recently reported inverter topologies proving the merits of the proposed topology is included.

KEYWORDS: Flying Capacitor (FC), Solar Photovoltaic (PV), Neutral Point Clamped (NPC).

I. INTRODUCTION

The depletion of fossil fuels, rising environmental concerns and day-by-day increasing demand for electrical energy has elevated the need for generating energy from alternate sources. Wind and solar photovoltaic (PV) technology has gained a lot of attention among renewable energy sources as they are environment-friendly. This quick growth has created an arena in view of exploiting the wind and PV energy fully, wherein many expeditious technologies in the field of power electronic converter structures for enabling the integration of renewable energy based system for electric power generation have emerged.

Multilevel inverters (MLIs) have been extensively investigated during the recent past and are undoubtedly the emerging solution for a variety of power electronics applications owing to their propitious features like improved power quality, reduced device stress, high modularity, reduced filter requirement, etc.,

The traditional MLIs predominantly use dare cascaded H-bridge, neutral-point-clamped (NPC), modular multilevel inverter, flying capacitor inverters and their variants. However, recently the use of MLIs as power interface for low power applications like grid connected renewable energy sources has become more prevalent.

Following the commercial availability of power devices (MOSFETs and IGBTs) with a voltage rating up to 1.2 kV sufficing the lowpower applications, a rapid research on new MLI topologies with a pertinent focus on reducing the number of part count (switches, capacitors, diodes) is witnessed.

Use of switched dc sources for the generation of a multistep waveform is the preeminent idea of multilevel dc-ac power conversion [7]. In the recent past, attempts have been made to separate the level and polarity generation part to reduce the number of dc sources and power switches for a given number of voltage levels [8], [9]. On the other hand, many hybrid topologies combining the traditional and not so- traditional MLIs are found in the literature. An FC-based single dc source multicell converter capable of doubling the RMS output voltage is presented in [10]. In [11], cascade connection of a five-level (5L) double flying capacitor multi cell converter and a floating capacitor (FC) fed H-bridge resulting in a nine-level (13L) output voltage is proposed. It requires single dc source, ten switches and two capacitors for its operation. A single dc source switched-capacitor (SC) based MLI proposed in [12] comprises of two capacitors, nine switches, and two diodes. An use of MLI for transformerless grid-connected photovoltaic (PV) system is being demonstrated.

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II. LITERATURE SURVEY

R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter," IEEE Trans. on Industrial Electronics, vol. 55, no. 7, pp. 2694-2702, 2008.

The elimination of the output transformer from grid- connected photovoltaic (PV) systems not only reduces the cost, size, and weight of the conversion stage but also increases the system overall efficiency. However, if the transformer is removed, the galvanic isolation between the PV generator and the grid is lost. This may cause safety hazards in the event of ground faults. In addition, the circulation of leakage currents (common-mode currents) through the stray capacitance between the PV array and the ground would be enabled. Furthermore, when no transformer is used, the inverter could inject direct current (dc) to the grid, causing the saturation of the transformers along the distribution network. While safety requirements in transformerless systems can be met by means of external elements, leakage currents and the injection of dc into the grid must be guaranteed topologically or by the inverter's control system. This paper proposes a new high-efficiency topology for transformerless systems, which does not generate common-mode currents and topologically guarantees that no dc is injected into the grid. The proposed topology has been verified in a 5-kW prototype with satisfactory results.

S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel Inverter Topologies for Stand-Alone PV Systems," IEEE Trans. on Industrial Electronics, vol. 55, no. 7, pp. 2703-2712, 2008.

This paper shows that versatile stand-alone photovoltaic (PV) systems still demand on at least one battery inverter with improved characteristics of robustness and efficiency, which can be achieved using multilevel topologies. A compilation of the most common topologies of multilevel converters is presented, and it shows which ones are best suitable to implement inverters for stand-alone applications in the range of a few kilowatts. As an example, a prototype of 3 kVA was implemented, and peak efficiency of 96.0% was achieved.

W. Yu, J. S. Lai, H. Qian, and C. Hutchens, "High-Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic Nonisolated ACModule Applications," IEEE Trans. on Power Electronics, vol. 26, no. 4, pp. 1253-1260, 2011.

A novel, high-efficiency inverter using MOSFETs for all active switches is presented for photovoltaic, non-isolated, ac-module applications. The proposed H6-type configuration features high efficiency over a wide load range, low ground leakage current, no need for split capacitors, and low-output ac-current distortion. The detailed power stage operating principles, pulse width modulation scheme, associated multilevel bootstrap power supply, and integrated gate drivers for the proposed inverter are described. Experimental results of a 300 W hardware prototype show that not only are MOSFET body diode reverse-recovery and ground leakage current issues alleviated in the proposed inverter, but also that 98.3% maximum efficiency and 98.1% European Union efficiency of the DC - AC power train and the associated driver circuit are achieved.

R. A. Ahmed, S. Mekhilef, and W. P. Hew, "New multilevel inverter topology with minimum number of switches," in Proc. IEEE TENCON, pp. 1862-1867, 2010.

This paper presents two types of multilevel inverters, known as symmetrical and asymmetrical multilevel inverter. Both types are very effective and efficient for improving the quality of the inverter output voltage. Firstly, we describe briefly the structural parts of the inverter then switching strategy and operational principles of the proposed inverter are explained and operational topologies are given. The proposed topology reduces the number of switches, losses, installation area and converter cost. Finally, the simulation results are provided to validate the proposed theory.

M. R. Banaei and E. Salary, "New Multilevel Inverter with Reduction of Switches and Gate Driver," in Proc. IEEE IECC, pp. 784-789, 2010.

This paper presents a novel topology for symmetrical cascaded multilevel converter. The proposed circuit consists of series connected sub multilevel converters blocks and it can generate DC voltage levels similar to other topologies. The proposed topology results in reduction of switches number, losses, installation area and converter cost. This converter has been used in a Dynamic Voltage Restorer (DVR). Simulation results are being carried out.

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III. EXISTING SYSTEM

The existing method describes a combination of CHB with FC H Bridge presented in consists of one dc source and eight switches only. However, regulation of FC voltage at 1 = 3Vdc requires additional circuit, while mere experimental results are presented. A configuration which includes 5L double flying capacitor multi cell (DFCM) converters cascaded with FC H Bridge is recommended to overcome the increased diversity factor in a DFCM converter. A 13L cross- connected intermediate level unit integrated with ANPC is introduced. Most of these topologies are hybrid combinations of one or more converter families (NPC, FC, and CHB). Many such hybridizations resulting in 13L RPC inverter are reported in literature. Although for identical voltage levels, the topologies mentioned require a lesser number of components, the drawbacks associated are high-frequency switching of power devices, a lot of feedback sensors, increased voltage diversity factor and higher control complexity.

DRAWBACKS OF EXISTING METHOD:

1. High-frequency switching of power devices, a lot of feedback sensors, increased voltage diversity factor and higher control complexity.

IV. PROPOSED SYSTEM

Proposed method: The proposed method proposes a novel hybrid 13L inverter on the basis of reduced part count and using sensor less PWM technique. A detailed comparison is carried out and is presented to illustrate the distinctive characteristics and benefits of the proposed inverter. Firstly, a single-phase grid-connected system comprising the proposed topology is simulated, and then its loss evaluation is manifested through the simulation results. Further, a laboratory scale prototype of the proposed inverter is built. Simulation waveforms and experimental measurements are elucidated both for steady-state and transient operating conditions to validate the proposed hybrid inverter.

ADVANTAGE OF PROPOSED METHOD:

A novel hybrid 13L inverter on the basis of reduced part count and using PWM technique.

STATES	S1	S2	S3	S4	S5	OUTPUT VOLTAGE	FC VOLTAGE
L4+	1	0	1	1	0	Vdc	NO EFFECT
L31+	0	0	0	1	0	3Vdc / 4	DISCHARGING
L32+	1	0	1	0	0	3Vdc / 4	CHARGING
L2+	0	0	1	1	0	Vdc / 2	NO EFFECT
L11+	0	1	0	1	0	Vdc / 4	DISCHARGING
L12+	0	0	1	0	0	Vdc / 4	CHARGING
L0+	0	1	1	1	0	0	NO EFFECT
L0-	1	0	1	1	1	0	NO EFFECT
L11-	1	0	1	0	1	-Vdc / 4	DISCHARGING
L12-	0	0	0	1	1	-Vdc / 4	CHARGING
L2-	0	0	1	1	1	-Vdc / 2	NO EFFECT
L31-	0	0	1	0	1	-3Vdc / 4	DISCHARGING
L32-	0	1	0	1	1	-3Vdc / 4	CHARGING
L4-	0	1	1	1	1	-Vdc	NO EFFECT

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V. BLOCK DIAGRAM & PROPOSED SYSTEM

Block Diagram of Proposed Method: Circuit topology of the proposed inverter.

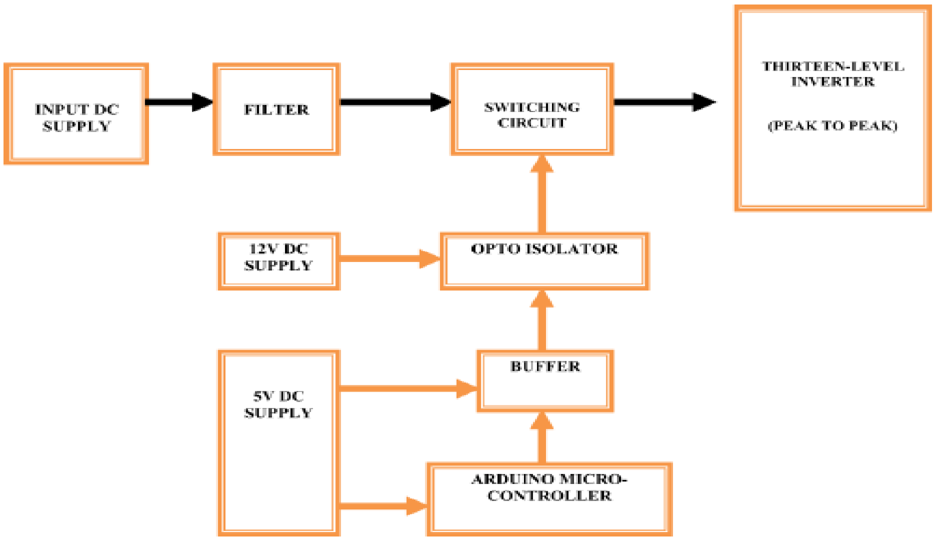

Fig 1: Block Diagram

SWITCHING CIRCUIT theory is the mathematical study of the properties of networks of idealized switches.

Such networks may be strictly combinational logic, in which their output state is only a function of the present state of their inputs; or may also contain sequential elements, where the present state depends on the present state and past states; in that sense, sequential circuits are said to include "memory" of past states. An important class of sequential circuits are state machines. Switching circuit theory is applicable to the design of telephone systems, computers, and similar systems.

In the paper, A Symbolic Analysis of Relay and Switching Circuits of 1938, Claude Shannon showed that the two-valued Boolean algebra can describe the operation of switching circuits. The principles of Boolean algebra are applied to switches, providing mathematical tools for analysis and synthesis of any switching system.

Ideal switches are considered as having only two exclusive states, for example, open or closed. In some analysis, the state of a switch can be considered to have no influence on the output of the system and is designated as a "don't care" state. In complex networks it is necessary to also account for the finite switching time of physical switches; where two or more different paths in a network may affect the output, these delays may result in a "logic hazard" or "race condition" where the output state changes due to the different propagation times through the network.

COUPLED INDUCTORS: A coupled inductor is actually a pair of inductors. A normal inductor is coupled only to itself -- that is, it has one input and one output, with voltage and current following the relationship.

In electric circuits coupled inductors are the next step after inductors in circuit analysis. Mutual inductance which is the voltage generated in second inductor by changing current is taught. Coupled circuits analyses is used in RF circuits.
But an inductor is a passive electrical device employed in electrical circuits for its property of inductance which is an effect that results from the magnetic field that forms around a current-carrying conductor.

VOLTAGE DOUBLER: A voltage doubler is an electronic circuit which charges capacitors from the input voltage and switches these charges in such a way that, in the ideal case, exactly twice the voltage is produced at the output as at its input.

The simplest of these circuits are a form of rectifier which take an AC voltage as input and outputs a doubled DC voltage. The switching elements are simple diodes and they are driven to switch state merely by the alternating voltage

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of the input. DC-to-DC voltage doublers cannot switch in this way and require a driving circuit to control the switching. They frequently also require a switching element that can be controlled directly, such as a transistor, rather than relying on the voltage across the switch as in the simple AC-to-DC case.

Voltage doublers are a variety of voltage multiplier circuit. Many, but not all, voltage doubler circuits can be viewed as a single stage of a higher order multiplier: cascading identical stages together achieves a greater voltage multiplication. In electronics, an opto-isolator, also called an optocoupler, photocoupler, or optical isolator, is a component that transfers electrical signals between two isolated circuits by using light. Opto-isolators prevent high voltages from affecting the system receiving the signal. Commercially available opto-isolators withstand input-to-output voltages up to 10 kV and voltage transients with speeds up to 10 kV/μs.

A common type of opto-isolator consists of an LED and a phototransistor in the same opaque package. Other types of source-sensor combinations include LED-photodiode, LED-LASCR, and lamp-photo resistor pairs. Usually opto-isolators transfer digital (on-off) signals, but some techniques allow them to be used with analog signals.

Arduino (ATMEGA 2560): ARDUINO microcontroller is used to produce switching pulses to multilevel inverter. It consists of 54 pins IC (of which 14 provide PWM output, 16 analog inputs and having a clock speed of 16 MHz. It is one of the most popular microcontroller. The microcontroller generates switching pulses, which are given to the driver circuit. The output of the driver circuit is 12 volts. An optocoupler is used for isolation in the driver circuit.

PROPOSED THIRTEEN-LEVEL INVERTER OPERATING PRINCIPLE AND CONTROL

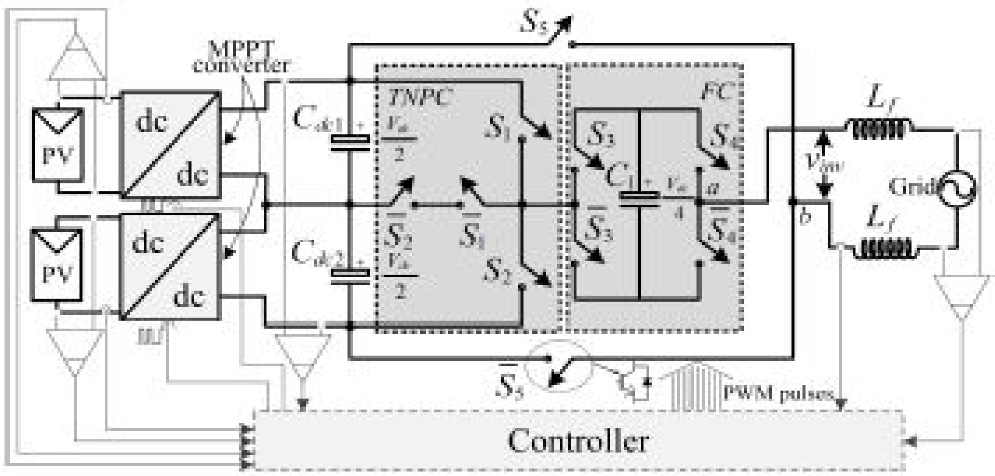

Fig 2: Proposed System

- **TNPC Inverter:** It serves as a fundamental multilevel voltage generation unit capable of producing three unique voltage levels namely Vdc = 2; 0; Vdc = 2. The switches S1, S2, _ S1 and _ S2 constitute the TNPC unit, which are required to block a voltage of Vdc for S1, S2 and Vdc = 2 for _ S1 and _ S2 respectively.

- **SC Unit:** It is basically a two-level (2L) voltage converter capable of generating levels 0 and Vdc = 4, comprising of the switches S3, _ S3 and a FC (Cf) , whose voltage (V_C) need to be regulated at one-fourth of the total dc-link voltage i.e., Vdc = 4 for the generation of output voltage with uniform steps.

- **Line frequency switches (LFSs):** Two switches (S4 and _ S4) operating at line frequency is connected across the dc-link. The principal function of this unit is to add Vdc to the 5L voltage generated by the series connected TNPC and SC unit. Consequently, a 13L voltage waveform is synthesized. In other words, the addition of LFSs doubles the number of voltage levels generated by the latter combination.

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Circuit Description in Fig. 1 shows the power circuit topology of the proposed 13L inverter. It comprises mainly three units; a 3L TNPC cascaded with 3L FC H-bridge unit and two low-frequency switches (LFS) across the dc-link. With Vdc being the total input voltage, the voltages across the dc-link capacitors and FC are equal to Vdc/2 and Vdc/4 respectively. The idea of cascading TNPC with FC yields in the following advantage of fewer number of power devices, power diodes, and capacitors, and more importantly it is modular in comparison with other inverters generating same number of levels.

VI. RESULTS AND DISCUSSION

In the Fig 3 & 4, it shows the Simulation Circuit Implementation using MAT LAB Software of 13L Inverter.

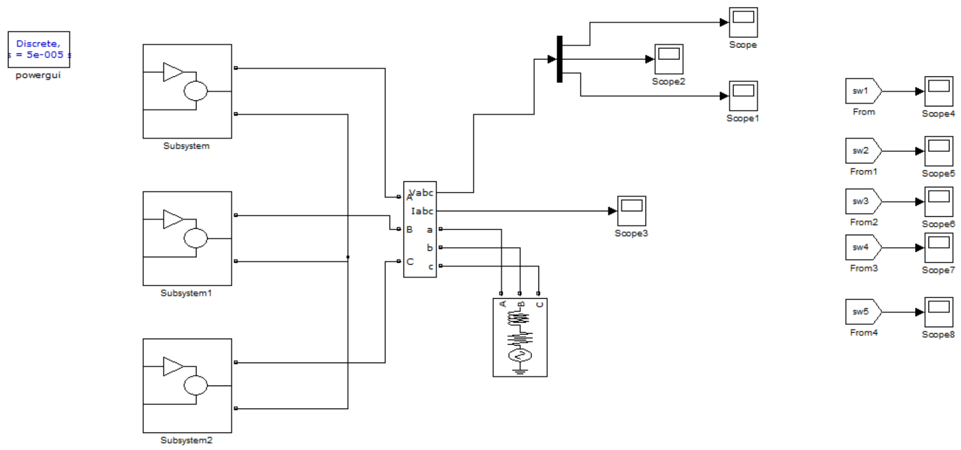

Fig 3: Simulation Circuit Diagram

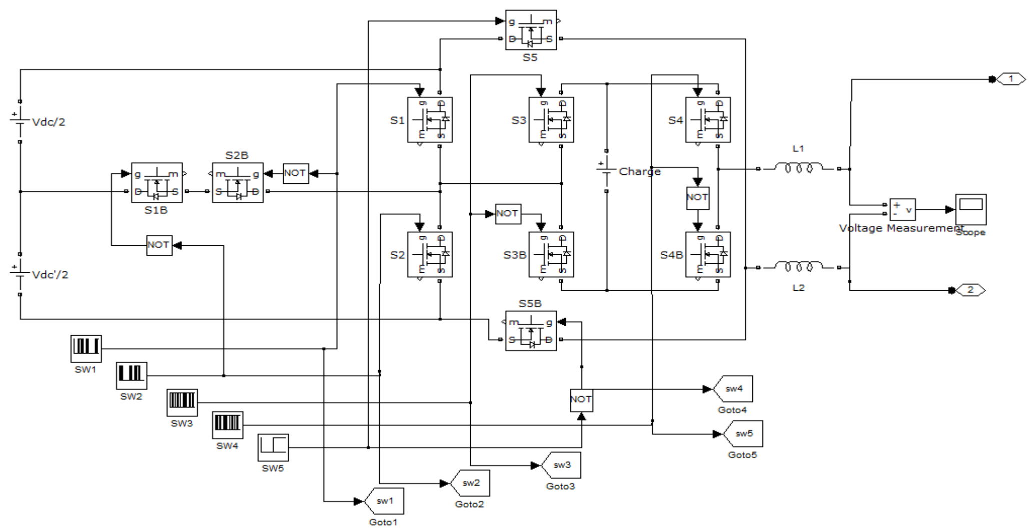

Fig 4: Simulation Circuit Diagram

In the Fig 5 & 6, the Simulation Circuit Output Waveforms are being represented.

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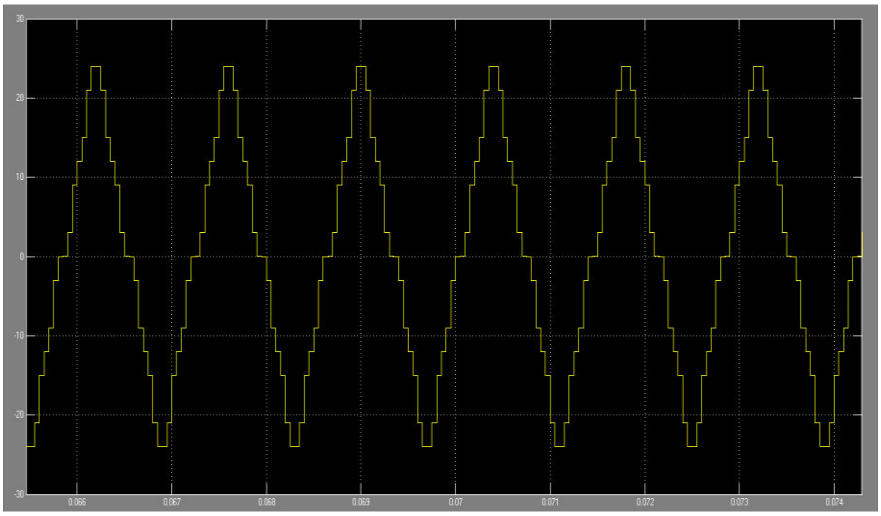

Fig 5: Simulation Circuit Output Waveforms

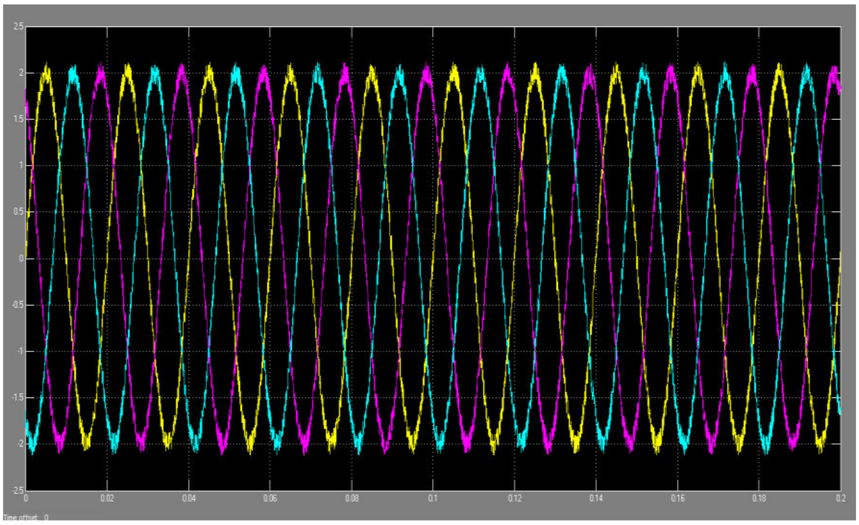

Fig 6: Simulation Circuit Output Waveforms

In Fig 7, the Hardware Set – Up along with its Output obtained is being represented.

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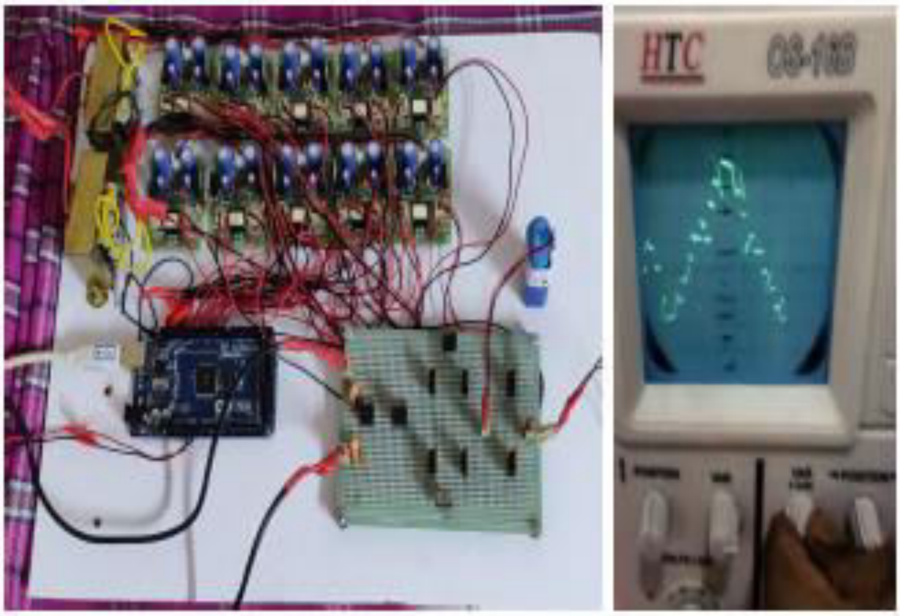

Fig 7: Hardware Set - Up along with Output Waveforms

VII. CONCLUSION

In this paper, the working concept of the proposed 13L SC-based MLI was discussed and verified experimentally. The topology is highly compact comprising of eight switches (while two of them operate at line frequency) and one FC. Also, the number of current conducting switches are less in comparison to other 13L topologies. Due to the inherent selfbalancing capability, the voltage across FC ideally remains constant at all operating conditions. Besides, the developed logic-form equations-based controller does not involve any cost function minimization or complex computations and thus simplifies its real-time implementation. The experimental results presented verifies the feasibility and theoretical concept of the proposed topology. A wide-ranging comparison regarding the number of switches required, FCs, total blocking voltage and price factors verifies the superior performance of the proposed inverter with recently acclaimed topologies. The capability to generate a multilevel output voltage and lower power electronics cost requirement enables the presented topology to be a challenging candidate for the conventional grid-connected inverters.

REFERENCES

[1] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, “Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter,” IEEE Trans. on Industrial Electronics, vol. 55, no. 7, pp. 2694-2702, 2008.

[2] S. Daher, J. Schmid, and F. L. M. Antunes, “Multilevel Inverter Topologies for Stand Alone PV Systems,” IEEE Trans. on Industrial Electronics, vol. 55, no. 7, pp. 2703-2712, 2008.

[3] M. R. Banaei and E. Salary, “New Multilevel Inverter with Reduction of Switches and Gate Driver,” in Proc. IEEE IECC, pp. 784-789, 2010.

[4] R. A. Ahmed, S. Mekhilef, and W. P. Hew, “New multilevel inverter topology with minimum number of switches,” in Proc. IEEE TENCON, pp. 1862-1867, 2010.

[5] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral point clamped inverters,” Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2219-2230, 2010.

[6] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, “High-Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic Nonisolated AC Module Applications,” IEEE Trans. on Power Electronics, vol. 26, no. 4, pp. 1253-1260, 2011.

[7] K. Gupta and S. Jain, "Topology for multilevel inverters to attain maximum number of levels from given DC sources," IET Power Electron., vol. 5, no. 4, pp. 435-446, 2012.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 8.514 | A Monthly Peer Reviewed & Refereed Journal |

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| DOI:10.15662/IJAREEIE.2024.1309008 |

[8] P. Roshankumar, P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A Five-Level Inverter Topology with Single- DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge," IEEE Trans. Power Electron., vol. 27, no. 8,
pp. 3505-3512, 2012.

[9] M. F. Kangarlu and E. Babaei, "A Generalized Cascaded Multilevel Inverter Using Series Connection of Sub multilevel Inverters," IEEE Trans. Power Electron., vol. 28, no.2, p. 625, 2013.

[10] Vahedi, Student, IEEE, Kamal Al-Haddad, Fellow, IEEE, Hadi Y. Kanaan, Senior Member, IEEE "A New Voltage Balancing Controller Applied On 7-Level PUC Inverter" 978-1-4799-4032-5/14/$31.00 2014 IEEE.

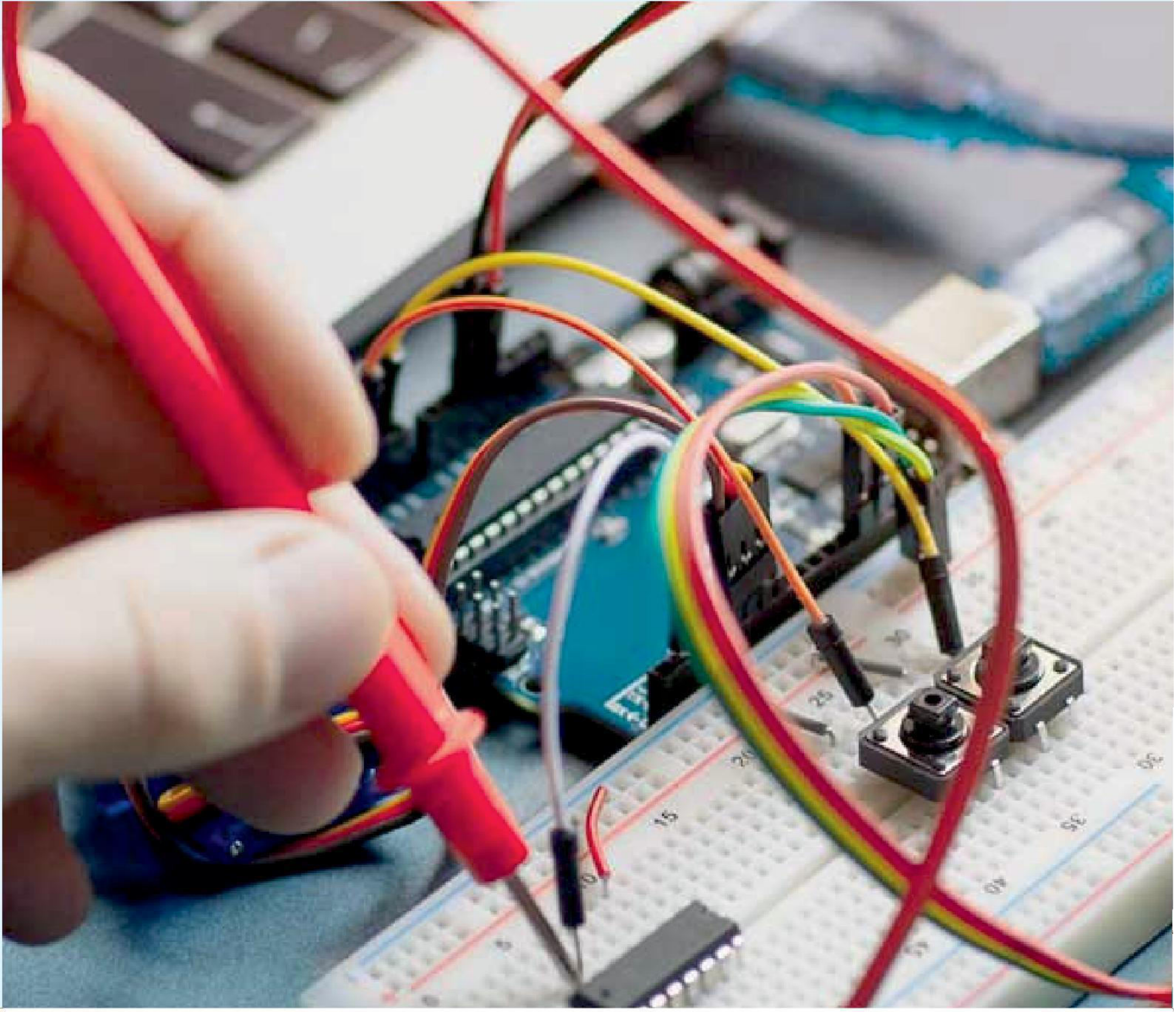
[11] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J.Rodriguez, M. A. P´erez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, 2010.

[12] C. Cecati, F. Ciancetta, and P. Siano, "A multilevel inverter for photovoltaic systems with fuzzy logic control," IEEE Trans. Ind. Electron., vol. 57, no. 12, pp. 4115–4125,
2010.

[13] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase shifted pulse width modulation," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1517–1526, 2010.

[14] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven level grid-connected inverter for photovoltaic system," IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2435–2443, 2011.

[15] G. Buticchi, D. Barater, E. Lorenzani, C. Concari, and G. Franceschini, "A nine level grid-connected converter topology for single-phase transformerless PV systems," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3951–3960, 2014.



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