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Power Optimized Dynamic Comparator for SAR Analog to Digital Converter

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ABSTRACT: Due to the high demand of ultra-low power in digital application, the needs of energy efficient Analog-to-digital converter (ADC) are really essential. The comparator being an important part of successive approximation register (SAR)-ADC needs to have optimum performance under low power condition. This paper presents the comparison on power consumption together with the output performance low power SAR-ADC dynamic comparators from two different designs. The two circuits are simulated and compared in terms of power consumption. The simulation is using Cadence Virtuoso and setup with 45nm CMOS technology, VDD at 1V and clock speed 2MHz. The analysis results obtained provides the lowest voltage input different (ΔVin) possible for double tail dynamic comparator with sleep transistor technique using 45nm CMOS technology.

I. INTRODUCTION

Presently multi day in world a large portion of the innovations are digitized yet it is in simple. For these fast applications, a noteworthy necessity is given to low power philosophies. The minimization in power utilization of these gadgets can be accomplished by focusing on littler element estimate forms, anyway as we move littler element measure forms the handling parameters and different attributes will be influence the execution of the gadget. Presently simple to advanced converters requires greatest slew rate, less power utilization, low counterbalance and rapid. The execution of the restricting squares in such ADCs is regularly gain speakers and comparators in which comparators configuration is generally vital. Consequently, the different plan issues identified with speed, gain, control scattering, counterbalance and exactness are transcendent significance.

Dynamic comparators are significant piece of the present ADCs extensively in light of the fact that these comparators have rapid and zero static power usage and giving full swing advanced dimension yield voltage term in shorter time interim yet eat up more power dispersal and give high information implied balance voltage. In these dynamic comparators, consecutive inverters give positive criticism framework which changes over a little voltage distinction. Nonetheless, an information implied counterbalance lock voltage, coming to fruition as a result of the gadget befuddles, for instance, edge voltage, current factor, yield stack capacitance and parasitic hub capacitance bungles, constrains the precision of such comparators, in light of this reason, the data suggested hook balance voltage is a champion among the most structure parameters of the locked comparators. In case the tremendous gadgets are used for the hooking stage, a less confound can be cultivated to the detriment both of the extended deferral (due to slower recuperation time) and the extended power dispersal.

II. LITERATURE SURVEY

The need for ultra-power, area efficient, and high speed Analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In the existing papers an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the trade-offs in dynamic comparator design.
In the previous references they have used 180nm and 90nm technology using HSPICE Tool and Cadence Spectre Tool. Two common structures of conventional dynamic comparator double tail comparators were analysed. Based on the theoretical analysis, a new dynamic comparator with low-voltage, low-power capability was proposed in order to improve the performance of the comparator. Proposed double tail comparator is designed and simulated using 90nm CMOS technology. From the simulated results it is observed that the delay of the proposed double tail comparator is 91.42ps which is comparatively less than the earlier comparators. Also the average power consumption of the proposed double tail comparator is calculated as 0.5604uW.
The modifications in this paper are:

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45nm technology in the Candence virtuoso software tool is used. Comparing the comparator average power consumption of the comparator without sleep transistor technique and the average power consumption of the comparator with sleep transistor technique. By using the sleep transistor technique the power will be reduced. Due to the better performance of the double tail architecture in low voltage applications, the proposed comparator in which we are using sleep transistor technique should be designed based on the double tail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross coupled manner. During reset phase (CLK=0, Mtail1 and Mtail2 are off, avoiding static power). M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cutoff. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision making phase (CLK=VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. At the beginning of this pahse, the control transistors are still off (since fn and fp are about VDD). Thus fn and fp start to drop with different rates according to the input voltages.

III. METHODOLOGY

Presently multi day in world a large portion of the innovations are digitized yet it is in simple. For these fast applications, a noteworthy necessity is given to low power philosophies. The minimization in power utilization of these gadgets can be accomplished by focusing on littler element estimate forms, anyway as we move littler element measure forms the handling parameters and different attributes will be influence the execution of the gadget. Presently simple to advanced converters requires greatest slew rate, less power utilization, low counterbalance and rapid. The execution of the restricting squares in such ADCs is regularly gain speakers and comparators in which comparators configuration is generally vital. Consequently, the different plan issues identified with speed, gain, control scattering, counterbalance and exactness are transcendent significance.

Dynamic comparators are significant piece of the present ADCs extensively in light of the fact that these comparators have rapid and zero static power usage and giving full swing advanced dimension yield voltage term in shorter time interim yet eat up more power dispersal and give high information implied balance voltage. In these dynamic comparators, consecutive inverters give positive criticism framework which changes over a little voltage distinction. Nonetheless, an information implied counterbalance lock voltage, coming to fruition as a result of the gadget befuddles, for instance, edge voltage, current factor, yield stack capacitance and parasitic hub capacitance bungles, constrains the precision of such comparators, in light of this reason, the data suggested hook balance voltage is a champion among the most structure parameters of the locked comparators. In case the tremendous gadgets are used for the hooking stage, a less confound can be cultivated to the detriment both of the extended deferral (due to slower recuperation time) and the extended power dispersal.

A comparator consists of a high gain differential amplifier whose output is compatible with the logic gates used in the digital circuit. The gain is high enough that a very small difference between the input voltages will saturate the output, the output voltage will be in either the low logic voltage band or the high logic voltage band of the gate input. Analogue op amps have been used as comparators, however a dedicated comparator chip will generally be faster than a general-purpose operational amplifier used as a comparator, and may also contain additional features such as an accurate, internal reference voltage, adjustable hysteresis, and a clock gated input.

A dedicated voltage comparator chip such as LM339 is designed to interface with a digital logic interface (to a TTL or a CMOS). The output is a binary state often used to interface real world signals to digital circuitry (see analog-to-digital converter). If there is a fixed voltage source from, for example, a DC adjustable device in the signal path, a comparator is just the equivalent of a cascade of amplifiers. When the voltages are nearly equal, the output voltage will not fall into one of the logic levels, thus analog signals will enter the digital domain with unpredictable results. To make this range as small as possible, the amplifier cascade is high gain. The circuit consists of mainly bipolar transistors. For very high frequencies, the input impedance of the stages is low. This reduces the saturation of the slow, large p–n junction bipolar transistors that would otherwise lead to long recovery times. Fast small Schottky diodes, like those found in binary logic designs, improve the performance significantly though the performance still lags that of circuits with amplifiers using analog signals. Slew rate has no meaning for these devices. For applications in flash ADCs the distributed signal across eight ports matches the voltage and current gain after each amplifier, and resistors then behave as level-shifters.
The LM339 accomplishes this with an open collector output. When the inverting input is at a higher voltage than the non inverting input, the output of the comparator connects to the negative power supply. When the non inverting input is higher than the inverting input, the output is 'floating' (has a very high impedance to ground). The gain of op amp as comparator is given by this equation V(out)=V(in)

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A. *45nm Technology*

The relentless drive in the semiconductor industry for smaller, faster, cheaper integrated circuits has brought the industry to the 45nm technology node. Penryn (codename), Intel's next generation family of processors implemented in a 45nm High-k metal gate silicon process technology and designed to meet a wide range of power envelopes and market segments. In transistor design with the use of high-k and metal gate for the insulating walls and switching gates of its 45nm transistors. The 193nm immersion lithography has the wavelength of 193nm, but the medium for the light conduction is changed from air to water. Then Intel include new micro architecture.

B. *Successive Approximation Register*

A **Successive-Approximation ADC** is a type of Analog-to-digital converter that converts a continuous Analog waveform into a discrete digital representation using a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.

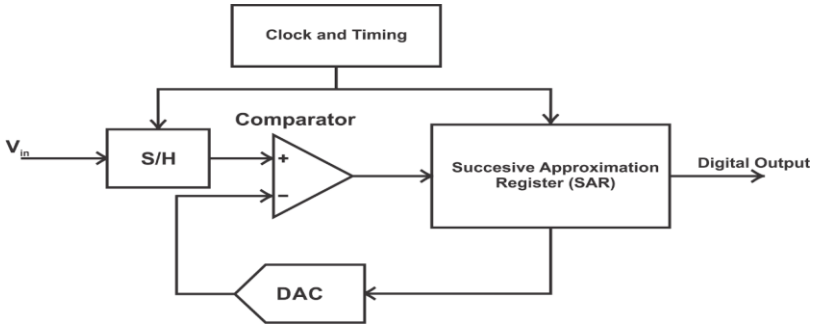

Fig1. Successive Approximation ADC block diagram

C. **Algorithm:**

The Successive-Approximation Analog-to-digital converter circuit typically consists of four chief subcircuits:

1. A sample-and-hold circuit to acquire the input voltage V_{in}.
2. An Analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive-approximation register (SAR).
3. A successive-approximation register subcircuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that, for comparison with V_{ref}, supplies the comparator with an Analog voltage equal to the digital code output of the SAR_{in}.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the Analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this Analog voltage exceeds V_{in}, then the comparator causes the SAR to reset this bit; otherwise, the bit is left as 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion (EOC).
Mathematically, let $V_{in} = xV_{ref}$, so x in $[-1, 1]$ is the normalized input voltage. The objective is to approximately digitize x to an accuracy of $1/2^n$. The algorithm proceeds as follows:

1. Initial approximation $x_0 = 0$.
2. ith approximation $x_i = x_{i-1} - s(x_{i-1} - x)/2^i$, where, $s(x)$ is the signum function ($\text{sgn}(x) = +1$ for $x \geq 0$, -1 for $x < 0$). It follows using mathematical induction that $|x_n - x| \leq 1/2^n$.

As shown in the above algorithm, a SAR ADC requires:

1. An input voltage source V_{in}.
2. A reference voltage source V_{ref} to normalize the input.
3. A DAC to convert the ith approximation x_i to a voltage.
4. A comparator to perform the function $s(x_i - x)$ by comparing the DAC's voltage with the input voltage.
5. A register to store the output of the comparator and apply $x_{i-1} - s(x_{i-1} - x)/2^i$.

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IV. COMPARATOR

COMPARATOR is one of the fundamental building blocks in most Analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes.

Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs.

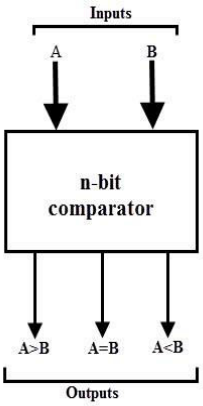

Fig2. Block Diagram of n-bit comparator

Many techniques, such as supply boosting methods, techniques employing body-driven transistors, current-mode design and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock, removes the threshold voltage requirement such that body driven MOSFET operates as a depletion-type device. Based on this approach a 1-bit quantizer for sub-1V modulators is proposed. Despite the advantages, the body driven transistor suffers from smaller transconductance (equal to g_{mb} of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration.

Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity, additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The proposed comparator works down to a supply voltage of 1V with a maximum clock frequency of 2MHz and consumes less power. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed is based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range.

V. LOW POWER TECHNIQUES

Advancement feature size and limit voltage have been scaling for a significant long time for achieving high thickness and unrivalled. In light of this development design, transistor spillage compel has extended exponentially [4]. As the part measure gets the opportunity to be smaller, shorter occupy lengths bring extended sub-edge spillage current through a transistor amid it is off. We can achieve extended sub-limit spillage current in light of the fact that transistors can't be murdered completely at the low edge voltage. Subsequently, static power usage, i.e., spill control dispersal, has transform into a basic piece of total power use for silicon advancements. There are VLSI techniques to less spillage

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control. Each methodology give a successful way to deal with decrease spillage control; however obstacles of each framework compel usage of each technique. We proposed other technique, to low-spillage control VLSI makers.

i. Sleep approach:
The most outstanding ordinary technique is the rest philosophy. These rest transistors slaughter the circuit by evacuating the power rails. By expelling the power source, this procedure can decrease spillage control feasibly. Regardless, the methodology brings demolition of express a coasting out voltage into rest mode.

ii. Sleepy keeper
Drowsy manager utilizes spillage analysis technique. As shown in the Fig. 3 in the midst of rest mode, rest transistors are murdered and one of the transistors in parallel to the rest transistors keeps the relationship with the appropriate rail of power.

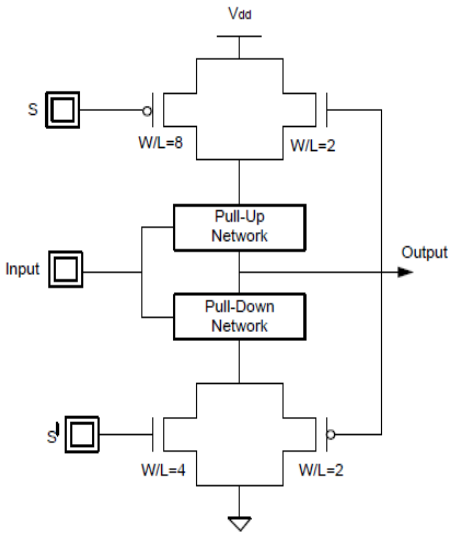

Fig 3. Sleepy Keeper

iii. Dual Sleep
Double rest system uses the advantage of using the two extra draw up and two extra draw down transistors in rest mode either in OFF state or in ON state. As shown in the Fig. 4 the twofold rest bit can be made fundamental to all reason equipment, less number of transistors is required to apply a specific method of reasoning circuit.

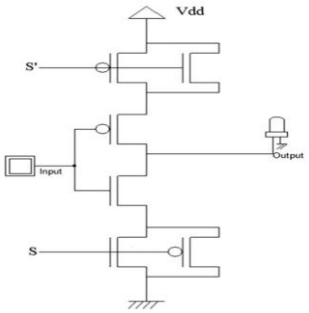

Fig 4: Dual Sleep

iv. Controlled double-tail comparator:
In the above Fig. 4.3.4 it is shown that in the midst of reset organize (CLK = 0, Ntail1 and Ntail2 are off, keeping up a key separation from static power. Widely appealing organize transistors, NR1 and NR2, reset both bolt respects ground. In the midst of fundamental initiative stage (CLK = VDD, Ntail1, andNtail2 are on), transistors P1 and P2 murder. Along these lines when passing, the qualification some place in the scope of f1 and f2 (ΔVf1/f2) increases in an

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exponential way, inciting the decline of bolt recuperation time. The transient amusement results are showed up as pursues. The deferrals of proposed twofold tail comparator included by two parameters, those are delay due to t0 and delay due to tlatch all of these parts will be inspected in detail. Fig.3 Sleepy keeper 726 L. Anantoju et al.

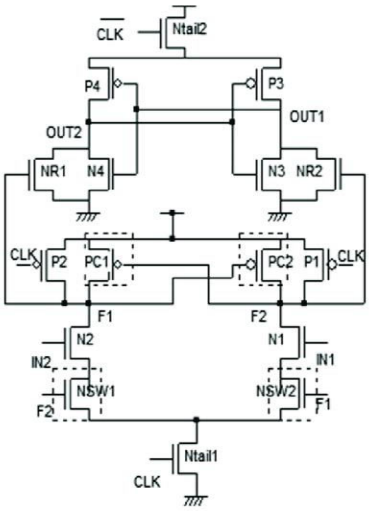

Fig 5. Schematic Diagram of Controlled Dual Tail Comparator

VI. PROPOSED APPROACH

i. Proposed sleep controlled Double-Tail comparator

As shown in the Fig. 6 the task of the proposed rest controlled double tail comparator, amid reset stage. When CLK = in3 = 0, Ntail1 and Ntail2 are off, P1 and P2 transistors pulls both f1 and f2 hubs to VDD, consequently transistors Pc1 and Pc2 are cut off. Middle stage arrange transistors, NR1 and NR2, reset both lock yields to ground. Amid basic leadership stage (CLK = in3 = VDD, Ntail1, andNtail2 are ON). The rest transistor doesn't permit VDD to lock circuit. The measure of spillage control lessens unimportantly little contrasted with controlled double tail comparator.

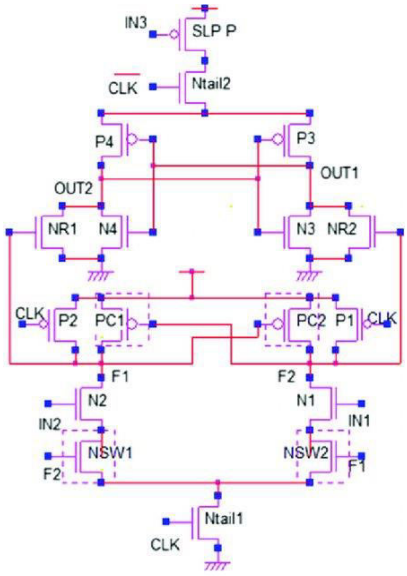

Fig 6. Proposed sleep controlled dual tail comparator schematic diagram.

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VII. RESULTS

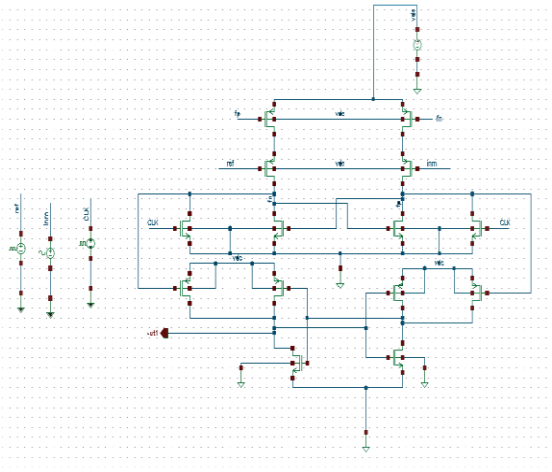

Fig 7. Dynamic double tail comparator without sleep transistor technique

The dynamic double tail comparator without sleep transistor circuit was simulated using Cadence Virtuoso tool with 45nm CMOS technology and shown in fig 7. The supply voltage used in simulation is 1V. The waveforms of this comparator are shown below:

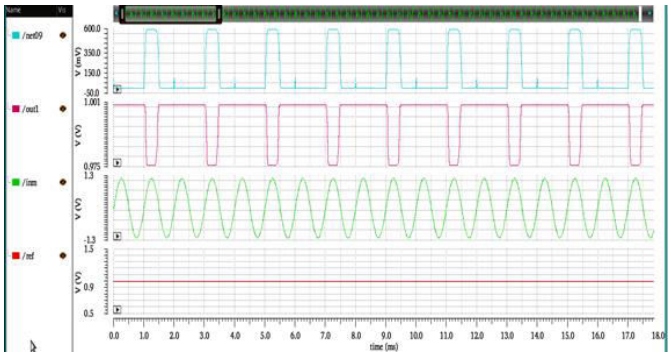

Fig 8. waveforms of comparator without sleep transistor technique.

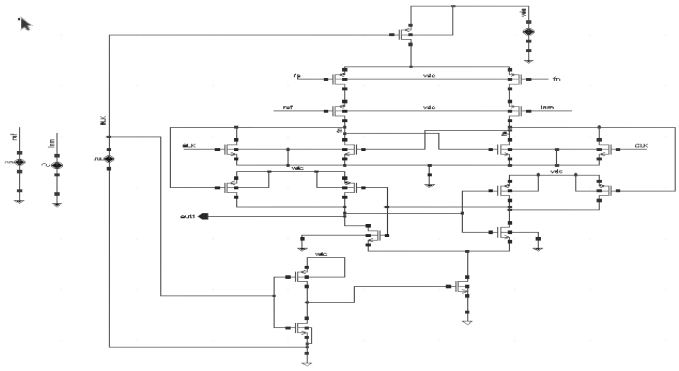

Fig 9. proposed dynamic double tail comparator with sleep transistor technique

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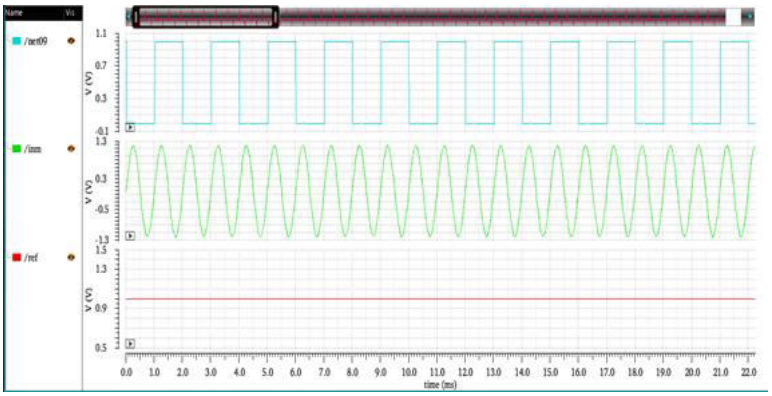

Fig 10. Waveforms of dynamic comparator with sleep transistor technique

VIII. COMPARISON TABLE

Comparator type	Power Consumption
Comparator without sleep transistor technique	**40.56uW**
Comparator with sleep transistor technique	**36.56nW**

IX. CONCLUSION

Double tail comparator with sleep transistor technique is designed and simulated using 45nm CMOS Technology. From the simulated results it is observed that the power of the dynamic double tail comparator with sleep transistor technique is reduced which is comparatively less than the comparator without sleep transistor technique. The average power consumption of the proposed dynamic double tail comparator with sleep transistor technique is calculated as 36.56nW. The average power consumption of the dynamic double tail comparator without sleep transistor technique is calculated as 40.56uW. Hence the power consumption is reduced as compared with the dynamic comparator without sleep transistor technique.

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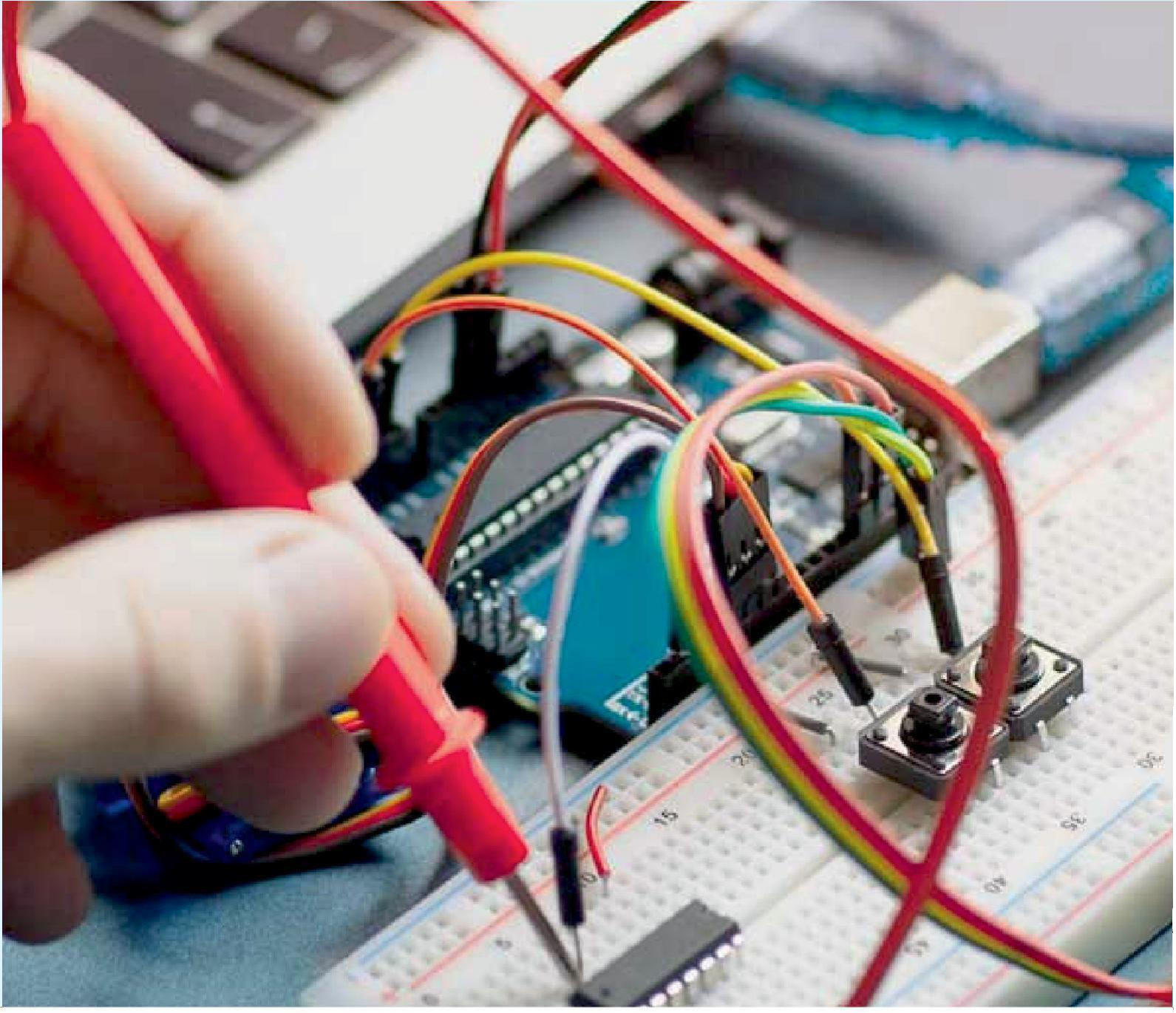

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