ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 9, Issue 3, March 2020

Quantum Cellular Automata

M.Divya[1], A.Rajiv[2], S.Vinothkumar[3]

Assistant Professor, Department of ECE, Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Chennai, India[1]

Assistant Professor, Department of ECE, Sriram Engineering College, Chennai, India[2]

Assistant Professor, Department of ECE, Sriram Engineering College, Chennai, India[3]

ABSTRACT: In the last few decades, the exponential scaling in feature size and increase in processing power have been successfully achieved by conventional lithography-basedVLSI technology. Nanotechnology provides new possibilities for computing due to the unique properties that arise at such reduced feature sizes. Among these new devices, Quantum-dot Cellular Automata (QCA)relies on new physical phenomena(such as Coulombic interactions), and innovative techniques that radically depart from a CMOS-based model. QCA not only gives a solution at nano-scale, built also offers a new method of computation and information transformation. QCA uses two basic logic gates, namely the INVand Majority Voter (MV). QCA is very promising because with this technology, computational paradigms which radically depart from traditional CMOS, can be implemented. Besides the extra-high density feature, QCA can provide ultralow power dissipation and true power gain which are very promising due to the high density of this nano device. Recent development in QCA manufacturing involves molecular implementation. It is expected that molecular QCA will be manufacturing using DNA self-assembly and/or large scale cell deposition on insulated substrates

I. INTRODUCTION

Conventional lithography-based VLSI technology (mostly utilizing CMOS) hasbeen extremely successful in the last few decades, reducing feature size below 100nm. As CMOS is fast approaching its fundamental physical limits (ultra thin gateoxides, short channel effects, etc.), new technologies at extremely small feature sizes (such as at nano scale) have been investigated to assess their viability for manufacturing future electronic/computing systems. New devices, such as carbonnanotubes, Si nanowires, single electron transistors, resonant tunneling diodes,single molecule devices, and spin transistors have been proposed. It is projectedthat ultra-high density integration and ultra highspeed operation can be achieved using these new devices.

Nanotechnology is a broad term that includes various areas of research suchas electronics, chemistry, biology, physics, material science, and medicine. Here wefocus on aspects of nanotechnology related to electronics. The National ScienceFoundation defines nanotechnology as having a feature size in the range of 1 to100 nm to produce structures, devices, and systems with novel properties due tothe reduced dimension. Devices that operate at nano scale, such as Field EffectTransistors (FETs), diodes, molecular and mechanical switches, have been recentlybuilt; moreover, non-volatile devices that hold their states in a few molecules, havebeen experimentally demonstrated. Different techniques have been shownto be effective in the assembly of nanometer wide wires into large arrays. At this reduced size, systems require completely new approaches to manufacturing and fabrication with immediate implications and significant impact on circuit designand architectures. Currently, semiconductor technology uses a “top-down” approachthat lithographically imposes a pattern. Unnecessary bulk material is then etchedaway to generate the desired structure. An alternative process to avoid the sophisticated and expensive nano-scale lithography is to use a so-called self-assembly, inwhich the nanostructures can be spontaneously built, i.e., self-assembled from the“bottom” on a molecule to molecule basis.

Carbon Nanotubes (CNTs) can be visualized as sheets of graphite rolled into seamless cylinders of nanometer diameter and micron scale length. As molecular-based devices, CNTs are extremely strong, flexible andtransfer heat very

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 9, Issue 3, March 2020

efficiently. Depending on their chirality (i.e., the latticestructure), CNTs can be metallic orsemiconducting. The tubes can be made intoIt has been shown that CNTs can be used as molecular wires and scanningprobe microscopy and lithography, diodes, field-effect transistors(FETs), SETs, programmable switches, memory or energy storage for batteries and fuel cells. However currently there is no known synthesis procedure to produce a pure batch of just one type (metallic or semiconducting) of CNTs. This makes specific device fabrication a likely random process and it poses severe limitations on integrating large systems.

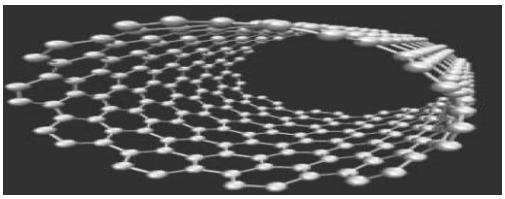

Figure 1A Single Walled Carbon Nanotube

An enhancement-mode p-type FET built with a single CNT has been demonstrated. This gate consists of an Al wire (as gate) over a negativeAl2O3 layerof only a few nanometers in thickness, that lies beneath a single CNT (as conducing channel). This CNT FET has been used to build various logic circuits such as aninverter, NOR gate and SRAM cell. However, the process by which semiconducting nanotubes are placed on specific locations on the wafer, still remains very difficult to solve. Without special processing, CNT FETs exhibit p-type characteristics. It has been shown that n-type CNT FETs can be manufactured by doping, or annealing p-type CNT FETs in vacuum. An inverter made of both ptypeand n-type CNT FETs has been demonstrated, and shown in Figure 2.Metallic CNTs have been shown to be ballistic. In ballistic transport, charge carriers

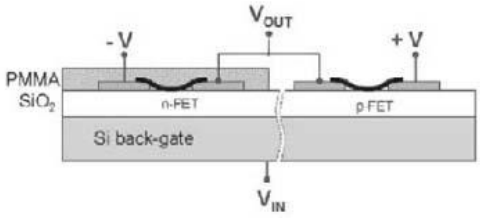

Figure 2CNT Inverter

II. BASICS OF QCA

A. QCA Cell

QCA cell is the fundamental unit of QCA technology. Each cell has four quantum dots. Two electrons remain in a cell. Due to the columbic forces these electrons always try to reside at the diagonal places of the cell in quantum dots [5]. This leads to two polarisation state, logic “0” and logic “1” displayed in Figure. 3. In QCA technology, information is propagated by cell polarization states, as state of one cell can be strongly influenced by neighbouring cell.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 9, Issue 3, March 2020

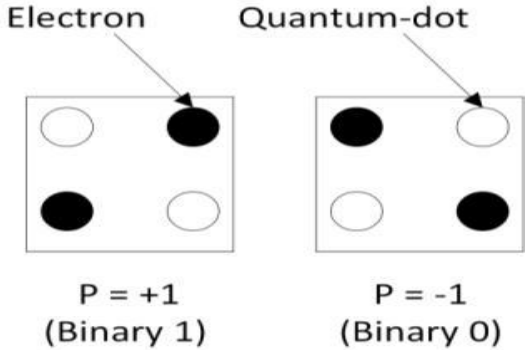

Figure 3. Possible two cell polarization

B. QCA wire

When the QCA cells are placed in the sequential manner, it forms a QCA wire. Binary signal can be transmitted from input end to output end by QCA wire. Orientation of QCA cell in wire is an important criterion for classification of QCA wire. A 90° aligned QCA wire is one where polarization of input cell is once fired will other cells in wire as demonstrated in Figure. 4, whereas 45O aligned QCA wire also known as anti-align QCA wire shows negation property as displayed in Figure. 5. Thus the output of wire is the negation of input as cells in a wire are 45° rotated.

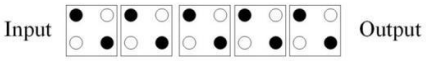

Figure. 4. 90° QCA wire

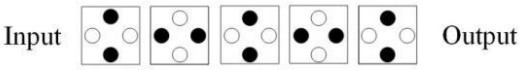

Figure. 5. 45° QCA wire

C. QCA Crossover

There are two types of wire crossing of QCA technology. One is coplanar wire crossing and other is multilevel wire crossing. In coplanar wire crossing whole design is onthe same plane or a single layer which is known as main layer cell. The crossing is done via both 90° and 45° QCA wire as displayed in the Fig. 6. In multilayer wire crossing three layers are used whenever crossing is required, which is known as main, middle and upper layer as displayed in Figure. 7

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 9, Issue 3, March 2020

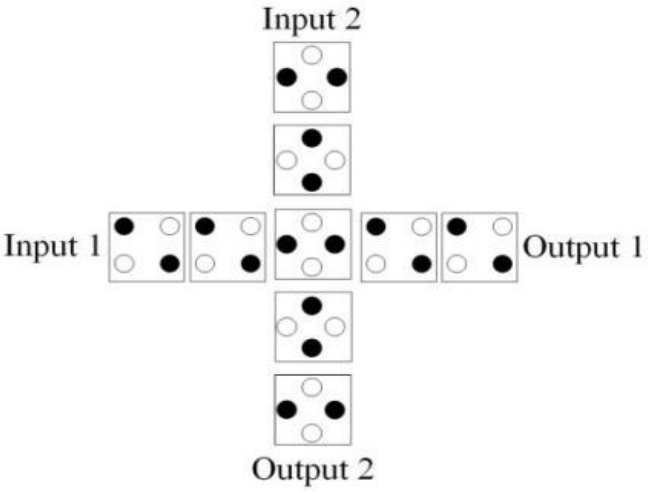

Figure. 6. Coplanar wire crossing

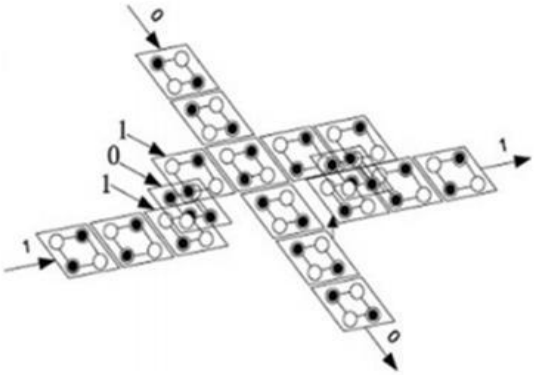

Figure. 7. Multilayer wire crossing

D. QCA basic logic gates

By the use of inverter and 3-input majority gate any logical expression can be designed in QCA using QCA Designer tool. These two are the basic gates to designing complicated circuits. In Figure 9, the output is inverted due to the anti-aligning behaviour of the cell. 3-input majority gate is created by arranging the 5 cells in a proper manner, displayed in Fig. 10. The logic function of 3-input majority gate is

M (A, B, C) = AB+BC+CA where 3-input majority gate act as AND gate and OR gate, when one input out of three input is logic "0" and logic "1" respectively.

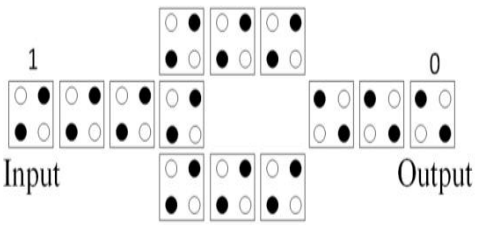

Figure. 8. QCA inverter

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 9, Issue 3, March 2020

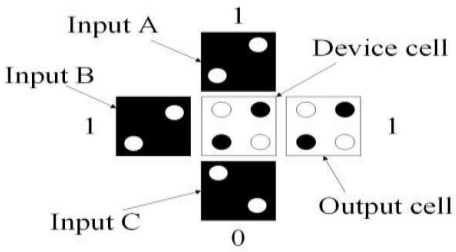

Figure 9. 3-input majority gate

E. QCA Clocking

QCA clock is the most prominent factor in QCA based designed circuits. QCA Clock not only delivers power to the circuit but also control the direction of data flow. In QCA clock cycle is consist of four phases. The four phases are switch, hold, and release and relax as depicted in Figure 10. Normally, a cell is in unpolarised state. Cell get polarized during the switch phase and act as a latch during the hold phase and unpolarised during relax and release phases.

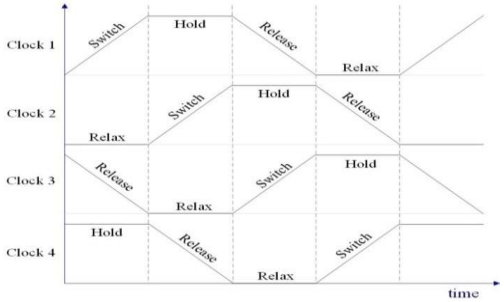

Figure. 10. Four clock zones

III. CHALLENGES

The small size of QCA-based systems combined with their manufacturing methods(such as self-assembly) are substantially different from CMOS and make them moresusceptible to defects and faults. In addition, defect in QCA manufacturing may well manifest themselves differently at logic level than CMOS. Defect characterizationis therefore vital to design and test of QCA systems.

One of the fundamental issues in the testing community is the radical shiftin computation and fabrication technology and its effect on the test flow. Do testgeneration and design-for-test become even intractable? Since the manufacturing process for nano devices is ill-defined, it is extremely difficult to address manufacturing
Testing problems. However, it would be inappropriate to ignore testing of these devices until themanufacturing state. QCA has the capability to provide defect tolerant operation and architectures that avoids massive logic redundancy or post fabrication configuration. For QCA, placing individual cells on specific location on the substrate is difficult, and various types of cell misplacement defects may occur (such as cell misalignment, missing cell, or additional cell). These defects can have a substantial effect on the functionality of the device and hence the circuit. So proper testing of these devices for manufacturing defects plays a major role for qualityof QCA-based circuits. Since the basic logic elements of a QCA-based design are different from conventional CMOS design, they need different testing schemes.
Moreover there are other manufacturing defects (such as faults in the clockingcircuitry and the I/O mechanism) that may not occur during cell synthesis phase (inwhich the individual cells or molecules are manufactured) or deposition phase (inwhich the cells are placed in a specific location on the surface). Some of these faultscould separately be tested prior to QCA cell deposition, while others must be studied for modeling and characterization. Because QCA system employs radically different computation paradigms,new design methodologies are needed to efficiently design large scale QCA systems.In QCA, the basic logic gate is the 3-input Majority Voter (MV), instead ofthe NAND, NOR gates in CMOS. Existing logic synthesis tool may not make use ofMV efficiently. The quality of logic synthesis results when

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 9, Issue 3, March 2020

using existing tools needto be investigated. Additionally, there are no CAD tool available to directly translateQCA netlist into QCA layout. The lack of CAD support for QCA makes designinglarge logic systems extremely difficult, if possible at all. Design automation tooltailored to the unique features of QCA need to be developed.

IV. CONCLUSION

Complementary metal-oxide semiconductor (CMOS) technology has been the industry standard for implementing Very Large Scale Integrated (VLSI) devices for the last four decades, mainly due to the consequences of miniaturization of such devices (i.e. increasing switching speeds, increasing complexity and decreasing power consumption). Quantum Cellular Automata (QCA) is only one of the many alternative technologies proposed as a replacement solution to the fundamental limits CMOS technology will impose in the years to come.

Although QCA solves most of the limitations of CMOS technology, it also brings its own. Research suggests that intrinsic switching time of a QCA cell is at best in the order of terahertz. However, the actual speed may be much lower, in the order of megahertz for solid state QCA and gigahertz for molecular QCA, due to the proper quasi-adiabatic clock switching frequency setting.

REFERENCES

[1] "International Technology Roadmap for Semiconductors," Jointly Sponsored by European SemiconductorIndustry Assc.,Japan Electronics and Information Technology Industry Assc., Korea SemiconductorIndustry Assc., Taiwan Semiconductor Industry Assc., and Semiconductor Industry Assc.,2004.
[2] Lent, C. S. and B. Isaksen, "Clocked Molecular Quantum-Dot Cellular Automata," IEEE Transactionson Electron Devices,Vol. 50, No. 9, 2003, pp. 1890-1895.
[3] Lent, C. S., P. D. Tougaw and W. Porod, "Quantum Cellular Automata: The Physics of Computingwith Arrays of Quantum Dot Molecules," PhysComp '94: Proceedings of the Workshop on Physicsand Computing, IEEE Computer Society Press, 1994, pp. 5-13.
[4] Smith, C. G., "Computation Without Current," Science,Vol. 284, No. 5412, 1999, pp. 274.
[5] Amlani, I., et al., "Demonstration of a Six-Dot Quantum Cellular Automata System," AppliedPhysics Letters, Vol. 72, No.17, 1998, pp. 2179-2181.
[6] Orlov, A.O., et al., "Realization of a Functional Cell for Quantum-Dot Cellular Automata," Science,Vol. 277, No. 5328, 1997, pp. 928-930.
[7] Frost, S. E., et al., "Memory in Motion: A Study of Storage Structures in QCA," 1st Workshop onNon-Silicon Computation, 2002.
[8] Niemier, M. T., A. F. Rodrigues and P.M. Kogge, "A Potentially Implementable FPGA for QuantumDot Cellular Automata," 1st Workshop on Non-Silicon Computation, Cambridge, MA, 2002.
[9] Walus, K., et al., "RAM Design Using Quantum-Dot Cellular Automata," NanoTechnology Conference,Vol. 2, 2003, pp. 160-163.
[10] Niemier, M. T. and P. M. Kogge, "Problems in Designing with QCAs: Layout=Timing," InternationalJournal of Circuit Theory and Applications,Vol. 29, No. 1, 2001, pp. 49-62.
[11] Kummamuru, R. K., et al., "Power Gain in a Quantum-dot Cellular Automata Latch," AppliedPhysics Letters,Vol. 81, No.7, 2002, pp. 1332-1335.
[12] Timler, J. and C. S. Lent, "Power Gain and dissipation in Quantum-dot Cellular Automata," Journalof Applied Physics,Vol. 91, No. 2, 2002, pp. 823-831.
[13] Bernstein, G. H., et al., "Electron Beam Lithography and Liftoff of Molecules and DNA Rafts,"IEEE conference on Nanotechnology, 2004, pp. 201-203.
[14] Armstrong, C. D., and W. M. Humphreys, "The Development of Design Tools for Fault TolerantQuantum Dot Cellular Automata Based Logic," 2nd International Workshop on Quantum Dots forQuantum Computing and Classical Size Effect Circuits, 2003.
[15] Fijany, A. and B.N. Toomarian, "New design for Quantum Dots Cellular Automata to Obtain FaultTolerant Logic Gates," Journal of Nanoparticle Research, Vol. 3, No. 1, 2001, pp. 27-37.
[16] Governale, M.,et al., "Modeling and Manufacturing Assessment of Bistable Quantum-Dot CellularCells," J. Appl. Phys., vol 85, No. 5, 1999, pp. 2962-2971.