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Nonzeroing Bit Truncation using Energy Scalable with High Speed Full Adder Design

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ABSTRACT: Approximate Addition is a technique to trade off energy consumption and output quality in error-tolerant applications. In prior art, bit truncation has been explored as a lever to dynamically trade off energy and quality. In this brief, an innovative bit truncation strategy is proposed to achieve more graceful quality degradation compared to state of- the-art truncation schemes. This translates into energy reduction at a given quality target. When applied to a ripple-carry adder, the proposed bit truncation approach improves quality by up to 8.5 dB in terms of peak signal-to-noise ratio, compared to traditional bit truncation. As a case study, the proposed approach was applied to a discrete cosine transform engine. In comparison with prior art, the proposed approach reduces energy by 20%, at insignificant delay and silicon area overhead.

KEYWORDS: Energy quality scaling, Approximate computing, error-tolerant systems, low-power design, VLSI design**.**

I. INTRODUCTION

Approximate adders has difficulty detecting and correcting errors since they are designed for error-acceptable applications with a target accuracy. However, accurate computations are still required at certain times, according to the application. VLSI can provide accurate results, but has large delay and area overhead for the error detection and correction. Power consumption of the Ripple carry adder can be used to detect the given bit into non zeroing values. Dynamic power consumption with voltage scaling at a fixed frequency is proportional to capacitance

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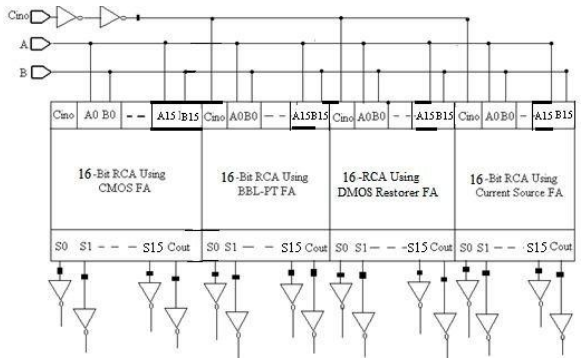

Fig.1.1 Ripple carry adder**.**

This RCA (Ripple Carry Adder) is mainly used for the detection of non zeroing values in the given bits. Some of the basic uses has been given in the following.

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- Ripple carry adder is a combinational logic circuit mainly used for the addition of n-bit binary values and given the output with high accuracy.
- A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder.
- This ripple carry adder is also as called carry out adder because each carry bit gets rippled into the next stage.
- This adder reduces circuit complexibility. It can be used to construct a ripple carry counter to add an n-bit number.

The Energy quality scalable is mainly used for the high accuracy output bit values. This may basically reduce the consumption of the power and also it may take less time for deliver the output bit. This may used the approximate adders process and the application of this purpose is mainly deliver the data with accuracy in Least Significant Bit (LSB). This LSB's is may change the given bit into approximate value that is it may access the value in the given bit as 0. Then the Least Significant Bit (LSB) bit may use this approximate bit value finally it may deliver the value as detected value.

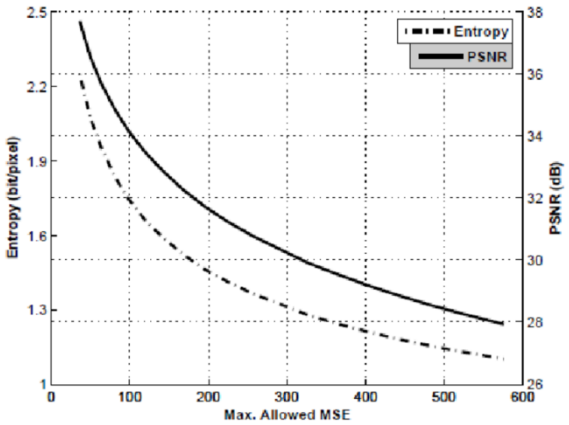

Fig.1.2 PSNR and MSE comparison.

The **MSE (**Mean square error) and **PSNR** (Peak signal-to-noise Ratio) are used to compare the given image compression in high quality. C.Nagarajan *et al.*[2] [7] [13] proposed the cumulative squared error between the compressed and the given output image may deliver the output with increasing values, whereas PSNR represent a measure of the peak error. The lower value of the MSE may be giver the output at lower error.

Let us consider the two bit as A and B with n-bit values. $A = A_0 \ldots A_{n-1}$ and $B = B_0 \ldots B_{n-1}$.
Then the given LSB bit has been changed the values. The basic comparison result of bit truncation of the PSNR and MSE values has been given below, the given bit truncation has been extend into proposed bit truncation values of the given general bit values.

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The comparison value of PSNR and MSE table is given below.

Binary values		MED (mean square error)		PSNR (Peak SNR)	
n	K	Proposed truncation (db)	Δ_{PSNR} (db)	Proposed truncation (db)	Δ_{MSE} (db)
8	4	38.7	+5.8	9.7	-21.5
	3	45.6	+6.5	5.7	-23.6
	2	57.8	+8.1	2.1	-29.8
16	**8**	**68**	**+8.4**	**8.7**	**-31.0**
	6	69.8	+8.9	10.8	-32.9
	4	81.7	+8.6	26.9	-35.8
32	16	89.6	+9.5	74.9	-39.8
	12	94.8	+9.6	145.8	-40.4
	8	101.6	+9.9	1975.2	-42.9

Table.1 Comparison table

In this comparison table the give bit has been compared by using the both value of PSNR and MSE. But in this paper the bit can be assigned and compared only with LSB (least significant bit). This adders may give the accuracy and approximate results but this results will be under certain condition. This may be used for many applications such as some basic uses are multimedia, DSP (discrete signal processing), DCT (discrete cosine transform), wireless network communication, etc,. This Adders may used to given the output values with approximation and this may be deliver the results in binary values process. The results level will be in dynamic process. During the stimulation of output bit the LSB (least significant bit) is only detected, this detection is done during the run time process. Then the values has been produced the approximate binary value results.

II. BINARY BITs APPROXIMATE ADDITION

Let us consider 16 bits binary values, this bits may be separate into two bit as k-bit and h-bit. The values of the bit has been given as both accurate and inaccurate values. The bit has been goes under the tradition bit truncation, this truncated values produced the approximate results. The h-bit may truncated as accurate value whereas the k-bit may truncated as inaccurate value.

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Binary bit values has been truncated and this approximation addition has been given below.

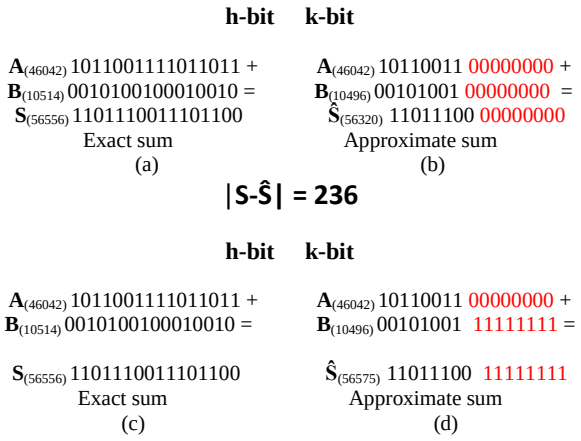

Fig 2.1 Bit truncation.

(a) traditional bit truncation for exact sum
(b) traditional bit truncation for approximate sum
(c) proposed bit truncation for exact sum
(d) proposed bit truncation for approximate sum

Let us consider 16bit binary values two number, these number can be assigned as A and B the by adding the binary values we get the result and this result can be assigned as S

In the Exact sum the value of bit $A_{(46042)}$ and $B_{(10514)}$ cab be added the it give the exact value and this value can be assigned as S then the value of the bit $S_{(56556)}$. But the value the k-bit can be assigned as 0's bit then the addition can be done as approximately. The value of the given bit can be assign as 0 then the addition result can also be changed.

After getting this addition results the value of h-bit results will be accurate and the value of the k-bit bit is inaccurate. By subtraction the two results of binary values we get 236 as results. Whereas by assigning the k-bit of $B_{(10514)}$ as 1's bit then the value has been changed as $B_{(10751)}$ then the addition can be done for this assigned bit this addition is only by done using the approximate values. In this value also the h-bit and k-bit values are accurate and inaccurate respectively. By subtracting the value of the bit we get 19 as result.

By comparing this two results both of then are different and this changes can be done only by changing the k-bit assignment. That is the value of k-bit can be assigned as 1's bit value.

Power consumption of the ACA adder can be roughly estimated as follows. Dynamic power consumption with voltage scaling at a fixed frequency is proportional to capacitance. Vdd2, where the capacitance is proportional to the area.

In general the implementation has been given by using the binary values of the given 16bit values. Then the values has been implemented by using the 0…n bit values.

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Therefore, with a random input vector, the probability it may given a correct result in the proposed adder is given as below. In the i'th sub-adder, errors occur when the LSB part of the result is may be changed by using the given equation below,

$$P(h, k) = \left(1 - \frac{1}{2^k} \cdot \frac{2^k - 1}{2^{k+1}}\right)^{\frac{N}{k}} - 1$$

III. PROPOSED MODEL

Bit Truncation method

Bit truncation scheme was introduced to inhibit the activity of the LSBs by zeroing the corresponding input bits. However, this approach was shown to suffer from ungraceful quality degradation at larger number of truncated bits.

This bit has been implemented by using the given bit values under the RCA implementation. Root Cause Analysis is a useful process for understanding and solving a problem. As an analytical tool, RCA is an essential way to perform a comprehensive, system-wide review of significant problems as well as the events and factors has been implemented by using the given values.

The given bit values has been signed and the input values has been given by the signed bit implementation their signed bit may deliver the results in unsigned bit. By using the signed bit values the values. This RCA has been implemented by using n-bit values this implementation has been assigned using the given binary values. This implementation has been assigned by using the AND and OR gate no more special gates has been used.

The RCA implementation has been used for n-bit values, this process has been described by using both AND, OR gates and no more special gates has been used. The given bit truncation has been used only for adders the values of the given bit may be assigned by using full adders. The N no. of bit has been implemented at a time. So we must used n-bit RCA has been used and this values has been connected with full adders.

A binary full adder is often found in the critical path of microprocessor and digital signal processor data paths, as they are fundamental to almost all arithmetic operations. The design of a gate level binary full adder ,based on and multiplexing control input technique for the carry and sum outputs, is given in the figure.

The RCA of n-bit has been implemented by using the values of both AND, OR gates values and no more special gates has been assigned for this process.

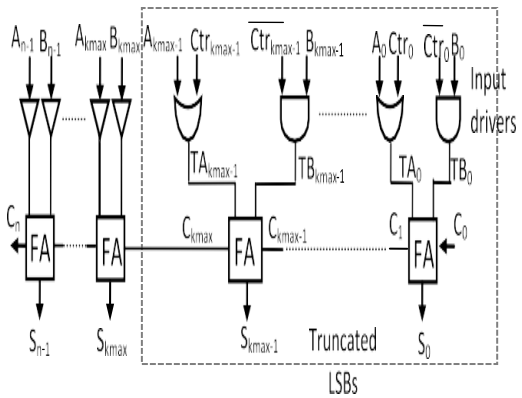

Fig 3.1 RCA bit truncation.

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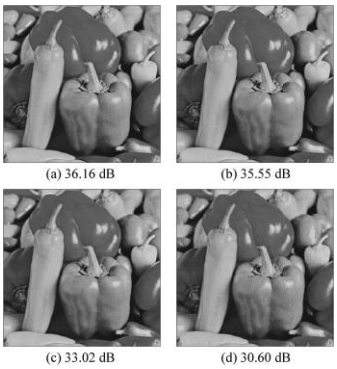

Fig 3.2 DCT Images

In the given image (a) the value of DCT has been detected as 36.16db whereas the following image (b,c,d) the value of DCT has been detected as 35.55db, 33.02db, 30.60db respectively.

The value of the PSNR table has been compared with energy level stimulation is may giver in the below bar graph.

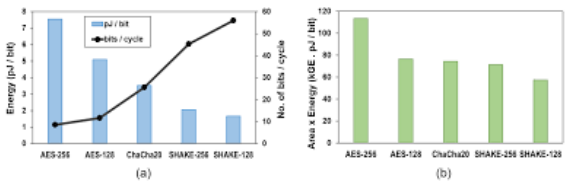

Fig 3.3 Comparison table.

IV. CONCLUSION

This paper presented the binary values is goes under the bit truncations process uses the non-zeroing bit truncation scheme. The value of the given input has been truncated the digits this may produced the value in non-zeroing bit levels. In this paper more than 32 bit has been proposed and they will deliver the output with minimum error. In the output value we increase the DCT as 35db, PSNR as 9.2 db and MED values use 75%. Finally the merits of out proposed system the value of DCT engines has been used with high quantified results, then the confirmed results has been essentially same as compared to the individual results. The proposed bit truncations has been deliver the results with minimum error by using more than 64 bit has been truncated.

REFERENCES

[1] J. Han and M. Orshansky, "Approximate computing: An emerg- ing paradigm for energy-efficient design," in Proc. ETS, May 2013, pp. 1–6.
[2] C.Nagarajan, M.Muruganandam and D.Ramasubramanian – 'Analysis and Design of CLL Resonant Converter for Solar Panel - Battery systems- International Journal of Intelligent systems and Applications (IJISA), Vol.5 (1),pp.52-58, 2013.
[3] M. Alioto, "Energy-quality scalable adaptive VLSI circuits and sys- tems beyond approximate computing," in Proc. IEEE DATE, Lausanne, Switzerland, Mar. 2017, pp. 127–132.
[4] M. Alioto, V. De, and A. Marongiu, "Guest editorial energy-quality and computing: From approximate to communication-inspired and learning-based," IEEE J. Trans. Emerg. Sel. Topics Circuits Syst., vol. 8, no. 3, pp. 361–368, Sep. 2018.
[5] D. Shin and S. K. Gupta, "Approximate logic synthesis for error tolerant applications," in Proc. IEEE DATE, Mar. 2010, pp. 957–960.
[6] F. Frustaci, M. Khayatzadeh, D. Blaauw, D. Sylvester, and M. Alioto, "SRAM for error-tolerant applications with dynamic energy-quality management in 28 nm CMOS," IEEE J. Solid-State Circuits, vol. 50, no. 5, pp. 1310–1323, May 2015.
[7] C.Nagarajan and M.Madheswaran - 'Stability Analysis of Series Parallel Resonant Converter with Fuzzy Logic Controller Using State Space

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Techniques'- *Electric Power Components and Systems*, Vol.39 (8), pp.780-793, May 2011

[8] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power dig- ital signal processing using approximate adders," IEEE Trans. Comput.- Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137, Jan. 2013.

[9] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 850–862, Apr. 2010.

[10] H. A. F. Almurib, T. N. Kumar, and F. Lombardi, "Inexact designs for approximate low power addition by cell replacement," in Proc. IEEE DATE, Mar. 2016, pp. 660–665.

[11] J. Miao, K. He, A. Gerstlauer, and M. Orshansky, "Modeling and synthesis of quality-energy optimal approximate adders," in Proc. IEEE/ACM ICCAD, Nov. 2012, pp. 728–735.

[12] F. Frustaci, D. Blaauw, D. Sylvester, and M. Alioto, "Approximate SRAMs with dynamic energy-quality management," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 6, pp. 2128–2141, Jun. 2016.

[13] K Umadevi, C Nagarajan, "High Gain Ratio Boost-Fly Back DC-DC Converter using Capacitor Coupling", 2018 Conference on Emerging Devices and Smart Systems (ICEDSS), 2nd and 3rd March 2018, organized by mahendra Engineering College, Mallasamudram, PP. 64-66,201

[14] M. Imani, D. Peroni, and T. Rosing, "CFPU: Configurable floating point multiplier for energy-efficient computing," in Proc. IEEE/ACM DAC, Jun. 2017, pp. 1–6.

[15] J. Park, J. H. Choi, and K. Roy, "Dynamic bit-width adaptation in DCT: An approach to trade off image quality and computation energy," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 5, pp. 787–793, May 2010.

[16] A. Dalloo, A. Najafi, and A. Garcia-Ortiz, "Systematic design of an approximate adder: The optimized lower part constant-OR Adder," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 26, no. 8, pp. 1595–1599, Aug. 2018.