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Review on Comparison of Symmetric and Asymmetric Multilevel Inverters for Dynamic Loads

Neha Bornare, Prof. Sushant Sananse

Department of Electrical Engineering, KCES'S COEIT Jalgoan, BATU University, Jalgoan, Maharastra, India

ABSTRACT: Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This paper implements and compares a symmetric hybridized cascaded multilevel inverter and an asymmetric multilevel inverter utilizing a switched capacitor unit for 17 level inverters. The symmetric hybridized multilevel inverter topology consists of a modified H-bridge inverter, which results in an increase in the output voltage to five level from the three level by using a bi-directional switch at the midpoint of a dual-input dc source. In the proposed asymmetric multilevel inverter, dc sources are replaced with the switched capacitor unit, which in turn boosts the output voltage and produces twice the voltage levels at the loads.

I. INTRODUCTION

In achieving higher voltage levels and power levels, cascaded multilevel inverters (MLI) are proven to be more flexible than conventional topologies. Its modularity property can be used to increase the power output of the inverter. Cascaded MLIs are constructed by linking in series output terminals of several H-bridge inverters. It is hence evident that this configuration supports high power levels with the use of low voltage rating components in inverters. In case of a fault in any one of the inverter cells, it can be easily and quickly replaced because of its modularity property. In order to maintain reliability in inverter output in the event of a fault in any inverter cell, a suitable control strategy can be used to bypass the faulty cell without disturbing the load.

A basic structure of 7-level multilevel inverter is shown in Fig. To obtain a 7-level multilevel inverter, three full bridge inverters are connected in series. Each full bridge inverter can generate three different voltage outputs: +Vdc, 0, and –Vdc. The phase output voltage is synthesized by sum of three inverter outputs, an a1 a2 a3 V =V +V +V
The number of output phase voltage levels in a cascaded multilevel inverter is 2S+1, where S is the number of dc sources. The values of dc sources used are equal which can be called as symmetric cascaded multilevel inverter. Each full bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase leg switching timings.

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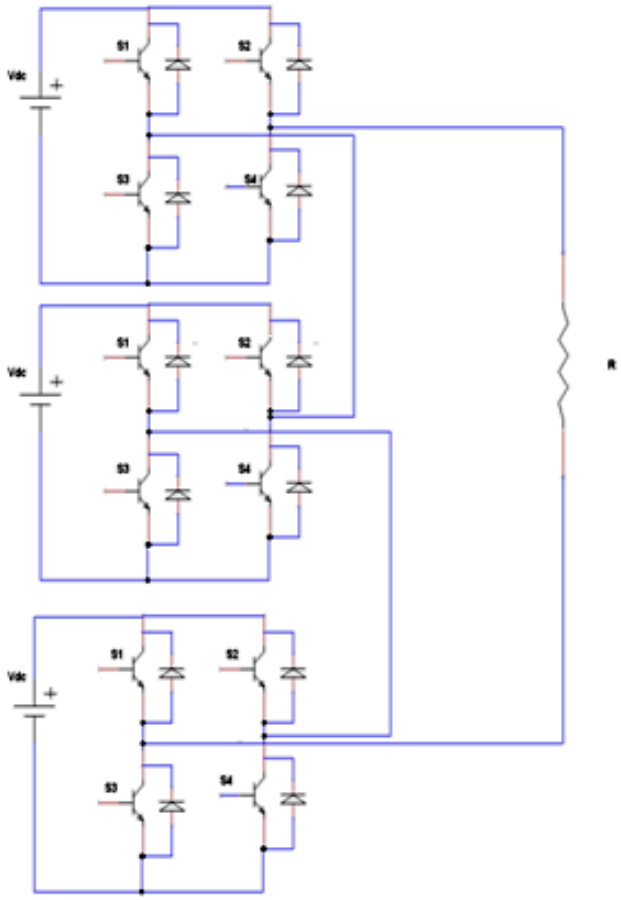

Fig 1. Circuit diagram of existing system

II. LITERATURE SURVEY

Tekale Anil A. et al [2] states that a Five-Level inverter are gaining attention, exertion are being directed toward attenuating the device count for increased number of output levels. A novel topology for Five-Level inverter has been proposed in this paper to attenuate the device count. The operating principle of the proposed topology has been illustrated and mathematical formulations suiting to output voltage, source currents, voltage stresses on switches, and power losses have been eliminate. Comparisons of the proposed topology with existing topologies acknowledge that the proposed topology significantly reduces the number of power switches and associated gate driver circuits.

Durga Prasad G et al. [3]studied A symmetrical MLI with reduced power semiconductor devices has been discussed in this paper where the required number of levels can be easily achieved by duplicating one source, active and passive switch in LGM. The performance of the topology is trustworthy as it operates only one high frequency switch for each level generation. The topology is simulated to observe the performance for R, and RL loads; and the results show that the percentage THD reduces to an acceptable standard. The proposed topology is investigated experimentally for the same loading condition and the test result validates the simulation results. The topology is tested for different control strategies and simulation results show that IPD-SPWM control method is best suited for the topology.

G.Lourds Sajitha and C.R.Balamurugan [4] examines the novel DC link coupled VL quasi Z source based reduced switch multilevel inverter. The proposed circuit has two combinations of switches that is low and high frequency switches. The VL Quasi Z Source inverter is connected in between these two switches. To analyze this circuit two references with PDPWM strategies with triangular carriers are used for generation of gate signal for switches. The proposed circuit is operated in three modes namely over modulation, under modulation and normal modulation region. During these modulation regions the performance in terms of THD and Vrms are obtained. Form the results its observed that both references almost gives less THD and Vrms is higher in the case of third harmonic injection reference. The results are satisfactory. Simulation is performed through MATLAB/SIMULINK software. Different rectified reference strategies with two references and triangular carriers have been developed using MATLAB-SIMULINK and tested for different modulation indices ranging from 0.6 to 1.5 for new topologies of VL qZ source

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based multilevel inverter. The proposed circuit may be employed for variable speed drives. By changing the modulation index in three different region like over, normal and under modulation regions the proposed circuit perform better for third harmonic injection reference in terms of THD and root means square value of voltage. All most both references gives less total harmonic distortion for both reference but the Vrms is more for THI reference. The results are satisfactory.

G Bhaskar Rao et al [5] proposed a novel SC-based cascaded multilevel inverter. Both 9-level and 13-level circuit topology are examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The accordant results of simulation and experiment further confirm the feasibility of proposed circuit and modulation method. Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by SC frontend. For instance, the number of voltage levels increases twice in half cycle of 9-level circuit, and the number of voltage levels increases three times in half cycle of 13-level circuit. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology and total harmonic distortion is reduced in 17 and 13- level inverter when compared to 9-level inverter the Meanwhile, the magnitude control can be accomplished by pulse width regulation of voltage level, so the proposed multilevel inverter can serve as HF power source with controlled magnitude and fewer harmonics. This project mainly analyzes nine-level ,13 and 17-level inverters. The method of analysis and design is also applicable to other members of the proposed inverter. The proposed inverter can be applied to grid-connected photovoltaic system and electrical network of EV, because the multiple dc sources are available easily from solar panel, batteries, ultra capacitors, and fuel cells.
John N. Chiasson et al [6] studied how to reduce harmonic distortion for a multilevel inverters. In this paper, the seven level inverter scheme with harmonics reduction was demonstrated. The harmonic reduction was achieved by selecting appropriate switching angles. The functionality verification of the seven level inverter was done using MATLAB.

S. Kouro et al [7] studied the working principle of single phase five level switched DC sources inverter and single phase five level cascaded H-bridge inverter. The Performances of single phase five level switched DC sources inverter and single phase five level cascaded H-bridge inverter were compared on the basis of number of switches used, voltage across switches, efficiency, total harmonic distortion (THD) of output voltage waveform and complexity of gate drive circuit. Single phase five level switched DC sources inverter and single phase five level cascaded H-bridge inverter were simulated using MATLAB/Simulink tool. The Performances of single phase five level switched DC sources inverter was compared with that of single phase five level cascaded H-bridge inverter on the basis of voltage across switches, efficiency, total harmonic distortion (THD) of output voltage waveform using MATLAB/Simulink tool. The Prototypes of both single phase five level switched DC sources inverter and single phase five level cascaded H-bridge inverter were developed in the laboratory with two input DC voltage sources of 24V each and performances of both types of inverters were found out.
Krishna Kumar Gupta, and Shailendra Jain [8] studied a multilevel inverter that had been conceptualized to reduce component count, particularly for a large number of output levels. It comprised floating input dc sources alternately connected in opposite polarities with one another through power switches. Each input dc level appeared in the stepped load voltage either individually or in additive combinations with other input levels. That approach results in reduced number of power switches as compared to classical topologies. The working principle of the multilevel inverter was demonstrated with the help of a single-phase five-level inverter. The Single phase five level inverter was investigated through simulations and validated experimentally on a laboratory prototype. An exhaustive comparison of the switched DC source inverter was made against the classical cascaded H-bridge inverter topology.
Xiaoming Yuan and Ivo Barbi [9] Studied conventional two – level pulse width modulation (PWM) inverter provide less distorted current and voltage but at cost of higher switching losses due to high switching frequency. The comparison was made in three level and five level diode clamped multilevel inverter for total harmonic distortion. A sinusoidal PWM technique was used to control the switches of the inverter.
L. Tolbert et al [10] studied the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multi cell with separate DC sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters were also discussed. This paper also presented the most relevant control and modulation methods developed for different types of converters like multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination and space-vector modulation.

III. PROPOSED SYSTEM

The hybridised H-bridge circuit topology utilized as a part of the development and implementation of the 17-level symmetric inverter is, as shown in Figure.1. The operation of appropriate topology can be interpreted in terms of two-

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stages. In the first stage, the output levels +V1, 0, −V1 is delivered by the association of bidirectional switch to the second leg on H-bridge while in the second stage, the output levels +2V1, 0, −2V1 are generated. The generated five-level output voltage using symmetric basic hybridised cascaded MLI topology is depicted in Figure.2. The switching states representing the status of the basic MLI are given in Table 1.

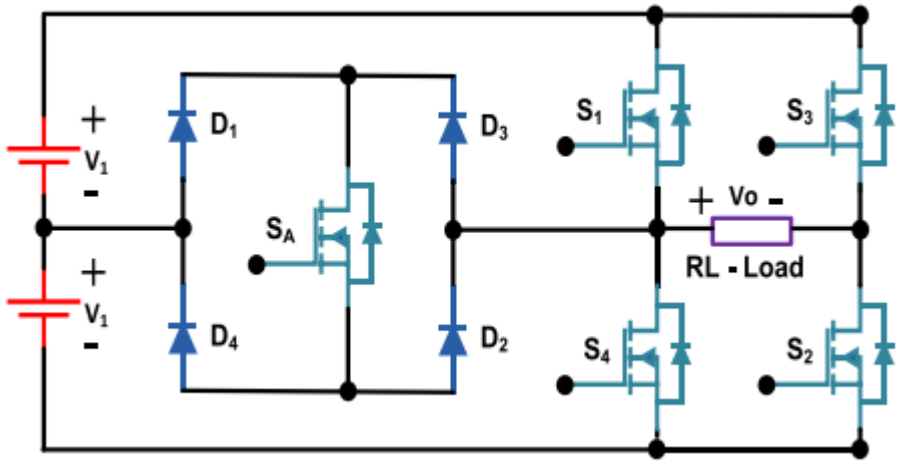

Fig.2. Basic Hybridised H-bridge topology.

TABLE 1. State table of proposed basic hybridized MLI.

Output voltage levels	Switching States				
Switches	S_1	S_2	S_3	S_4	S_A
+2 V	1	1	0	0	0
+1 V	0	1	0	0	1
0 V	0	1	0	1	0
0 V	1	0	1	0	0
-1 V	0	0	1	0	1
-2 V	0	0	1	1	0

BLOCK AND CIRCUIT DIAGRAM

The proposed 17-level symmetric hybridized cascaded MLI is illustrated in Figure.3. In this topology, the operation of every H-bridge is similar to the basic Hybridised H-bridge topology as indicated in Figure. 1. In this symmetric inverter, pulses are generated using staircase modulation scheme for obtaining different output voltage levels. The pulses are generated individually and fed to the first, second, third and fourth stage respectively and finally, all the outputs of the individual stages are combined to obtain the required output voltage. The control states of the power switches are illustrated in Table 2. In this proposed topology, all the input voltage sources are fixed as V = 25 V for acquiring the maximum peak to peak voltage of 200 V at the load ends. The loads used for testing are 100 ☐resistor and 175 mH inductor respectively. The voltages at various stages, output voltage and current are shown in Figure.4.
Table Switching state table of 17-level symmetric MLI.

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V_O	1	2	3	4	5	6	7	8	0		-1	-2	-3	-4	-5	-6	-7	-8
S_1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_3	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_4	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S_5	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_6	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_7	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_8	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
S_9	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
S_{10}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{11}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{12}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S_{13}	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
S_{14}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{15}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{15}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
S_A	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
S_B	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
S_C	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
S_D	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

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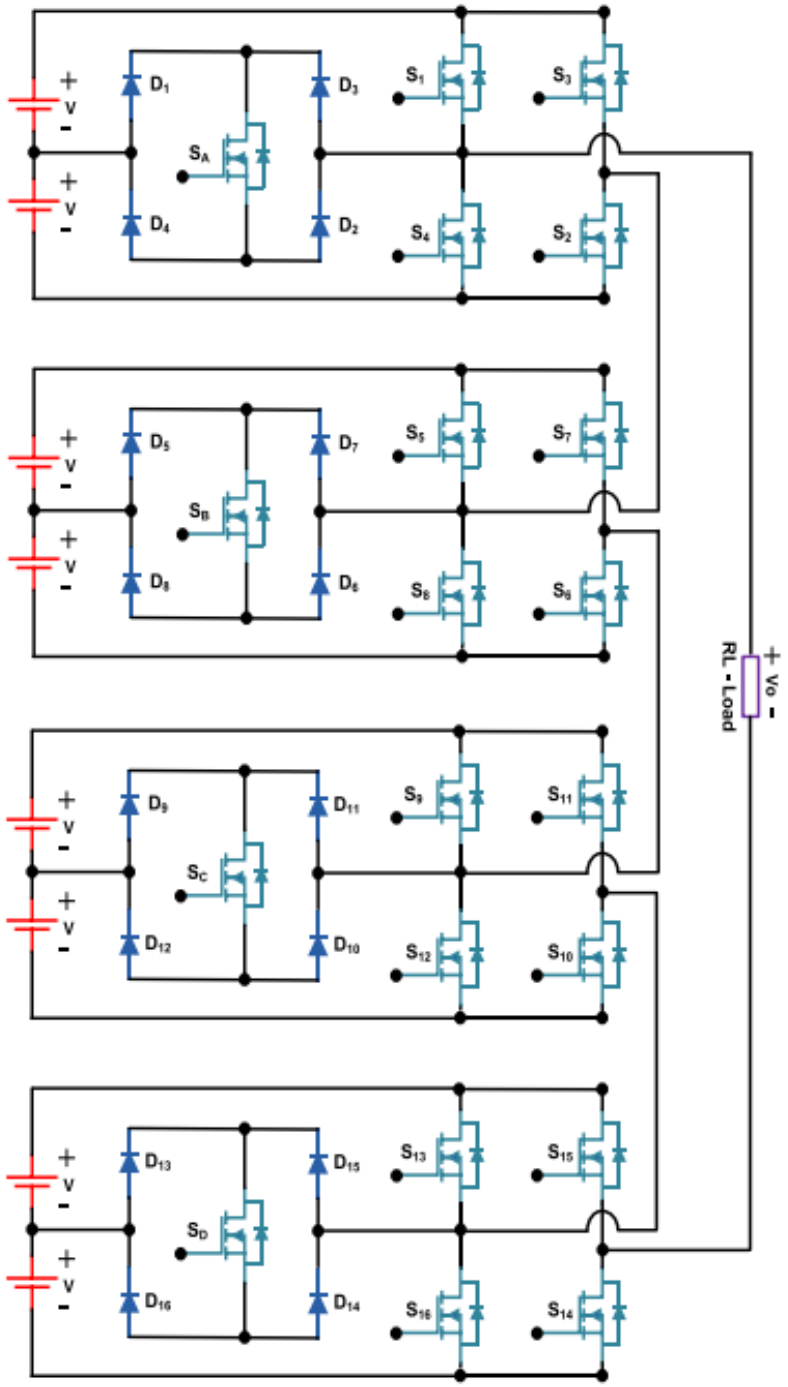

Fig 3. Proposed 17-level symmetric MLI

IV. CONCLUSION

This research presents the implementation and analysis of a 17 level symmetric and asymmetric multilevel inverters. The proposed 17 level inverter systems have been effectively tested with unity and lagging power factor loads. In case A, testing has been carried out under steady-state condition, load disturbance conditions and analysis of THD with 17 level symmetric inverter output were presented.

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