International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE)

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

A Relative inspection of Delay line in CMOS and CNT utilize LECTOR Technique at 32nm Technology

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ABSTRACT: An analytical standard for figuring the flow of current, postponement, and intensity of a submicron CMOS inverter is displayed. In this current research three stage delay line designed with lector technique for reduction in leakage power without increasing the propagation delay. A lector technique is warned two LCT transistor which one of p-type and another one is n-type at each stage of Delay line and LCT is manage by source of second LCT transistor. In this current commodity is simulate and compare the various aspects are power dissipation, frequency, average power of three stage delay line based CMOS as well as CNT at 32nm transistor based technology with the help of lector technique then comparison CNT based transistor better result display as compare to the CMOS based transistor using SPICE simulation tools.

KEYWORDS: CMOS, carbon nano tube (CNT), lector, leakage power, leakage current

I. INTRODUCTION

To minimize the rationale circuit configuration time, PC supported outline apparatuses must incorporate productive procedures for the quick, yet sensibly precise, estimation of basic way delays, control scattering, and pinnacle supply streams in computerized incorporated circuits. The issues of controlling the timing and the power utilization are developing as CMOS innovation progresses. For unwavering quality outline, the pinnacle supply-current values are additionally expected to appropriately estimate the power and ground lines with a specific end goal to keep away from electro migration disappointments and voltage drop issues [1].

The Delay processed utilizing the proposed display are contrasted and those created by HSPICE for a huge inverter (m). Note the understanding even for a heap of 250 fF, which is little for such a substantial inverter. At that point, to confirm the legitimacy of the model over an extensive variety of inverter sizes, the postponements on account of a base size inverter (m) are looked at. The exactness of the model over an extensive variety of exchanging conditions is exhibited, where the info progress time is changed over the range ns, and the relating delay is plotted for a few estimations. Note that ns compares roughly to the change time of the scorch. The transients signal of paired interconnect lines may differ remarkably with the input-switching device [8]. The multi paired RC/RLC interconnect lines are despaired into potent RLC-model-based signal transient pitch of the casualty line due to the imbalance switching time difference (culprit signals assault the casualty line at t = t). V represents a marvelous harmony (solid line) with the generic paired line model (dotted line). Figure1. RLC-model-based delayed comeback of the casualty line for the two cross-coupled switching lines with an imbalance of the rise times of the casualty line input signal. Single line structure is readily returning the transient signal characteristics being the input switching ornament. For the RC-dominant paired lines, modeling three-coupled lines, the center line is decoupled through engage a potent capacitance. In contrast, for the RLC-paired lines, carving more than three lines, the center line is decoupled by operate a potent capacitance and an effective inductance. The potent single-line model-based signal transient characteristics for multi coupled lines show excellent agreements through SPICE simulations utilize the generic paired line circuit structures. Thus, with the proposed multiline decoupling approaches, the dynamic signal timing of the multi paired lines due to the input switching ornaments can be exactly as well as efficiently determined. The modeling can be straightly

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as well as neat employed for the dynamic timing verification of today's strongly-coupled DSM-based VLSI circuit interconnect.

The resolution of the highest and the maximum delay step is determined via optical delay lines. They reveal the hold up of even the minutest picoseconds ranges amidst the increments which are linear. If the space distance amid input and output fiber optic transceiver is adjusted then also the signal is delayed. This illustrates that as the distance of a light flow is greater amid the two points, the output signal will be hold up simultaneously. There is a limitation of the optical delay being the delay range which is just few 100ps. When there are extremely long delays, there are various optical delay lines which on maintaining their linearity and resolution extend the ranges. But, these are earned on the foundation of the complexity of the system as fiber optic cables are being amidst exhibiting an expensive, fragile and bulky setup. On comparing this system with the existing one there is a reduced system complexity and the costs too [2].

Further, there are two main limitations along with the CMOS delay lines for the conventional ones. The first and the foremost drawback are jitter performance, considerably launching under the picoseconds. On comparing both the CMOS and the optical fiber the former is used more as they reduces the cost and integrates the system as the delay lines which are robust in nature as compared to the latter optical counterparts. The long delay range is linear including the delay steps of high resolution but realizing a long range of delay is mainly the second issue. The delay lines of the CMOS cannot be cascaded as they exhibit a very fine and high resolution whereas optical delay lines can be easily cascaded as the increments of the delay are non-linear. The reason behind it is their nature of complex parasitic capacitance network within the delay elements of delay line. The implementation of PCB is leaded in a complex manner because of the cascading methodology. Thus, there is s necessity of developing a single chip solution for overcoming of the shortcomings [3].

Currently, the complexity of the chip is enhanced and the size of the feature decreases according to the advancement of the VLSI technology, thus enhancing both the size as well as the density of the device circuits. As there is a continuous increase in the lengths of copper and aluminium interconnects technology, some serious issues caused being electro-migration and formation of voids in various levels of path interconnect [9]. Because of this reason new materials were introduced like the carbon nano tubes as they were the easiest possible solutions. CNT are made by the graphene sheets and are known as allotrope. In these the sheets are rolled into a cylinder form. the regulation of the graphene sheet rolling examined the chiral indices and the structures of the CNTs. Depending upon the chiral indices of the structure is determined of the CNT, it exhibits zigzag or the armchair structure. The metallic and the semiconductor properties of the CNT depends over the type of the structure as well as the chiral indices. As, the thermal and the electrical properties of these CNTs are excellent, therefore they are in demand now-a-days [4].

II. LITERATURE REVIEW

Jatinderpal et.al in 2014 stated that these CNT multi walled tubes are probing attention and are one of the promising methods regarding the utilization of the nano-electronics in near future. They empired that they revealed the replacement potential above hitch of the chip copper (Cu) as they have huge carrying capacities of current and conductivity. Amongst the integration modules, one of the main constraints of modules is delay on the large scale policy of VSLI. They have explored about the trimming time and insertion repeater attains on that retard for both couples of MWCNT and Cu utilize the various nodes of the methods i.e. 32 nm and 22 nm respectively. The current articles trades in amidst voltage scaling effects in the repeaters for lengths of long interconnect in the modules of VSLI regarding the propagation delay. The reduction in the propagation delay can be attained amidst enhancing in bias repeater voltage at various interconnects of various length and nodes of technology of 32 nm and 22 nm respectively [6].

Majumdar et.al in 2012 stated that the accurate hierarchy modeling for the interconnect bundle for the assorted CNT. They also proposed various bundled structures based above the hierarchical structure. These proposed for different arrangements for single walled CNTs too MWCNTs. Utilize an equivalent single conductor all various model of the bundle of assorted CNTs was also developed. This assorted CNT was constructing through the combination of single walled CNTs and MWCNTs. Below the attained of the dynamic crosstalk; there propagation delay was further compared regarding the structures which were proposed for the assorted CNT bundles. The results indicated that the delay time improves significantly which was introduced or induced via crosstalk regarding the structures in which the peripheral space was occupied via MWCNT and the remaining SWCNT occupied the centre space of the bundle [7].

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III. RESEARCH METHODOLOGY

A delay line circuit is a simple way of scheme to reducing power dissipation. CMOS based transistor to be used for design three stage delay line. In this circuit output of first inverter are connected to the input of next inverter and so on. CMOS based three stage delay line as exhibits in figure 1.

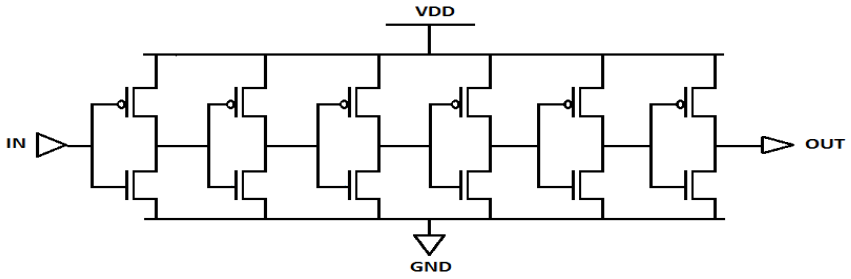

Figure 1: Three Stage Delay Line using CMOS Technology

Now design three stage delay line with carbon nanotube transistor based technology because CNT reduce leakage power due to smaller and shorter channel length and CNT made of rolled sheet of grapheme so that it is like a cylindrical shape as showing in a figure (2).

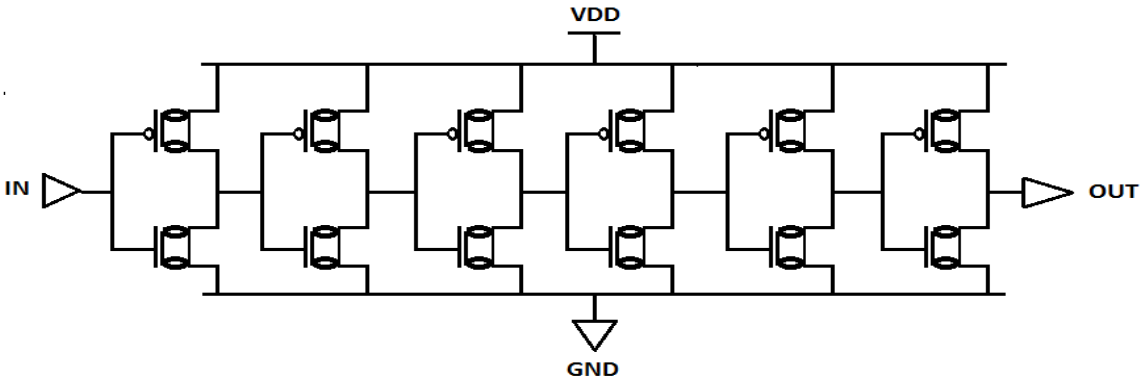

Figure 2: Three Stage Delay Line using CNT Technology

Lector technique to apply in CMOS based three stage delay line as showing in a figure (3). In this circuit six inverters are connected in parallel at each inverter has made of one PMOS and other one NMOS transistor in that circuit.

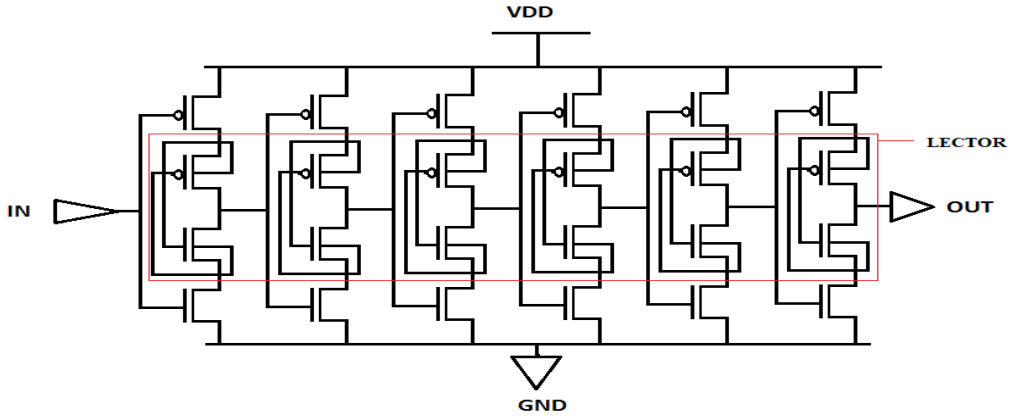

Figure 3: Three stage CMOS based delay line with lector technique

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In the control box, Leakage controlled transistor (LCT) is attached in series connection of each five inverter M2 (PMOS) and M3 (NMOS) which are LCT. Leakage controlled transistor are fix among pull up and pull down mesh. Gate terminal M2 is connect to the source of M3 and gate M3 is connect to the source M2. Similarly design CNT transistor based ring oscillator operates lector technique as showing in a figure (4).

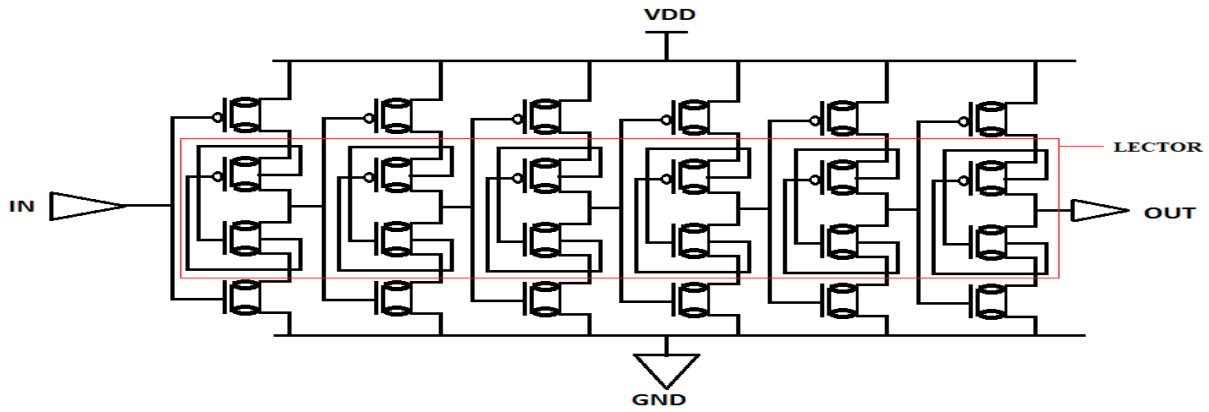

Figure 4: CNT Transistor based Three Stage Delay Line Circuit applying Lector Technique

IV. SIMULATION AND RESULTS

The proposed pattern is simulated employ spice tool at 32nm node of both CMOS and CNTFET based three stage delay line utilize LECTOR technique. The length and width are taken as L=32nm and W=32nm at 1V source is appealed. Simulated waveform of three stage CMOS based delay line employ lector technique as shown in figure 5.

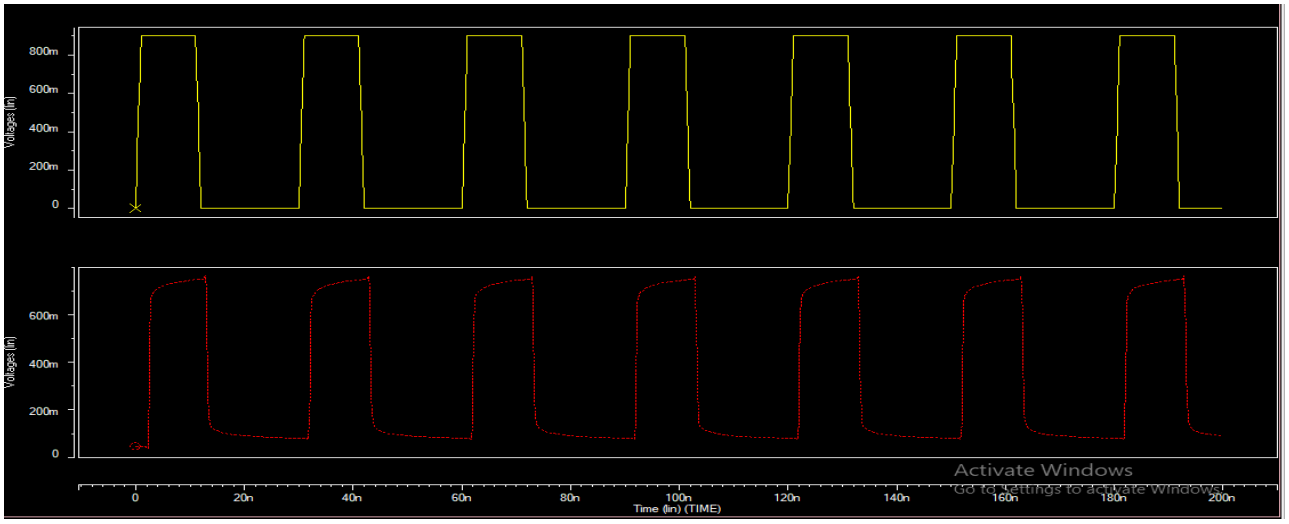

Figure 5: Waveform of Three Stage CMOS based Delay Line using Lector Technique

Simulated waveform of three stages CNTFET based delay line with lector technique to diminished delay signal and diminished power consumption in comparison of CMOS technology as clearly represent in figure 6.

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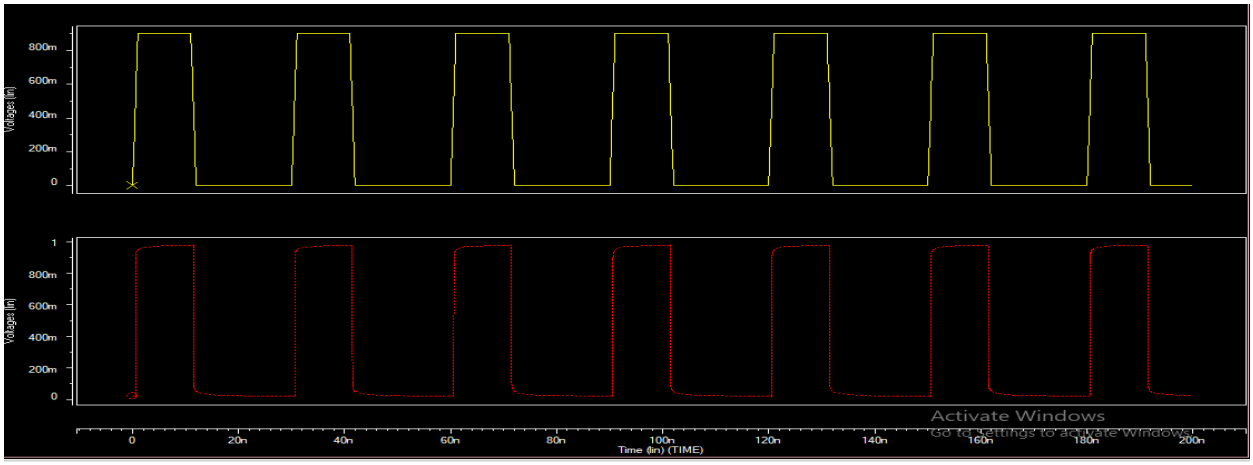

Figure 6: Waveform of Three Stages CNTFET based Delay Line with Lector Technique

In fashionable physical science manure, high performance of integrated circuits (ICs), actually five hundredth of the entire mode of energy is dissolve because of the sweep power, with extra transistors integrated on-chip, sweep currents will quickly govern the entire power consumption of high performance ICs. Relation between leakage current and power is given by

$$Pleak = Ileak.Vdd \quad (1)$$

Where,

P_{leak} = leakage power

I_{leak} =leakage current

Vdd = Supply voltage

In this relation we have to determine leakage power as well as leakage current. When supply voltage is 1V then leakage power and leakage current are same but in opposite direction.

Table 1- comparison with CMOS,CNT, lector CMOS, and lector CNT with spice tools.

Performance parameter	Delay Line			
	CMOS	**CNT**	**LECTOR CMOS**	**LECTOR CNT**
Technology	32nm	32nm	32nm	32nm
Supply voltage	1V	1V	1V	1V
Delay	10.9nS	10.8nS	10.4nS	10.2nS
Leakage power	1.595nW	0.843nW	0.98nW	0.45nW
Leakage current	1.595nA	0.843nA	0.98nA	0.45nA

Table 1 illustrates the simulation results of Delay Line. In CMOS based Delay Line with the help of LECTOR technique gives leakage power is 0.98nW and delay is 10.4nS is to be determined with the help of SPICE simulation tools. CNTFET based Delay Line leakage power was diminished to 0.45nW and delay is reduced to 10.2nS at 1V power Supply. Graphical representation of all Parameter was determined in both CMOS and CNTFET as shown in Figure.

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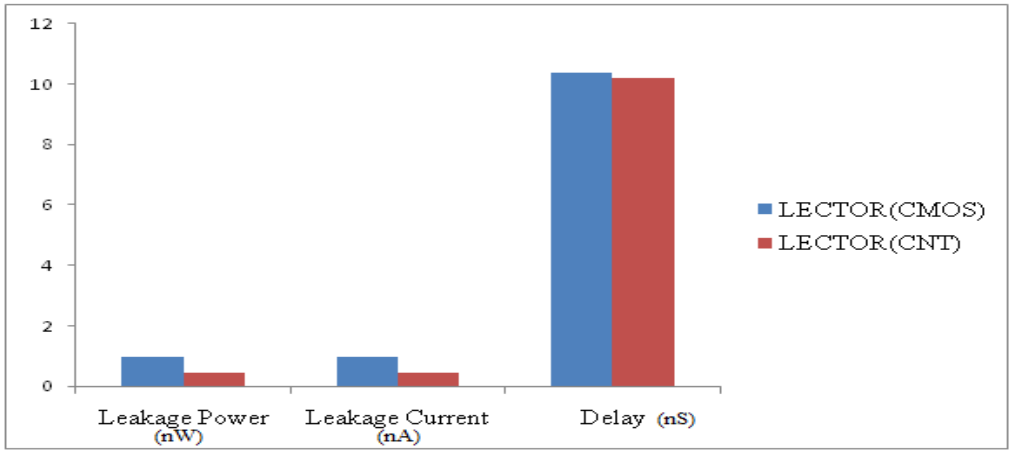

V. CONCLUSION

A three stage delay line was successfully planned and simulated utilize spice tools at 32nm channel length. The main target of this article is to be diminished the power dissipation and time delay of the signal of entire structure. We create the previous paper work by reducing voltage and using CNT technology and the result in the table (1) presently comparison between CMOS and CNT. According to the acquired simulation results we judge that the proposed three stage delay line with lector technique perform better result in the term of power dissipation and leakage current is diminished to 0.45nA at 1V. Therefore lector technique is to control leakage power for the circuit designers.

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