International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE)

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

Design and Estimation of Ultra Low Power 2x1 Multiplexer utilize MTCMOS Technique

Anjum Aara[1], Shushant Kumar Jain[2], Pradeep Yadav[3]

PG Scholar, Department of Electronics & Communication Engineering, ITM Universe, Gwalior, Madhya Pradesh, India[1]

Assistant professor, Department of Electronics & Communication Engineering, ITM Universe, Gwalior, Madhya Pradesh, India [2,3]

ABSTRACT: As transistors sizes downsize and levels of mix expand, spillage control has turned into a basic issue in present day low power gadgets. In this article we proposed a power diminishment system called 'MTCMOS'. MTCMOS technique gives two sleep mode transistors in current circuits are engage to diminished power consumption. In this proposed work is to construct low power 2*1 multiplexer using MTCMOS technique in 32nm both on CMOS and CNTFET. The proposed circuit to be enhanced in terms of leakage power, current and propagation delay for CMOS and CNT based 2*1 multiplexer has been construct by MTCMOS technique at 1V power supply. The proposed design is simulated using SPICE tool in 32nm technology node. After simulation it is established that results give a notable reduction in leakage power or delay for current design. Leakage power offers by MTCMOS approach in CNTFET based technology are 2.658pW and delay is diminished to 22.40nS at 1V power supply.

KEYWORDS: 2*1 MUX, CMOS, CNTFET, MTCMOS, SPICE Tool.

I. INTRODUCTION

Very large scale integration is that technology for intriguing of an integrated circuit (IC) by mixing thousands of transistors into a single chip. It is the proposal of truly small, complex circuitry with the help of semiconductor components. It may accommodate millions of transistors provide on single chip is familiar as Integrated circuit (IC). VLSI technology is built on Moore's law. According to the Moore's whole of transistors in an opaque integrated circuit doubles around each eighteen months. VLSI fabrication automation is immobile in the action of evolution which is dominating to smaller line widths and aspect size and to higher bulk of circuitry on a chip. Diminishing the aspect size is generally immobile to improved performance. Micro electronics technology is that technology to be designate in terms of different figure of merits [1].

The scheme strives have concentrate on optimizing speed to discern computationally exhaustive real-time tasks such as video compression, gaming, graphics etc. There are various aspects of technology evolution in the VLSI scheme such as 90nm, 65mn, 45 nm, 32 nm etc. These technologies are worn to enhance the performance of the circuit in idiom of power, area, delay etc. These technologies build upon the distance amid sources and drain [2]. For instance, in triple-RC-coupled lines, the flag spread deferral of the inside line might be half longer or half shorter than that of a solitary separated line with the same physical structure. Since the info exchanging designs shift to some degree haphazardly with circuit activity, they might be considered to be basically probabilistic in nature. In this way, the impacts may bring about a huge (deterministic) circuit timing jitter, in this way prompting the noteworthy planning skew. Lamentably, since flag coupling between IC lines turns out to be significantly more noteworthy with DSM forms, the information exchanging design reliance of the flag transient qualities will cause numerous more basic planning issues. Notwithstanding customary design based flag honesty portrayals, input-exchanging design subordinate flag transient attributes must be fused as a vital piece of flag uprightness check of dynamic circuit conduct in the circuit plan stage [3].

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

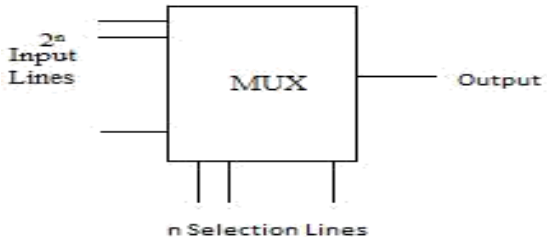


Figure 1: Block diagram of Multiplexer

Multiplexer means that many into one. Multiplexer is a too which prefers one out of numerous inputs on the shriek control lines. A multiplexer circuit that is worn to prefer and path of the various input signals to a single output. Figure 1 represents the traditional intension of a multiplexer with 2^n input signal, n control signals and one output signal. An effortless example of a non electronic model of multiplexer to single pole varied scene switch. Multiplexer is worn to perform high speed switching are fabricated of electronic components [5].

A 2x1 multiplexer is illustrating in figure 2 possess two inputs Io and I1, one selection line S and one output Y. The output equation of 2xI multiplexer is

$$Y=S'Io+ SI1 \qquad (1)$$

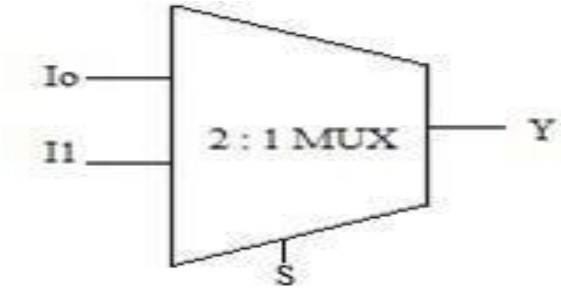


Figure 2: 2x1 multiplexer

II. LITERATURE REVIEW

Joseph et.al (2015) stated that the scheme of Schmitt trigger circuit is embraced of low voltage MOS transistor. The techniques were worn for implementation was named as DTMOS and multiple threshold MOS, VTMOS and FTMOS. This model was fabricated at 180nm CMOS technology operating TSMC for the conventional and the proposed circuits are stimulating at 0.5v power supply. They explored and compared to the concert of Schmitt trigger being hysteresis curve width, delay introduced, and consumption of power for the inputs as well as supply voltages. After attaining their outcomes of various applications for each of the Schmitt triggers were suggested [8].

Parakundil et.al (2014) stated that the most difficult and the crucial task for the circuits is the reduction or the minimization of the power consumptions. As the demand of portable devices is enhancing, so it is essential that these portable devices are designed with circuits consuming low power along with lesser dissipation of energy. The flip flops which are designed were both explicit as well as implicit. The circuits were diminishing of power consumption and the techniques to be applied in that circuit are MTCMOS and self tractable voltage level. The circuits which they designed were of 45 nm technology and the frequency taken was 1 GHz [10].

Coherent and unplanned process variations are most crucial drawbacks ahead of manufacturing the nanoscale apparatus and appliances. Now day's CNFET-based quaternary logic models are fabricated on multiple-Vth method, the collision of

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

the action imbalance, which oscillates the threshold voltages of CNFETs, should be surely conscious. The most significant idioms of threshold voltage of CNFET to be examined, diameter of nanotubes and the thickness of its gate oxide layer (Tox). While as the timing imbalance is considered as very important aspects for a circuit, delay attribute together with the energy dissipation of the proposed circuits are probe in the vision of process imbalance [4]. New high-speed, high-precision and PVT tolerant quaternary logic gates, decoder, multiplexer and arithmetic models have been proposed for nanotechnology, based on CNFETs. The proposed CNFET-based schemes have been fabricated on the CMOS-style binary gates, calmed of multiple-Vth nanodevices, and have exploited from the unique stuffs of CNFET. Additionally, the proposed MVL models are consistent with modern technologies. For manufacturing the proposed quaternary models having various CNT diameters, all are less than 2.3 nm, have been worn which improve the feasibility and manufacturability of the models. The simulation outcomes confirm the authenticity of the proposed approaches in various simulation situations as well as in the presence of tasks, voltage and temperature imbalances [6]

Additionally, the transient analysis of three-input quaternary MIN and MAX models are illustrated in figure. The proposed CNFET-based quaternary logic models and their 32 nm MOSFET complement were simulated i.e. 0.8 V, 0.9 V and 1 V and 250 MHz frequency, and their propagation delay, power consumption and energy consumption are tabulated in Table 3. According to the outcomes, the CNFET-based models are significantly surpassing their MOSFET equivalents in phrase of performance, power consumption and energy efficiency. Hereupon, Monte Carlo transient analysis with a logical number of 30 iterations for each simulation is governed. The statistical significance of 30 iterations is too high. If a scheme operates correctly for all the 30 iterations, there is a 99 % probability that above 80 % of all the viable component values operate properly [9].

III. CIRCUIT DESCRIPTION OF CMOS BASED 2*1 MULTIPLEXER USING MTCMOS TECHNIQUE

The leakage power or current is required to be more diminished to various modules has been implemented known as MTCMOS. As shown in figure (3) high V_t sleep transistor which are entrance of power supply and ground to the low V_t (Sleep Bar) results in diminish of the leakage power along with the embracing power dissipation in that circuit. This is constructing by integrated two sleep transistors in the CMOS based 2x1 multiplexer circuit. Figure (3) illustrate CMOS based 2x1 Multiplexer operate MTCMOS technique as shown.

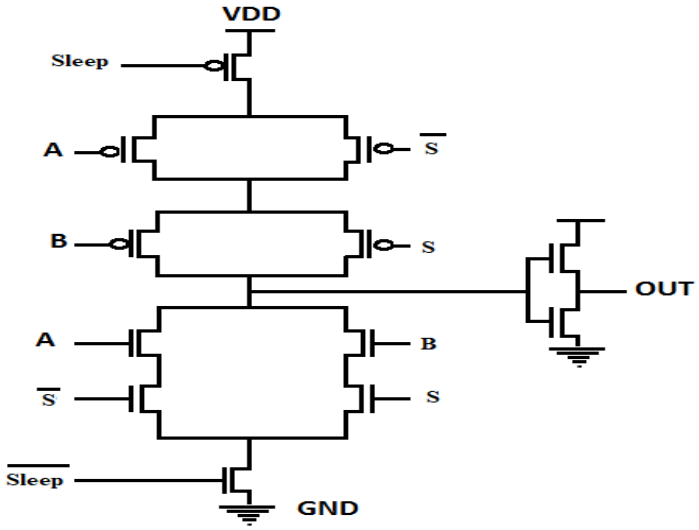


Figure 3: CMOS based 2x1 Multiplexer operate MTCMOS technique

IV. CIRCUIT DESCRIPTION OF CNTFET BUILD LOW POWER 2X1 MUX OPERATE MTCMOS TECHNIQUE

Transistor P1 is a sleep transistor and transistor N4 is sleep bar transistor. These two transistors provide by MTCMOS technique and rest of the part is conventional 2x1 MUX circuit. Transistor P1 is attached to the virtual VDD of

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

conventional 2x1 MUX and transistor N4 is connected to virtual GND. When low input signal is applied in proposed circuit sleep transistor P1 is OFF condition and sleep bar transistor N4 is ON means working condition. Alternately, high input signal is applied in this circuit P1 is ON and transistor N4 is OFF (standby) condition. Figure 4 represents CNTFET based 2x1 MUX using MTCMOS technique. We have to replace CMOS transistors by CNTFET transistors because it can work in nanometeric condition and reduced sizes of the circuit and reduced power consumption as compare to CMOS circuit.

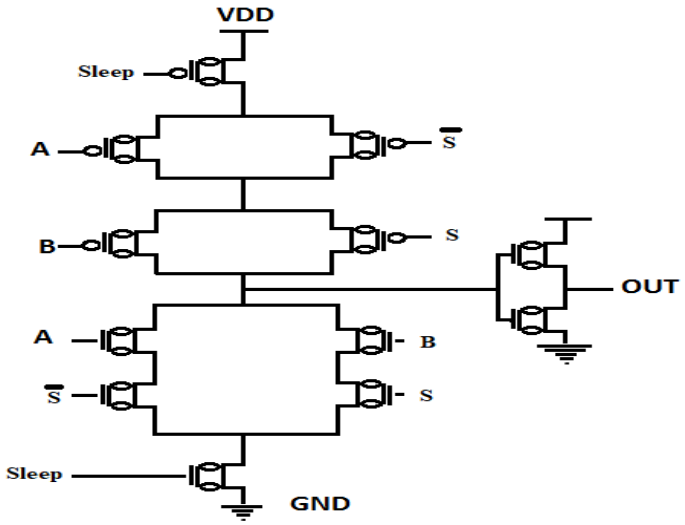


Figure 4: CNTFET based 2x1 MUX operate MTCMOS technique

V. SIMULATION AND RESULTS

The proposed 2x1 multiplexer circuits were simulated using SPICE tools in 32nm technology and their transient analysis or curve waveform is acquired at 1v power supply. Figure 5 represents the simulated waveform of CMOS based 2x1 multiplexer employ MTCMOS technique.

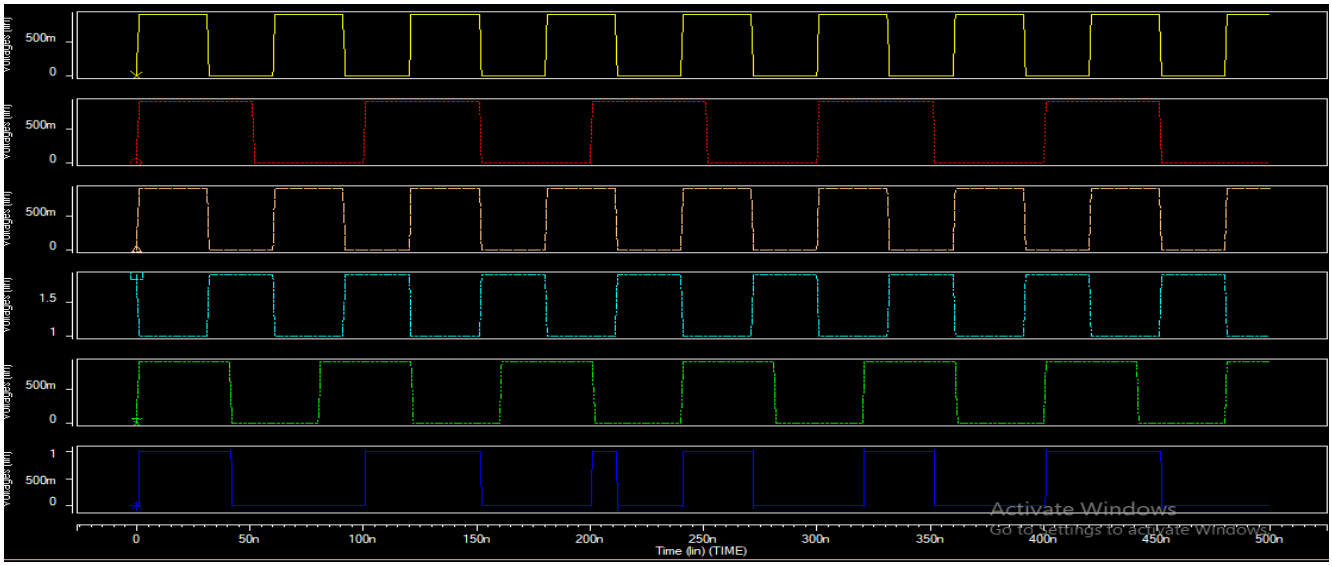


Figure 5: Simulated waveform of CMOS based 2x1 MUX employ MTCMOS technique

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

Similarly, figure 6 represents simulated waveform of CNTFET based 2x1 multiplexer use of MTCMOS Technique. In case of figure 6 clearly seen to better waveform result in comparisons of CMOS waveform.

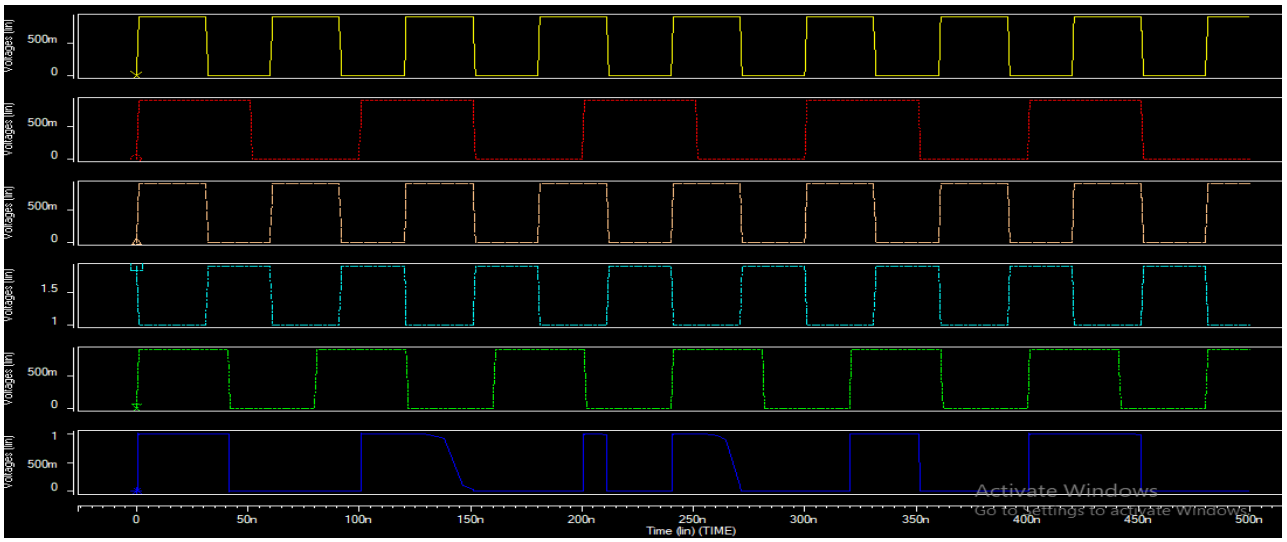


Figure 6: Waveform of CNTFET based 2x1 multiplexer using MTCMOS Technique

Speed of digital circuits can be found by: Delay

$$td= (CL * VDD) /Ion\text{……..}(1)$$

Maximum clock frequency:

$$fc, max= 1/ (td * Ld)\text{……. } (2)$$

Where, CL= capacitance load

VDD=Power source

Ion= leakage current drawn by each switch in on state

Ld= logic depth (no of stages through which a switching event must propagate during one clock cycle)

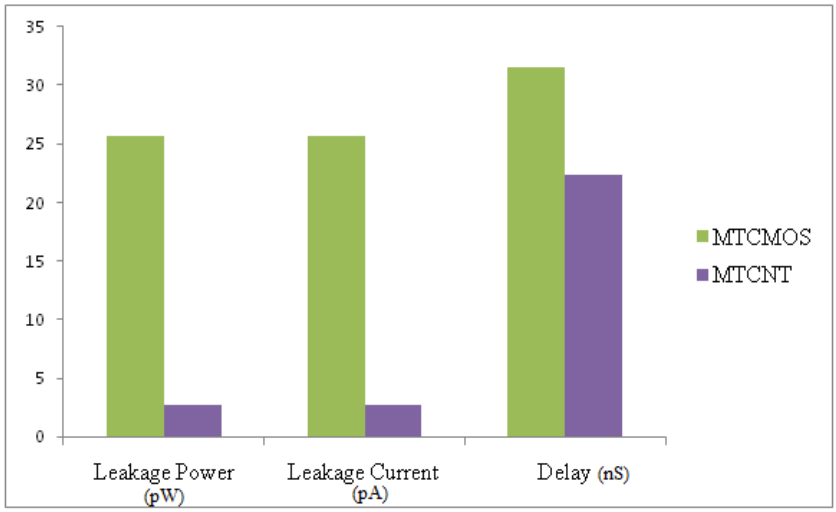
Table 1 Represent a Relative Analysis of Both CMOS and CNTFET 2*1 MUX Using MTCMOS Technique.

Performance parameter	2*1 Multiplexer			
	CMOS	CNT	MTCMOS CMOS	MTCMOS CNT
Technology	32nm	32nm	32nm	32nm
Supply voltage	1V	1V	1V	1V
Delay	40.86nS	40.84nS	31.57nS	22.40nS
Leakage power	504.218pW	319.20pW	25.684pW	2.658pW
Leakage current	504.218pA	319.21pA	25.684pA	2.658pA

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

Table 1 illustrates the simulation outcomes of 2x1 Multiplexer. In CMOS based 2x1 MUX by virtue of MTCMOS technique gives leakage power is 25.684pW and delay is 31.57nS is to be determined with the help of SPICE simulation tools. CNTFET based 2:1 multiplexer leakage power was diminished to 2.658pW and delay is reduced to 22.40nS at 1V power Supply. Graphical representation of all Parameter was determined in both CMOS and CNTFET as shown in Figure.



VI. CONCLUSIONS

Proposed circuits are design and simulated using SPICE tool in 32nm technology at 1V. Power consumption in CNTFET based 2*1 MUX using MTCMOS technique is 2.658pW. Propagation delay in 2*1 MUX based CNTFET technology using MTCMOS technique to be diminished for conventional circuit is 22.40nS but the vital concept of this proposed work to diminish power consumption and better efficiency of that circuit. So that CNTFET 2*1 MUX using MTCMOS technique gets better results in comparison of other conventional circuits.

REFERENCES

[1] Weste, “CMOS VLSI Design: A Circuits and Systems Perspective”, 3rd Edition, Pearson, 2010.
[2] V.S. Ingole, Prof. V.T. Gaikwad, “Design of Multiplexer using CMOS Ternary Logic”, IJERA, Vol. 2 Issue-2, April 2012.
[3] Maruf M. Ali, S.M. Maniul Islam, Md. Mehedi Farhad, ”Analysis of CMOS Multiplexer of different area and logic styles”, IOSR-JVSP, Vol. 3 Issue-6, Dec 2013.
[4] Vandana Shukla, O.P. Singh, G.R. Mishra, R.K. Tiwari, “ Novel design of a 4:1 Multiplexer circuit using Reversible Logic”, International Journal of Computational Engineering Research, Vol. 3, Issue 10, Oct 2013.
[5] Meenakshi Mishra, Shyam Akashe, “High Performance, Low power 200Gb/s 4:1 MUX with TGL in 45nm Technology” Springer, 2013.
[6] Arun Kumar, Manoj Sharma. “Design and analysis of Mux using Adiabatic ECRL and PFAL” ICCAI , pp. 13411345, 2013.
[7] Y.Syamala and A.V.N.Tilak, “Synthesis of Multiplexer and Demultiplexer Circuits using Reversible Logic,” Int. J. of Recent Trends in Engineering and Technology, Vol. 4, No. 3, Nov 2010 © 2010 ACEEE DOI: 01.IJRTET.04.03.12034 .
[8] Joseph, Richa Shukla“Performance evaluation of low voltage Schmitt trigger using variable Threshold Techniques”. IEEE (2015).
[9] Ira Parashar, Preeti Sikarwar, Rashmi Singh, Soumya Chauhan, Mrs. Shivani Saxena, “Design And Simulation Of 4*1 Mux Based On Low Power Design Techniques,” SSRG International Journal of VLSI & Signal Processing (SSRGIJVSP) – volume 2 Issue 2 March-April 2015 ISSN: 2394 - 2584 Available: www.internationaljournalssrg.org Page 6.
[10] Parakundil, N.Saraswathi “Low Power Pulse Triggeredn D-Flip Flops using MTCMOS and Self Controllable Voltage level Circuits” ICACCCT Conferrence, May 2014.