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Design and Comparison of the EMC and Efficiency Characteristics of the Hard and Soft Switching Multilevel Inverter

Suman Chaudhary, Anurag Govind Rao,

Master of Technology (M.Tech), Dept. of Electronics Design & Technology, NIELIT Gorakhpur,

Uttar Pradesh, India

(Deputy Director-'T'), Dept. of Electronics Design & Technology, NIELIT Gorakhpur, Uttar Pradesh, India

ABSTRACT: In this thesis a new Soft Switching circuit for Five Level Inverter is proposed with traditional Pulse Width Modulation (PWM) technique & Passive snubber circuit also. In this model extra switching losses are reduced and Electromagnetic Interference (EMI) noises also decreased by using Soft Switching circuit technique. Total Harmonic Distortion (THD) is reduced so find a better output and increased the efficiency of Five Level Soft Switching Inverter. In this paper Zero current source (ZCS) and zero voltage source (ZVS) technique are achieved so stress on the switches are reduced. Finally designing of soft switching circuit for five-level inverter with passive snubber is done for single phase prototype proposed inverter. A new 'Soft Switching Five Level Inverter (S5L Inverter)' which is now available provides reduced switching losses and higher efficiency. S5L inverters provide higher efficiency and additionally advantages in electromagnetic compatibility due to the soft switching performance, especially when using the 'Soft- Switching Passive Snubber Five Level Inverter'. A Soft Switching Active Snubber circuit inverter has been proposed; due to lack of lower order harmonics, high quality output is obtained. The new system makes fewer switches at the same stage. A typical method of control was limited primarily to the direct and indirect operation of the inverter. A multi-level power inverter method has been used in high and medium voltage conditions as an option. This multilevel inversion method not only reaches high power levels but also increases the complete system's performance in terms of harmonic distortion, dv / dt stresses and tension in the motor covers. Many topologies were created for multilevel inverters: i) diode clamped, ii) flying condensers, and iii) cascaded H-bridge. A cascaded multi-level inverter with independent DC outlets is the most feasible topology for compact and extensible modularization for medium and high power applications of control inverters. A H-bridge inverter displays large number of (i) large-level transformers, (ii) multi-level diodes, (iii) multi-level diode-clamped inverters, (iv) flying condensers required by flying-capacitor multi-level inverters. This study analyzed and contrasted the most rising topologies contained in publications. The first criteria were clarified and contrasted by different approaches to the design of multilevel inverters. Total harmonic distortion and modulation which for multilevel converters are necessary or desirable is addressed. Circuit function and control signal was represented by MATLAB. Multi-level inverters are implemented in MATLAB / SIMULINK applications for Soft Switching.

KEYWORDS: Pulse Width Modulation, PWM, Electromagnetic Interference, EMI, Total Harmonic Distortion, THD, Zero Current Source, ZCS, Soft Switching Five Level Inverter, S5L Inverter.

I. INTRODUCTION

Five level inverters have superior efficiency and harmonics than three level inverters. Five inverter rates have better performance at switching losses than three stage inverters Five stage inverters are therefore found at medium and high

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voltage levels, For starters, continuous power supply (UPS), motor drives, photovoltaic systems and wind turbines. The SS platform offers a better approach for the swapping errors and EMI. DC-DC converters are used in soft exchange approaches by stretching the passive or active snubber circuit for many years. The Zero Voltage Transition (ZVT) Method for switching to key switches is popular for soft switching technologies. The door voltage can be deduced to zero before the door signal is used. The technological improvements in renewable energy sources have made inverters popular in recent years. That is why in the last two decades soft switching techniques for inverters have been proposed. Passive snubber circuit is connected to the three-stage T-type inverter with passive snubber. Six diodes, two condensers and two inductions make up this snubber chain. It allows you to adjust zero voltage for key switches and to shift zero current. Once shut off, zero control (ZCS) and zero-voltage transitions (ZVS) are done with passive snubber to eliminate switching errors. The key switches have no voltage or current voltage, but a secondary DC voltage supply is required for each turn. Therefore, the expense and efficiency of the converter are that. For PWM inverters, a conventional passive snubber circuit is introduced.

For each stage of this converter a further energy recovery is necessary. InverterI is supplied with the Zero Current Transformation (ZCT) at three stages. The updated snubber circuit comprises of two L-C resonant tank operator switches. This circuit involves ZCT flipping on and off although the working system and current voltage are complex. The ZVS I inverter is collected. The snubber circuit consists of two active and resonant LC switches for each phase-bearing switch. New leg tolerance is added and the SS is provided at the Neutral Spanning Point (NPC) inverter for defect tolerance and phase legs. The resonant circuit has four condensers and an induction for every stage, making the circuit more complicated. The configuration of the 3-level T-type inverter (TCM) eliminates errors and increases efficiency. On the other side, different SS techniques can be applied to resonance inverters. This paper introduces a new five-level SS inverter. The new inverter has a large switching frequency for high power applications. This device has a snubber circuit with turn, integrated induction, six diodes and two central switch snubber capacities. No current or friction stress ZVT on and ZVS off on key switches are done. The controls are also disabled by ZCS and ZVS.

The latest snubber cell prevents the lack of switching capacity. The three-level soft swapping inverter was launched in 2011. Now we are introducing a new soft switch on five rates. The new topology circuit consists of electrical engines, photovoltaic grid-tide inverters, wind turbines and the power supply for PWM converters. It is very easy to design and thus inexpensive. It is used entirely as a soft swap and thus has very low currency losses. It provides high performance and a very high frequency of switching. The article begins with a summary of how the system functions. It then addresses advanced control processes. A variant of the S5L inverter has a passive snubber feature. A traditional 3-level soft switching inverter and a new S5L inverter evaluate the S5L inverter's advantages. The introduction of renewable energies into the energy market is intended to lead to greater power, stability and fuel quality. A five-style inverter has received greater attention for medium to high power applications, like wind turbines, PV systems and continuous supplies of power. It is an alternative to complicated five-tier topologies, and also provides better performance per production and harmonics than three-tier conversions. IGBTs therefore were used as clamping switches for inverters due to the advantages of lower drive failure.

II. EXISTING SYSTEM ANALYSIS

A. Hard and Soft Switching Inverter

High frequency of switching is a crucial factor in achieving high performance efficiency and in reducing the size of passive components. The last aspect becomes crucial in the recent times due to the growing prices of copper and iron. This together with the relative low prices of semiconductors leads to the evaluation of different topologies, with higher number of switching devices, under high switching frequency operation. Although high-power hard-wire PWM converters experience high switching errors and considerable EMI noise, using soft-switching technologies can shape the edges and voltage waveforms of standard PWM upwards and downwards. Switches and diodes may be triggered or disabled during this period under zero tension, which ensures lower switching error and greater efficiency. Over the

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years a variety of soft switch tests were carried out for three phase rectifiers or inverters with Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS).

In recent years, weak switching strategies have been adopted to improve electromagnetic compatibility, rising switching speeds and reach a high frequency of switching. A network of dc links has only passive components, but its gain is regulated by high voltage pressures and pulse variability. Better quasi-resonants, like the active resonant clamped dc-link system, reduce stress times for nominal bus voltage by incorporating clamping switches and condensers. With the help of an auxiliary device, the voltage tension of a resonant switch can be reduced at each inverter tip. At the bot of this circuit, many auxiliary switches and complex control logic are needed. They suggest a flexible model for soft swapping of inverters for both three and five phases. New resonant circuits are offered and optionally designed as an attached module. The hardwired inverter can be converted to a soft wired inverter by connecting the resonant element to a traditional inverter.

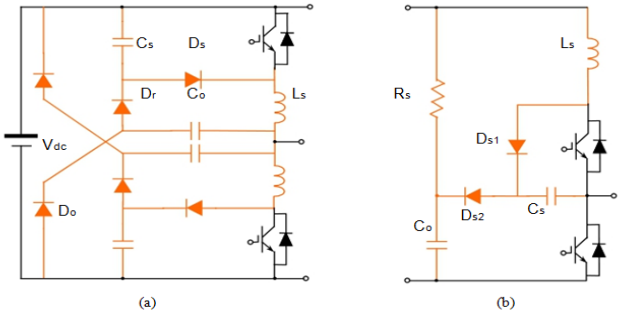

Fig.1 Passive Snubber for Inverter: (a) Lossless Snubber and (b) R-C-D Snubber

B. **Hard Switching**

This topology has been presented already in 1980 .Shows the circuitry topology of one single phase. The two 'outer' IGBTs V1 and V4 form together with their anti parallel diodes D1 and D4 a conventional 2 level PWM inverter. In combination with the IGBTs V2 and V3, and the respective diodes D2 and D3, a switchable path is set up to the centre tap of the input DC voltage Ud. With this, the terminal voltage u0 may be set to zero as well. This circuitry design is known as T-type inverter. It possesses particularly low conduction losses and therefore a high efficiency. This is based on the fact that with the T-type inverter only one power semiconductor switch conducts when V1 / D1 or V4 / D4 are turned on. On the contrary, when using a NPC I (neutral point clamped) inverter, two switches conduct in the respective time, which doubles the value of the forward voltage and so the conducting losses. Usually IGBTs are used as power semiconductor switches, recently IGBT modules.

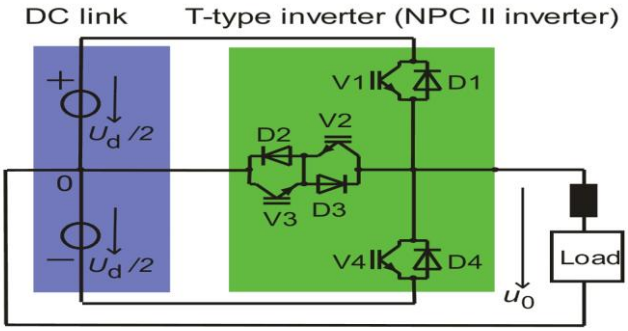

Fig.2 Single Phase Hard Switching Three-Level Inverter (NPC-II or T-Type)

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C. **Soft Switching**

Three-level inverters are used as grids in feed inverter in PV plants or as active power line filters in electric drive systems. So called Hard Switching Topologies have been implemented up-to-date. The now available' Easy Switching Three Level Inverter ' promises minimized switching errors and greater efficiency. This topology has been presented the circuitry topology of one single phase. The two 'outer' IGBTs V1 and V4 form together with their anti parallel diodes D1 and D4 a conventional 2 level PWM inverter. In combination with the IGBTs V2 and V3, and the respective diodes D2 and D3, a switchable path is set up to the centre tap of the input DC voltage Ud. With this, the terminal voltage u0 may be set to zero as well.

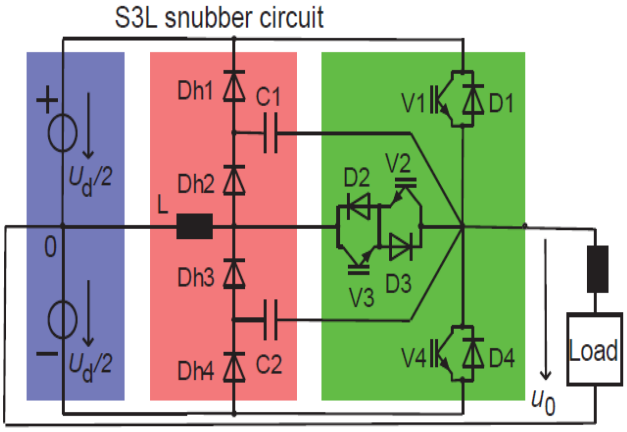

Fig.3 Soft switching three-level (S3L) inverter

This circuitry design is known as T-type inverter. It possesses particularly low conduction losses and therefore a high efficiency. This is based on the fact that with the T-type inverter only one power semiconductor switch conducts when V1 / D1 or V4 / D4 are turned on. On the contrary, when using a NPC I (neutral point clamped) inverter, two switches conduct in the respective time, which doubles the value of the forward voltage and so the conducting losses. Usually IGBTs are used as power semiconductor switches, recently IGBT modules. In addition to the conducting losses, the switching losses have to be taken into account. Switching errors arise at IGBT turn-on or turn-off as high current and low values occur simultaneously. This is known as 'hard switching.' An example of the uCE(t) collector/emitter voltage and the corresponding iC(t) collector current when the IGBT is triggered. It results in measured values of the turn-on energy Eon of 4,5 mJ.

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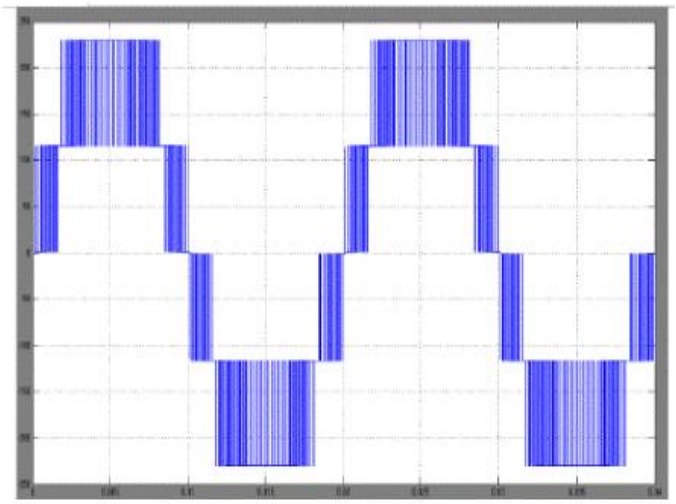

Fig.4 Output Voltage Waveform Of Three-Level

A simple additional modification of the S3L inverter reduces the described du/dt values when turning on the 'outer' IGBTs and with this the interference voltage. To achieve this, the time for turning on is lengthened by a reduction of the rate of rise of the gate-emitter-voltage. The simplest solution for this is the implementation of a gate-series resistor which is only active during turn on. In hard switching inverters this solution causes a dramatic increase of the switching losses when turning on the IGBTs which is severely disadvantageous. In contrast for S3L inverters, the rate of rise of the current when turning on the IGBTs is limited by the inductance L. Because of the slow increase of the collector current and the slow decrease of the collector-emitter-voltage, high values of current and voltage at the same time are comparatively limited. Compared to the original S3L inverter, the switching losses during turn on are increased slightly, But still significantly lower than the heavy inverter flipping. This topology is known as the ' Super Soft Flipping Three Rate (SS3L) Inverter.

III. PROPOSED SYSTEM ANALYSIS

This work provides a thorough study and critical assessment of the AC inverters. While various techniques have been claimed in the field of soft-switching inverters to improve the performance of the inverter compared with traditional hard-switching inverters, the effects of soft-switching inverters are not thoroughly investigated. The experimental measurements on the dynamometer accurately describe the output of soft-changing inverters in terms of loss reduction, EMI, Total harmonic distortion (THD) and compounds control. A analysis is carried out of the harmonic distortion induced by short pulses and the space vector-modulation method is suggested to minimize this effect. Next, by way of an efficiency competition between various soft-switching inverters using analytical measurements, the study shows the results of auxiliary circuit operation and the control of loss reduction. The three forms of switching device inverters that conduct Zero Voltage Transition (ZVT) or Null Current Transition (ZCT) operation are defined in order to achieve high efficiency operations. High frequency of switching is a key factor for the UPS in achieving high performance and in rising passive part capacity.

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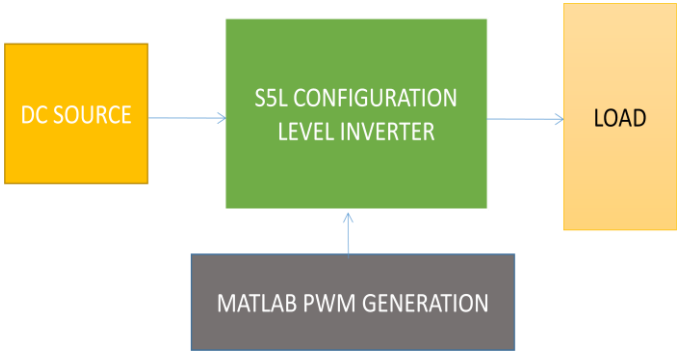

Fig.5 Functional Block Diagram

The last aspect becomes crucial in the recent times due to the growing prices of copper and iron. This together with the relative low prices of semiconductors leads to the evaluation of different topologies, with higher number of switching devices, under high switching frequency operation. Although switching PWM converters with a high power have large switching losses and severe EMI tone, a soft switching techniques that shape up and down the edges of traditional PWM switching currents and voltage waveforms are the effective approach to fix those problems. Switches and diodes may therefore be enabled or disabled in zero current conditions, which implies minimal loss of switching and increased efficiency. During the past several years many experiments have been conducted on either Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS). A simple additional modification of the S5L inverter reduces the described du/dt values when turning on the 'outer' IGBTs and with this the interference voltage.

- To achieve this, the time for turning on is lengthened by a reduction of the rate of rise of the gate-emitter-voltage. The simplest solution for this is the implementation of a gate-series resistor which is only active during turn on.
- In hard switching inverters this solution causes a dramatic increase of the switching losses when turning on the IGBTs which is severely disadvantageous. In contrast for S5L inverters.
- The rate of current change when IGBTs are switched on is constrained by inductance L. As the collector current rises gradually and the collector emitter voltage decreases slowly, high voltage and current values are at the same time relative reduced.
- The switching losses at turn-on compared to the original S5L inverter are slightly higher but still significantly lower than those of the hard switching inverter.

- C1, C2 =0.1 µF
- Udc=450 V
- fs=14 kHz
- Ls =40 µH
- R=55 ohm

The multi-level inverter is a dc source that supplies electricity to every H-bridge inverter. The control unit includes the modulations used to monitor the different switching sequences of various inverter switches. The load can be R-L or AC generators.

(i) DC Sources

Photovoltaic devices, fuel cells, batteries or correction circuits can be the DC power source (Vdc). The different fuel cells-fuel cell hydrogen-oxygen, lithium-ion source.

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(ii) S5L Configuration Inverter

A single h-bridge converter and a cable terminal voltages of various level converters are attached to each DC source in a series, which may produce three separate voltage outputs + Vdc, -vdc, and zero. The voltage waveform AC feature is the sum of the various converter outputs. Cascaded multilevel inverters have a special and appealing topology like structural simplicity, use of fewer materials, etc. The principal benefit of these inverters is that they can achieve extremely low output voltages for distortion and lower voltage (dv / dt). We can run at a lower switching level. Cascaded multi-level inverter is made up of H-bridge chain (Full Bridge).

(iii) Load

The cascaded multi-level inverter effectively eliminates harmonic input currents and regenerative activities on the main side of the transformer without problems. A second dc voltage detector (SMV) is developed to get dc voltages in Cascaded Cascaded (CHB) Static Synchronous Compenser (STATCOM) multilevel Cascaded Cascaded (CHB). Through inductor operation, the specifications for electric vehicles (EV) and hybrid electric vehicles (HEV) are added. The loads we use are heavy.

(iv) PWM

The main aim of the technique of the multilevel modulation inverter is the synthesis of signal voltage as similar to the sinusoidal process as possible. A variety of modulation approaches were developed to reduce harmonic losses and compatible losses. For inverters, the multi-level modulation approaches can be classified by size. High-frequency solutions have many semi-conductor control switches in a crucial performance tension cycle. The output voltage of the inverter can also be regulated by the inverter switch. The most effective way is to monitor the variation of the inverter pulse width. The inverter has a fixed input dc voltage and generates a controlled AC voltage, adjusting the inverter modules' on and off cycles. This is the best way to control present voltage and pulse width (PWM) modulation.

IV. PROPOSED CIRCUIT

A. Soft Switching Five Level Inverter With Passive Snubber Circuit

The goal of the "Soft Switching Five Level Circuit Inverter" presented here is to indicate an extremely simple circuit which,, compared to a hard switching three level inverter, indicates only a small additional outlay of exclusively passive components, which in principle avoids all switching losses and guarantees an effective di/dt limitation, as well as a du/d .

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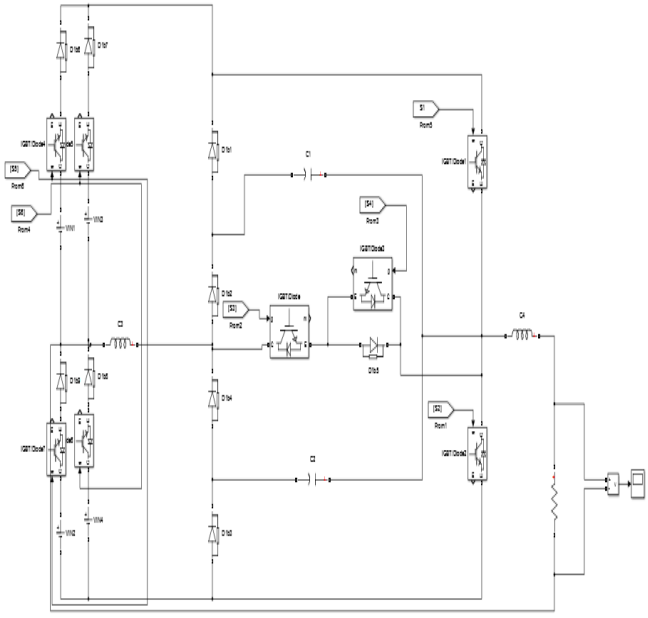

Fig.6 Soft Switching Five -Level Inverter

B. **Working of Proposed Model**

This figure Provide a schematic circuit diagram for the "Passive Snubber Circuit Soft Switching Five Stage Inverter." The basis is the five-level inverter circuit with heavy switching,, consisting of the 8 IGBT's S1 to S8 has terminal voltages V1 to V8 and the 8 diodes D1 to D8. As is known, the output negative terminal or with the central neutral tap of the input direct voltage Ud. A change between these terminals can be connected alternatively with the positive terminal, with the 5 switching states should be designated as commutation. This five level inverter, consisting of the 8 IGBT's S1 to S8 and the 8 diodes D1 to D8, snubber circuit added to it, consisting of the inductor L, the two capacitors C1and C2.

C. **Operating Principle**

- Five voltage output rates are produced as follows (+ V, +V/2, 0, -V/2, -V).
- S1 is switched on at the positive half period to produce a voltage point Vo=+V. The electricity is supplied by the C2 condenser and the voltage is+ Vdc. S6 is activated and the load terminal voltage is+ Vdc.
- S2 is enabled to produce the voltage level Vo=+V/2. The condenser C2 provides energy. The overvoltage is+ Vdc/2. S6 is switched on and the load terminal voltage is+ Vdc/2.
- The voltage level Vo= 0, S5 and S6 are disabled.
- The negative half loop is triggered to create a Vo=-V/2, S4 voltage level. The condenser C1 is supplied with electricity, and the voltage is –Vdc/2. S5 is switched on and the voltage of the load terminals is –Vdc/2.5) S3 is turned on to produce the voltage point Vo =-V. Power is supplied by the C1 condenser. The uncertainty is -Vdc. S5 is allowed, and the load terminal voltage is -Vdc.
- The frequency switches from 0 to 1 or 1 to 0 at the same moment as the S7 and S8 are on or off. The condenser C2 is filled for a positive half cycle, and the condenser C1 for a negative half cycle.

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V. RESULTS AND DISCUSSIONS

The purpose of the "Soft Switching Five Level Circuit Inverter" provided here is to demonstrate the very basic circuit, compared to a hard switching three level inverter, indicates only a small additional outlay of exclusively passive components, which in principle avoids all switching losses and guarantees an effective di/dt limitation, as well as a du/dt limitation. The soft 5-level inverter with passive snubber has a waveform output voltage of 5 levels + V,+V / 2,0-V ,- V/2.

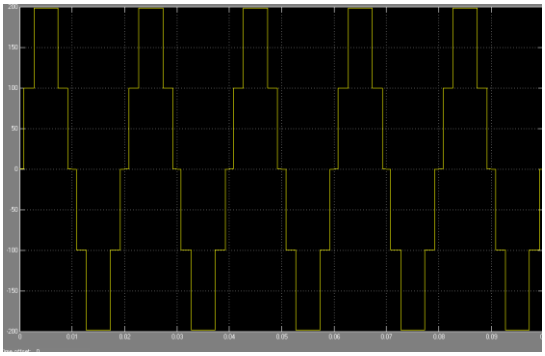

Fig.7 Output load voltage wave form

SOFT SWITCHING FIVE-LEVEL INVERTER WITH PASSIVE SNUBBER CIRCUIT

- A simple additional modification of the S5L inverter reduces the described du/dt values when turning on the 'outer' IGBTs and with this the interference voltage.
- To achieve this, the time for turning on is lengthened by a reduction of the rate of rise of the gate-emitter-voltage. The simplest solution for this is the implementation of a gate-series resistor which is only active during turn on.
- In hard switching inverters this solution causes a dramatic increase of the switching losses when turning on the IGBTs which is severely disadvantageous. In contrast for S5L inverters.
- The rate of rise of the current when turning on the IGBTs is limited by the inductance L. Because of the slow increase of the collector current and the slow decrease of the collector-emitter-voltage, high values of current and voltage at the same time are comparatively limited.
- Compared to the original S5L inverter, the switching losses during turn on are increased slightly, But still substantially reduced compared with the heavy inverter flipping.

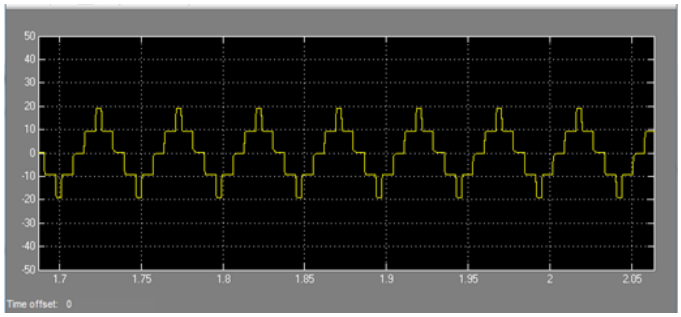

Fig.8 Output Voltage - Waveform of S5L Inverter

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The S5L inverter shows only slightly lower interference voltage compared to the S3L inverter. This is based on the fact of the remaining existence of high du/dt values in S5L. These are advantageously suppressed in the S5L topology.

PULSE WAVEFORM

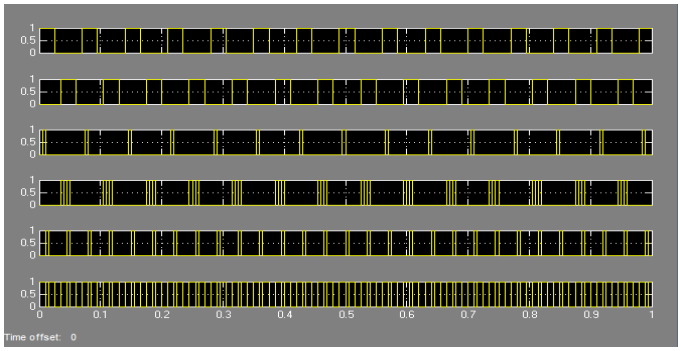

Fig.9 Output Pulse Waveform of S5L Inverter

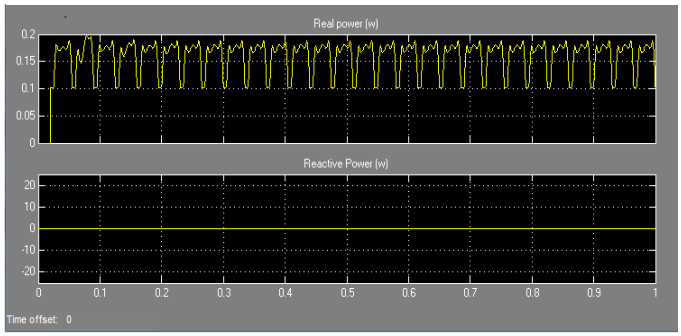

Fig.10 Real power R load

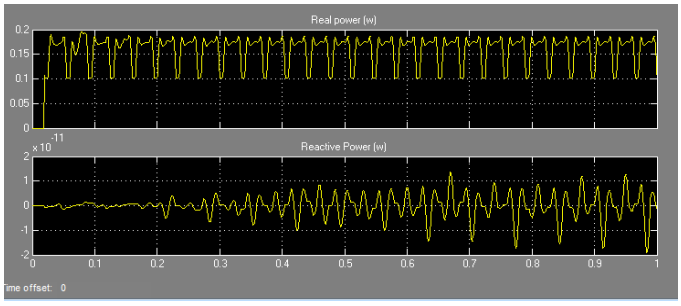

Fig.11 Real Reactive Power RL-load

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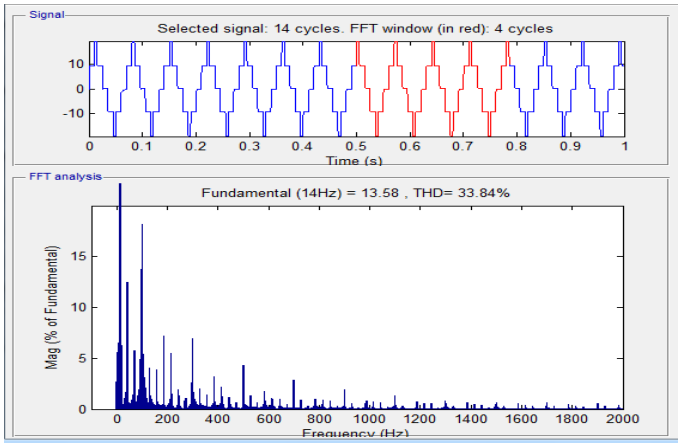

Fig.12 THD (Total Harmonic Distortion)

As expected the soft switching topologies provide better efficiency compared to the S3L inverter. The advantages in EMI reduction of S5L might cause a slight reduction in efficiency.

VI. CONCLUSION AND FUTURE SCOPE

This post introduces a new quick switch Five stage inverter. Most of them operate with soft switching, and during the shut off, Zero Voltage Transition (ZVT) technology was obtained for the main switches. The main switches have no voltage or current tension. Furthermore, optimum output at high frequencies can be accomplished with reduced power losses. Harmonic content relative to current output and EMI. Ultimately, this new soft switching inverter has benefits as compared to the other three levels and the 5 hardwired inverter, such as a simple structure, reduced harmonic current volatility at the output current and EMI. ZCS and ZVS methods are accomplished by passive snubber for main switches, which ensures there is a stress on switches in the proposed model. EMI elimination also coincides with lowered di / dt and dv / dt. Although high frequency oscillations cause additional power losses and harmonic effect production, oscillations are eliminated efficiently by the proposed RC circuit. The passive snubber avoids nuanced techniques of power. This paper uses the conventional PWM inverter control system. The soft switching S5L inverter provides significantly higher efficiency compared to the soft switching S3L inverter. Regarding the interference voltage, S5L inverters have only a small benefit compared to S3L inverters, whereas the S5L is advantageous. Especially when operated with variable switching frequencies, the S5L inverter is the most attractive solution. This paper discussed a new S5L approach for grid-connected single phase converters. To achieve the minimum number of commutations to maximize efficiency, the PWM technique was used. The topology uses the dc's midpoint voltage to provide two additional voltage ranges, reduced switching power losses and EMI. The midpoint voltage equilibrium was taken into account and an effective regulation was established that was able to offset the eventual system asymmetries. Multilevel simulation inverter is done by program MATLAB / SIMULINK. We can use the same design with lower THD to enable high-level Multi-Inverter with less switches.

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