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Literature Survey on Video Encoding Using Motion Estimation Methods

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ABSTRACT: One of the most efficient video compression techniques is Motion Estimation (ME). MPEG1, MPEG4 AND H.261, H.264 comprises the various standards for video compression. Motion Estimation Techniques drastically increases the compression due to which energy reduction is achieved within residual frames of videos. This paper summarizes the literature review on various motion estimation methods mainly focusing on BME (Block Motion Estimation). This paper discusses various motion estimation methods with their applications and limitations. Various Algorithms like (ITSS) Improved Three Step Search, (FTS) Flexible Triangle Search, (4SS) Four Step Search, (DS) Diamond Search, (FSBME) Full Search Block Motion Estimation, (MFSBME) Modified Full Search Block Motion Estimation, (LP-MFSBME) Low Power Modified Full Search Block Motion Estimation are analyzed and their performance characteristics are estimated.

KEYWORDS: ME(Motion Estimation); MV(Motion Vector); Video Compression; SAD(Sum of Absolute Difference).

I. INTRODUCTION

In order to increase efficiency Block Matching Motion Estimation Technique is used for encoding the sequence of image frames through motion-compensation. and a systolic array processor are included in the proposed model which can reduce the pin counts while performing parallel processing , also operates in real time video conference applications and it is a modular and simple design. (BMA)Block Matching Algorithm technique can be used to estimate the motion by a block-by-block basis. MAD(Mean of Absolute Difference) value is calculated by comparing a block of pixels in the current frame with the respective pixels block in the reference frame. This calculation is performed inside the search area and the (MV)Motion Vector is calculated from the block having the least MAD(Mean of Absolute Difference) and is considered as the best matched block [15].
Researchers have found several algorithms for motion estimation. An Improved Three Step Search(ITSS) motion estimation algorithm has been proposed which is efficient in performance compared to the previous (TSS) Three Step Search and (NTSS)New Three Step Search algorithms. ITSS comprises an in-built dynamic and flexible VLSI architecture. Low bit rate video coding like H.261 standard frequently employs this ITSS method.

VLSI tree processor and FPGA addressing circuits are implemented in ITSS Algorithm and this leads to reduced gate count. Several previous Three Step Search algorithms(TSS, NTSS) can also be implemented by ITSS motion estimation technique due to the flexibility in its architecture[14].

Another advanced Three Step Search Algorithm FTSS(Fast Three Step Search) Algorithm decreases the number of search points involved in motion estimation method. FTSS includes three processing elements and makes use of intelligent data arrangement and memory configuration. In this algorithm, current Motion Vector is calculated from the

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directional information of the previous Motion Vector. FTSS provides enhanced performance than the standard TSS method by reducing the number of search points by utilizing the directional information[13].

Motion Estimation can also be performed by using Fast Search and Full Search Algorithms. Current frame and reference frame are used for performing Block Matching based full search and the block with largest similarity i.e. minimum SSD value is chosen and Motion Vector is estimated by finding the difference between the two blocks. Fast Search algorithms are used more compared to the Full Search algorithms thereby reducing complex computations. Special patterns are employed in Fast Search Algorithms for motion estimation by reducing the number of checking or search points such as Hexagonal pattern and Diamond pattern. One such method is DS(Diamond Search) method and it employs two types of search pattern algorithms such as SDSP(Small Diamond Search Pattern) or LDSP(Large Diamond Search Pattern) thus reducing the number of search points further based on SAD(Sum of Absolute Difference) values obtained from the previous step. This most popular technique is named as Motion Vector Field Adaptive Search technique (MVFAST). Fast Search techniques also employs SKIP Mode to differentiate some types of blocks from other blocks and gives highest priority to the SKIP Mode thereby eliminating complex ME calculations. SKIP mode does not require motion search is considered to be less complex [12].

Another ME algorithm uses a flexible triangle to find the best block between reference and current frames whose direction and size of the triangle can be altered to reduce the number of ME calculations through various operations like translation, reflection, expansion , contraction . This method is called as FTS(Flexible Triangle Search) algorithm. To perform fine searches different orientation triangles are used which is used to change the size, location and direction of the search triangle. Power consumption is reduced as this algorithm provides more efficiency in achieving higher frame rates [11].

II. DISCUSSION ABOUT REVIEW PAPERS

This section briefs the working of Video Compression systems using various Full Search and Block based Motion Estimation techniques.
Fig 1. shows the Motion Estimation method along with motion vector.

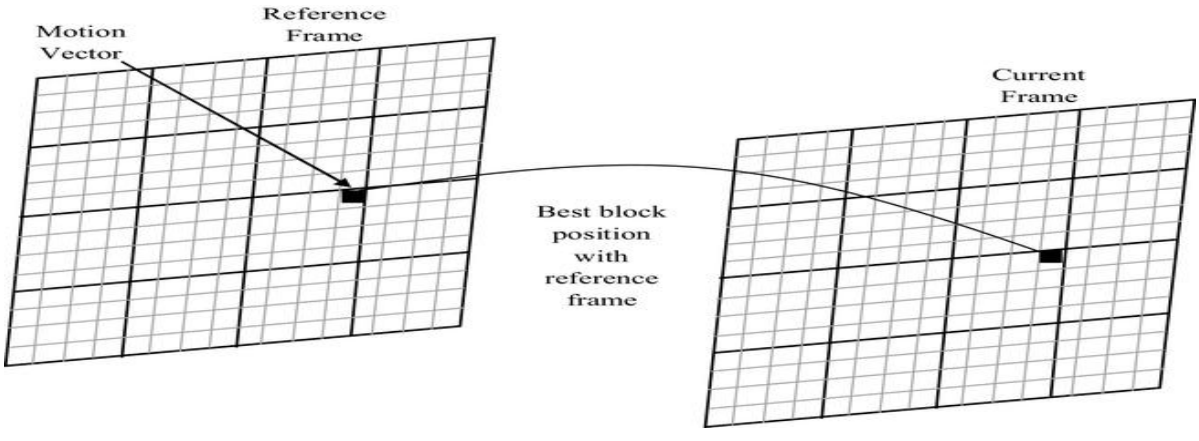

Fig. 1 Motion estimation Technique and Motion vector determination

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Paper [10] describes Modified Full Search Block Estimation Algorithm(MFSBMA) is more efficient compared to the Full Search Block Estimation Algorithm(FSBMA) but it maintains the same Peak Signal To Noise Ratio(PSNR) as that of FSBMA but SAD calculations are minimized by skipping the current background block SAD calculations and computing the SAD only for the current foreground block. FSBMA method implements Background elimination technique which uses threshold logic of Background Frame(BF) to find if a pixel is background or foreground pixel. When the BF pixel value is higher than the threshold value then the Current Frame(CF) pixel is a foreground pixel whereas when the BF pixel value is lower than the threshold value then the CF pixel is called a background pixel and its value is set as 0. SAD calculations are thereby reduced by calculating the Foreground pixels motion vectors.
In Paper[9], Parallel Bank Architecture is incorporated to provide maximum hardware utilization by providing maximum throughput and reduced latency. This method employs VLSI architecture which contains four main parts like computation core, address generator, off-chip memory and on-chip buffer. A Finite State Machine(Moore Model FSM) controls the nine processors running in parallel.
Four states are present in the major module of the FSM module namely SAD Generator State, Loader State, Comparator States and Idle State and all the modules are controlled by Comparator States. Higher speed is obtained from parallel processing and highly scalable VLSI architecture.
In Paper [8], FSBM(Full State Block Motion Estimation) Architecture is enhanced by employing Conservative Approximation technique. This conservative technique maintains high throughput and reduces the unnecessary SAD calculations and thereby reducing the power consumption by a factor of 2. This method determines the value of distortion conservative approximate for each macro block prior to calculating the exact distortion. When the conservative estimate of distortion is larger than the previously determined minimum Exact distortion value then the exact distortion calculation can be skipped. FSBM Conservative Approximation method reduces the power consumption in motion estimation without major effects in accuracy measure.
Another Paper [7] employs Global Elimination(GE) technique also known as Pixel Averaging Algorithm. There are two stages in GE algorithm , where the unnecessary SAD computations are skipped by comparing SSAD(Sub-Sample SAD) with minimum SAD in the first stage also known as pre-processing stage. SAD Calculations will be computed at random candidate macroblock positions which are matched at the second stage. A 16x16 macro block partitions and the 8x8 macro block partitions and various sub partitions are shown in Fig 2. and Fig 3.

The main limitation of Global Elimination Algorithm is that the sizes and shapes of the blocks used are fixed for computing Sub-Sampled SAD calculations in the pre-processing stage. By using the blocks which are capable of changing their block sizes dynamically based on macro block features the limitation of GE Algorithm can be minimized. Adaptive (GE)Global Elimination Algorithm increases the throughput by 50% and reduces the computations by 60%. Complex computations are decreased since SSAD(Sub-Sampled SAD) is used over the complete SAD for computing the best matched block between reference block and current macro block.

In the second stage Full Search method is employed to select top 'N' macro blocks and motion vector is found only for these macro block candidates. Each Macro block pixel variance is determined in order to find the correct amount of partitioning in adaptive GE algorithm. Partitioning size plays a major role where small count of partitions are used for Macro blocks with lower variance and larger count of partitions are used for Macro blocks with larger variance. SAD calculations have been reduced drastically by employing Adaptive Global Elimination Technique.

In Paper[6], Quarter pel FSBME(full search block motion estimation) was introduced which is a novel searching algorithm. All motion vectors(41) are computed in parallel for all the sub-blocks. This paper describes novel features like variable adaptive block sizes, Quarter sample accuracy, numerous reference frames for computing motion estimation. Five reference frames can be processed in parallel by using this proposed technique. RAMs with single port block are used in search window and its size ranges from Quarter pel(92x92) pixels. In 16x16 blocks, the motion vector value is between -3.75 to +4.00. Comparing units , 8 processing units , Shift Registers and AG(Address

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Generator) is also included in this novel architecture. This design is parallel and pipelined in nature for real time processing of Common Intermediate Format(CIF) Images. This design includes 41 PISO(Parallel In Serial Out) Shift Registers. The SAD values for each Macro Block with different size are calculated by each PISO and these values are fetched to the comparing unit to obtain the output which in turn generates the best motion vector.

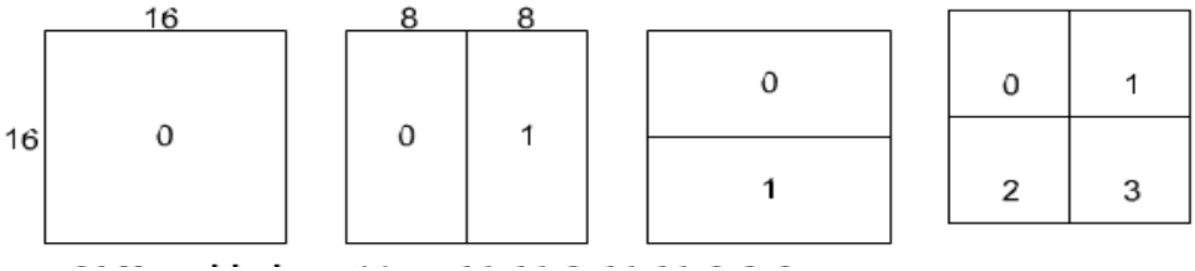

Fig. 2 16x16,8x16,16x8,8x8 Macro Block Partitions

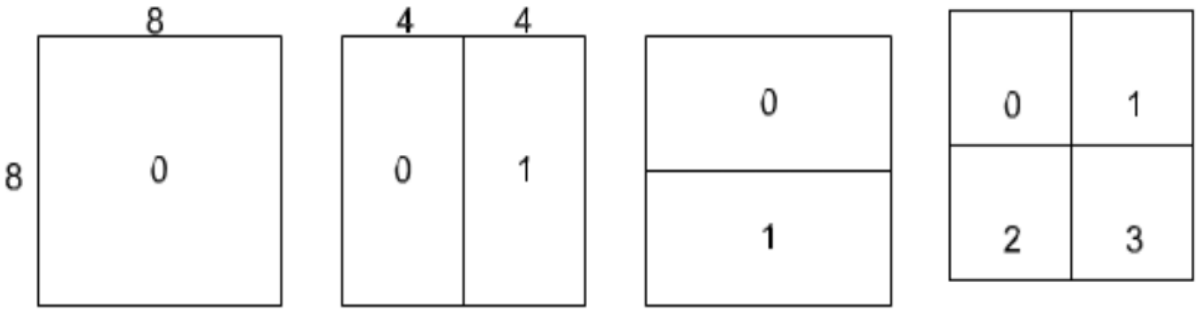

Fig. 3 8x8, 4x8,8x4,4x4 Macro Block Sub Partitions

In Paper [5], Effective video frames compression can be achieved by reducing the data redundancies between successive video frames. There are two major types of redundancies namely Inter-Frame or Temporal Redundancy which occurs due to pixels correlation between successive video frames and Intra-Frame or Spatial Redundancy which takes place in a video sequence having high values of correlated pixels.
In Order to reduce Spatial Redundancy various techniques are employed like Discrete Wavelet Transform(DWT), Haar Wavelet Transform(HWT) and Discrete Cosine Transform(DCT) whereas the Temporal Redundancy is decreased by using Motion Estimation Methods.
This Paper introduces Hexagon Based Search(HBS) to determine Motion Vector and makes use of a threshold value that varies dynamically and is not fixed. Two methods used in HBS such as Small Hexagonal Search Pattern(SHSP) and Large Hexagonal Search Pattern(LHSP) are used for motion estimation.

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In Paper [4], high quality of encoding is emphasized and the necessity for variable block sizes and its motion estimation computation are discussed. Considering rate distortion, performance efficiency can be achieved by employing Variable Block Size Motion Compensated Prediction(MCP) compared to the other conventional technique like Motion Compensated Prediction(MCP) with fixed block size.

The different block sizes comprises 4x4, 4x8, 8x4, 8x8, 8x16, 16x8, 16x16 and hence leads to 41 different possible combination of block sizes. In all the 41 different combinations of 16x16 macro block, many overlapping macro blocks exist in the search area and it depends on the memory size. Prior to computing SAD values, different macro blocks can be read by using various scan patterns such as raster scan, z scan or spiral scan and meander scan.

Raster scan patterns are frequently employed in Variable Block Size Motion Estimation technique which has the ability to read 1, 4 or 16 pixels simultaneously and these pixel values are transferred to the PE(Processing Elements) to compute SAD values. Z pattern of scanning is used in this paper than the raster scan pattern.

Current Macro Block pixels and 17 pixels which are candidate Macro Blocks are accessed by using 16-pixel z-pattern scan to determine the 41 different combinations in a 16x16 block. This method is carried out with decreased clock cycles (16 are used). By repeating the process 17 times , all the combinations of candidate block are available in 272 cycles from which the best match and motion vector are determined.

In Paper [3], a large scale implementation (1-D One Dimensional Implementation) was designed for full search called as Full Search Variable Block Size Motion Estimation(FSVBSME). Total of 41 MVs'(Motion Vectors) for sub-blocks are processed in the equal number of clock cycles in this 1-D technique and finally one Motion vector alone is computed in the conventional One Dimensional 1-D method.

This design uses computationally less complex devices like latches and multiplexers. The proposed design computes 16 SAD values of 4x4 sized blocks and these values are reused in calculation of SAD values of larger sized blocks. In this method Current Macro Block data and Search Range(Reference Block) data are arranged in dual raster pattern of scanning. Partial SAD values are shuffled and combined inside each Processing Element which comprises the main key aspect of the paper. Based on this mechanism, larger block SAD values can be estimated from the 4x4 block SAD values derived from the previous step without the need for the entire SAD computations to be performed.

Another paper [2], emphasizes the Block Motion Estimation using Enhanced Diamond Search(EDS) method. This proposed design contains two types of search like Small Cross Diamond Pattern(SCDP) and Large Cross Diamond Pattern(LCDP). SCDP includes 4 search points having ±1distance of pixels whereas LCDP includes 5 search points having ±2distance of pixels.

PSNR is significantly increased by using EDS approach and it also has only minimum number of search points. Field Programmable Gate Array(FPGA) device having fixed block size is used to implement EDS algorithm.
In Paper [1] Adaptive Rood Pattern Search(ARPS) was devised which is a new block matching method. Refined Local Search and Initial Search are the two search stages incorporated in ARPS technique. In initial search ARD pattern is employed which is symmetrical and is widespread in both horizontal direction and vertical direction. During the initial search 6 search points are present and it reduces to 5 points during refinement process which also includes the Motion Vector. Adaptive Rood Pattern Search method provides higher performance compared to Diamond search.

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III. CONCLUSION

Full Search and Modified Full Search Algorithms are considered to be more efficient than other conventional methods. Results with efficiency and minimum number of SAD calculations are also achieved using other algorithms like TSS, EDS, FTSS etc,. Good results are obtained in Enhanced Diamond search when compared to normal Diamond Search Algorithm. High throughput and speed can be achieved through reduced search points. The most challenging factor for various motion estimation techniques in Video Compression is to achieve minimum search points and high accuracy incorporating different sizes of macro blocks.

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