International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE)

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 8, August 2020 ||

Study of Various Design & Performance aspects of MOSFETs at Nanometer Technology

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ABSTRACT: As per the International Technology Roadmap for Semiconductors (ITRS) each lower node is 0.7 times the previous technology making chip faster by 17% every year. Scaling down of CMOS technologies to 22nm has significant challenges in design. CMOS technology dimensions are being aggressively scaled to reach a plateau where device performance must be assessed against fundamental limits. Conventional scaling of gate oxide thickness, source/drain extension (SDE), junction depths, gate lengths & alternative materials and structure have enabled MOS gate dimensions to be reduced from 10um in the 1970's to a present day size of 20nm. To enable transistor scaling into the 21stcentury, new solutions such as high dielectric constant materials and alternative structure and alternative to gate material. Also the traditional SiO2 gate dielectrics will reach fundamental leakage limits, due to tunneling, for an effective electrical thickness below 2.3 nm. There are Some solutions include modifications on the existing structures and technologies with a hope of extending their scalability. Other solutions involve using new materials and technologies to replace the existing silicon MOSFETs. Researchers currently focused on identifying alternatives which would enable continued improvement in the performance of electronics systems are high dielectric constant (High–K), metal gate electrode, double gate FET. The nanoscale devices are showing low short channel effects (SCEs) compared to other devices. The Double Gate MOSFET & alternative material like CNT (Carbon Nanotube) has the potential to overcome the short channel effect problem..

KEYWORDS: ITRS, Short Channel Effect (SCE), High-K Double Gate MOSFET & Carbon Nanotubes (CNT).

I.INTRODUCTION

Since the fabrication of MOSFET, the minimum channel length has been shrinking continuously. The motivation behind this decrease has been an increasing interest in high speed devices and in very large scale integrated circuits. Scaling the CMOS technology into nanometer regime require an innovative approach in overcoming a number of short channel effect (SCE). It is expected that the current CMOS technology, conventional planer bulk transistor, will be difficult to scale effectively, even with the utilization of high-k gate dielectrics, metal electrodes, strained silicon and other new materials being considered. Multi Gate Field Effect Transistor (MUGFET) is thought to be the leading new transistor technology which will take over as the leading workhorse in digital electronics. According to the projection of the 2008 International Technology Roadmap for Semiconductor, devices with gate lengths down to 10 nm can be expected in 2019. The MOSFET channel length is scaled down, the vertical dimensions, i.e. the gate oxide thickness and the source-drain junction depth must be scaled down as well, in order to keep the short-channel effects (SCE) within acceptable limits. Ideal scaling is, for several reasons, not always possible and SCE can be worse in the scaled-down technology. One of the main SCE is the reduction in the threshold voltage with decreasing channel length. Threshold voltage reduction causes the off-current of an MOS transistor to increase significantly, thus giving rise to higher static power dissipation. To comply with the requirements of technology scaling, devices have been designed with more complex doping profiles in an effort to maintain long channel behaviour at short channel lengths.

DG Structure is comprised of a conducting channel (usually undoped), surrounded by gate electrodes on either side. This ensures that no part of the channel is far away from a gate electrode. The Double- Gate MOSFET (DGMOSFET) structure minimizes short-channel effects in order to allow a more aggressive device downscaling, and numerical simulations have shown that it can be scalable down to 10 nm gate length. In ultimately scaled technology, CMOS circuit leakage power would be significantly reduced by DG devices.

Considering power and performance trade-off in circuit design, the DG inverter could offer lower leakage power or faster performance due to near-ideal slope factor (S) and lower Drain-Induced Barrier Lowering (DIBL).

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To overcome SCE and scaling down problems that have occurred, the designers are now searching for a more efficient transistor design to satisfy the same circuit characteristics as the MOSFETs. Engineers have been experimenting with different types of material. One of the materials is carbon-based. Carbon nanotubes are described as a sheet of graphene rolled up into a cylindrical shape. This rolled up sheet of graphene can take on two characteristics depending upon the way the sheet is rolled-up. These two characteristics are metal and semiconductor. The semiconductor-type material is what is needed to develop a carbon-nanotubes field-effect transistor (CNFET).Since the discovery of carbon nanotubes in the early 1990s [1], the field has witnessed an immense growth. Due to the small diameter (1 nm), nanotubes are ideal candidates to study one-dimensional (1-D) electrical transport phenomena, even at room temperature. In recent years, intensive research on single-walled Carbon Nanotube (SWNT)-based field-effect transistors (FETs) has revealed the excellent properties of these novel materials, including ballistic transport and high chemical stability and robustness. Nevertheless, it remains an open question as to what the ultimate Nanotube FETs may be in structure and performance and how to achieve the optimum ON current and high ON/OFF current ratios, steep switching, and highly scaled gate dielectrics and channels.

The most promising technology today for the control of short-channel effects is multi-gate MOSFETs. While it is not a new idea and originates from early 60s, the need for the suppression of SCEs towards the continuous scaling of electronic devices brought them up to the surface the last years [2]. The adjacent figure shows cross sections of different types of multi-gate devices as have been proposed lately. The multiple advantages of multi-gate MOSFETs can be summarized in the following points[2].

• Electrostatic shielding of the channel from parasitic electric fields originating from the gates and the drain. The mobility is increasing while the transverse electric fields cannot penetrate inside the channel.

• Better control of the channel because of the gates coupling. Better Subthreshold slope and smaller DIBL parameter are obtained.

• Two or more inversion volumes are created, that result in higher on-current and faster carrier transport within the tiny volume of the channel film.

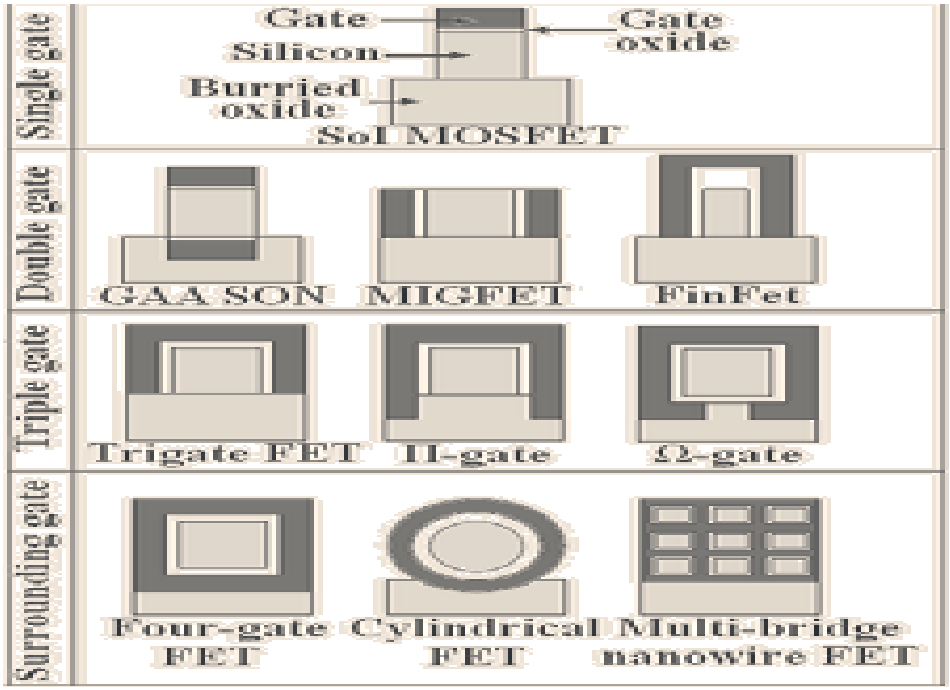

Fig. 1 Multiple Gate structures Proposed for design

II.LITERATURE SURVEY

M. Mustafa et al [4] the threshold voltage sensitivity to metal gate work-function for n-channel double gate fin field-effect transistor (FinFET) structures and evaluates the short channel performance of the device using threshold voltage dependence on metal gate work-function analysis. The study for a double gate n-channel n-FinFET with parameters as per the projection report of ITRS-2011 for low standby power (LSTP) 20 nm gate length technology node. Varying the

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device gate work-function improves the DIBL, SS, Off-current, On/Off current ratio, but causes a reduction in device On-current.

Table . 1 Device parameters undertaken for the simulation study

Device parameters	Values undertaken
Physical Gate Length (Lg)	20 nm
Equivalent Oxide Thickness (EOT or tox1, tox2)	1 nm
Vdd (Power Supply Voltage)	0.86
Fin width (Wch)	12.5 nm
Channel Doping	4x1018cm-3
Drain/Source Doping	1x1021cm-3
Extension length to Source /Drain (Ls & Ld)	30nm

M. Mustafa et al [1] also suggested the Advanced DG MOSFET structure to mitigate SCE.

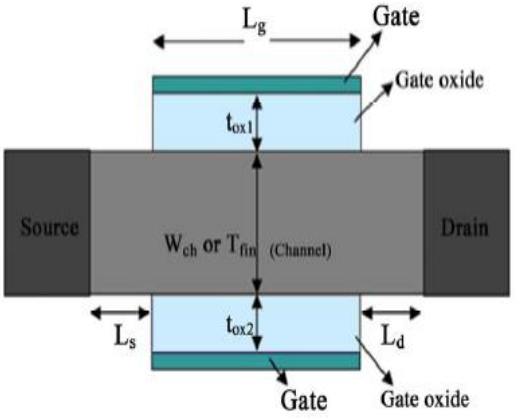

Fig.2 Two Dimensional DG FinFET Structure

S. Panigrahy & P. k. Sahu [5] describes the shrinking transistors is able to achieve better electronic performance by putting more of them on to a chip. The nanoscale devices are showing low short channel effects (SCEs) compared to other devices. The Double Gate MOSFET has the potential to overcome the short channel effect problem. A one dimensional (1-D) analytical solution is derived for an lightly-doped double-gate MOSFET. A threshold voltage is derived which shows that it is fully dependent on the gate work function.

The channel doping concentration (1×1016 cm-3). The doping concentration of source/drain region is kept at 1×1020cm-3. Oxide (SiO2) thickness =2nm. Metal Gate has been used.

Table .2 Values of device parameters according to different work functions

Work function	***DIBL***	***Leakage current***	***Threshold Voltage***	***Id_{max}***
4.8 ev	16.8 mv/v	0.9 nA/um	0.45V	1.1 mA
4.6 ev	45.2 mv/v	3.0 uA/um	0.25V	1.7 mA
4.4 ev	79.2 mv/v	4.5 uA/um	0.14V	2.4 mA

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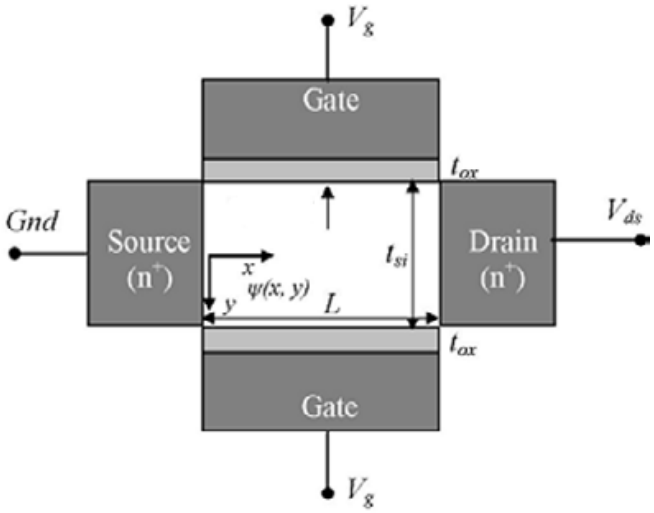

Fig. 1 Schematic structure of the undoped-body symmetric DG N-MOSFET

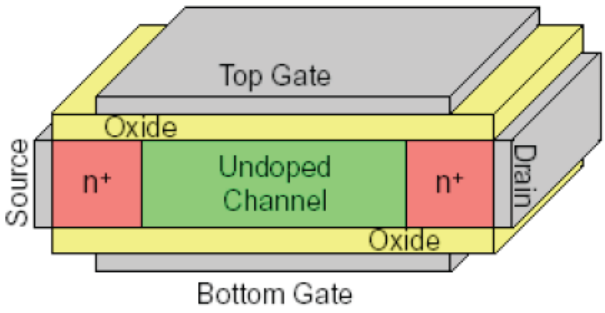

Fig. 4 Structure of DG N-MOSFET

Wang [6] in his thesis describes a comprehensive; simulation based scaling study – including device, performance characterization, and the impact of statistical variability – on decananometer bulk MOSFETs. After careful calibration of fabrication processes and electrical characteristics for n- and p-MOSFETs with 35 nm physical gate length, 1 nm oxide thickness and Doping profile Source and drain doping is 2x1020 cm-3, the simulated devices closely match the performance of contemporary 45 nm CMOS technologies. Scaling to 25 nm, 18 nm and 13 nm gate length n and p devices follows generalized scaling rules, augmented by physically realistic constraints and the introduction of high-k/metal-gate stacks.. It has been found that while scaling from 35 nm to 25 nm, threshold voltage variation is increased from 45 mv to 80 mv while it reduces to 70 mv in 18nm, Off current also increases 3.4 times to 7 times while scaling from 35 nm to 25 nm and ON current increases from 8 % to 17% for scaling of 35 nm to 25nm, while it increases to 26% in 18 nm.

Changhwan Shin et al [7] gives performance and threshold voltage variability of fully depleted silicon-on-insulator (FD-SOI) MOSFETs and are compared against those of conventional bulk MOSFETs via 3-D device simulation with atomistic doping profiles at 22 nm gate length. For FDSOI and the Doping concentrations of channel is 1×1018cm-3and for source/drain region is kept at 2×1019cm-3. Oxide (SiO2) thickness =1nm. Vdd =0.9. The result shows the FDSOI is Better over Bulk MOSFET to reduce short channel effect. The result obtained is shown in table.

Table. 3 Comparison of device Performance Parameters for VDD = 0.9

VDD= 0.9	FDSOI		BULK MOSFET	
	N-Type	P-Type	N-Type	P-Type
ION[µA/µm]	704	417	483	301
IOFF[nA/µm]	3	3	3	3
SS [mV/dec]	75	83	81	89
VT [mV]	164	-186	182	-207
DIBL [mV/V]	54.1	72.9	56.6	76.5

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Alok Kumar Kushwaha [8] suggested a advanced structure i.e SOI as an alternative to bulk MOSFET. Due to scaling down, short channel effect and secondary effects begin to influence the device performance significantly and more accurate device models as also innovative MOS device structures are required to be necessarily developed. Silicon-On Insulator (SOI) technology is one such alternative which can offer the performance as may be expected from next generation Si technology. Dual Material DG FDSOI MOSFET is used in this paper. Oxide thickness is 1 nm & doping concentration is 1x1017 cm-3. Result shows the reduction in SCE. The drain current increases with increase in the gate metal work function difference. The effect of DIBL is considerably reduced. Better control on threshold voltage is obtained.

Saji Joseph, George James et al [9] This paper investigates the effect of doping two thin layers of the channel close to the top and bottom gate oxide layers of a symmetric DG MOSFET. An increase in threshold voltage is observed if those layers are p-doped, with an accompanying decrease in leakage current when compared with an intrinsic channel device. But p-doping also reduces the drive current. But the decrease in drive current is less for a layer doped device than that for a full body doped device. Thus a p-layer doped device provides threshold voltage tunability lacking in intrinsic channel DG MOSFETs, along with greater drive current than full body doped devices. The Doping concentrations of channel is 1×1019cm-3and for source/drain region is kept at 5×1019cm-3. Oxide (SiO2) thickness =1nm. The device structure is given below.

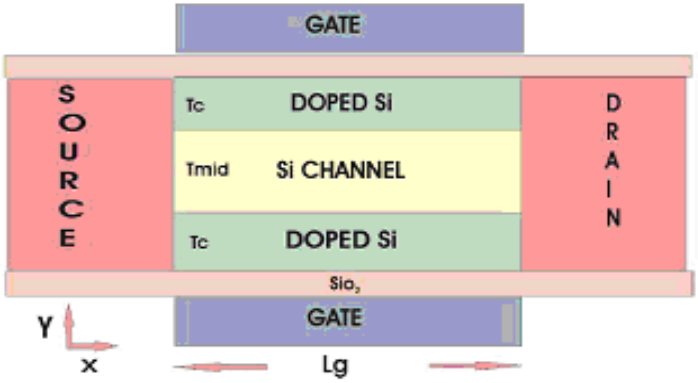

Fig. 5 A layer doped double gate MOSFET (LDDG MOSFET) structure.
Two thin layers of the channel close to the top and bottom gates are doped, while the middle layer is left undoped.

III. CONCLUSION

The scaling down to lower node MOSFETs has various challenges such as SCE, DIBL, High ON drive current, Sub-threshold voltage & parasitic capacitances. SCE can be reduced by properly adjusting Fin thickness twice the body thickness. Vertical Gate architectures can more area efficient & less complicated as compared to other. Use thick hard mask if gate oxide is not flexible to reduce parasitic capacitance. FinFET devices increase electrical width thus increasing device area which helps in reducing interconnect capacitance. It is clear from this paper that all these challenges are overcome by using various structures such as Double Gate (DG) MOSFETs, Multi-fin FinFETs & Gate All Around (GAA). Double gate & multi gate structure provide extra gate to reduce the problems caused due to scaling down of device. Thus proper design of these structures and the analyzing the each structure separately & the comparing the results with each other will yield the performance of MOSFETs.

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