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FPGA Based Pulse Amplitude Modulation Scheme Using DFL

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ABSTRACT: In this paper a Pulse Amplitude Modulated Signal (PAM) is generated using the principle of Digital Frequency Locking (DFL). The proposed method is used to lock other frequencies to a desired (reference) frequency and to carry out amplitude modulation whenever the frequency is being locked. Using the new method we can lock frequencies to a desired frequency with a single FPGA clock and pulse amplitude modulation can be performed. Thus by using a single FPGA clock we can eliminate the use of external VCOs. The main components of this system are a Direct Digital Synthesiser (DDS), DFL circuits and Amplitude modulation circuits. The information (data) on each clock cycles can be obtained during simulation and here DFL is performed using counters, thus reduces the errors and analog circuits.

KEYWORDS: Digital Frequency Locking, Direct Digital Synthesiser, Amplitude Modulation, Counters.

1. INTRODUCTION

Today we are living in a digital era. As technology is improving the communication systems gets converted into digital machines. The concept of analog frequency locking is an ancient one but it is quite difficult to do this digitally. The new digital technology extended their hands to solve this problem. But due to higher gate requirements it becomes more expensive. Also in this era of FM world it is much more important to lock a particular frequency to one of the desired frequency and also this locked frequency is required to be get modulated for accruing higher transmission ranges. In this paper we are introducing such a system based on counters for locking frequency digitally and to pulse amplitude modulate this locked signal. This is implemented using a single FPGA clock thus reduces the usage of VCOs and helps in eliminating the errors.

Many researches are done in the field of Digital Frequency Locking. In [1] they describe the architecture of a new CMOS fully integrated frequency-locked loop (FLL). It contains a frequency-to-voltage converter (FVC), an operational amplifier (op amp) and a differential voltage-controlled oscillator (VCO). The operation of the proposed circuit is based on frequency comparison of a reference and feedback signals. The architecture of the FVC is built upon capacitors charge redistribution principle, whereas the architecture of the VCO is based on differential delay cells in order to minimize the effect of the power supply and the substrate noise. This will increases the analog requirements and thus causes errors. In [2] An All-Digital Phase Locked Loop (ADPLL) circuit is implemented. The component of the ADPLL is the switch-tuning Digital Control Oscillator (DCO). Even ADPLL provides fast frequency locking, full digitization, easy design and implementation, good stability and controlled DCO the implementation requires external analog components which results in heat dissipation and errors. In [3] the circuits are completely digitized but the increased number of digital components results in the use of complex DCO. In [4] the system is based on a combinational approach of frequency dividing and multiplying which results in the use of complex digital components. In [5] even though frequency locking is done digitally using counters; the amounts of gates are high and errors are occurred even after signal is being locked.

Here the system proposed becomes novel than the existing ones. This uses a single clock multiple clocks for the whole digital system is generated. It also enables to lock frequency purely digital using less number of counters and is capable for extracting data when simulation. Apart from this the system helps to pulse amplitude modulate the locked signal.

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II. PROPOSED SYSTEM

The main components of the proposed Digital Frequency Locking System are counters. When using counters the requirement of gates will be less. Then we have comparators for comparing the desired and available frequency. Another component is Direct Digital Synthesiser which is used to produce a signal that is matched with the desired frequency. For pulse amplitude modulation we produce a carrier wave and using this carrier we will modulate the signal that is already frequency locked.

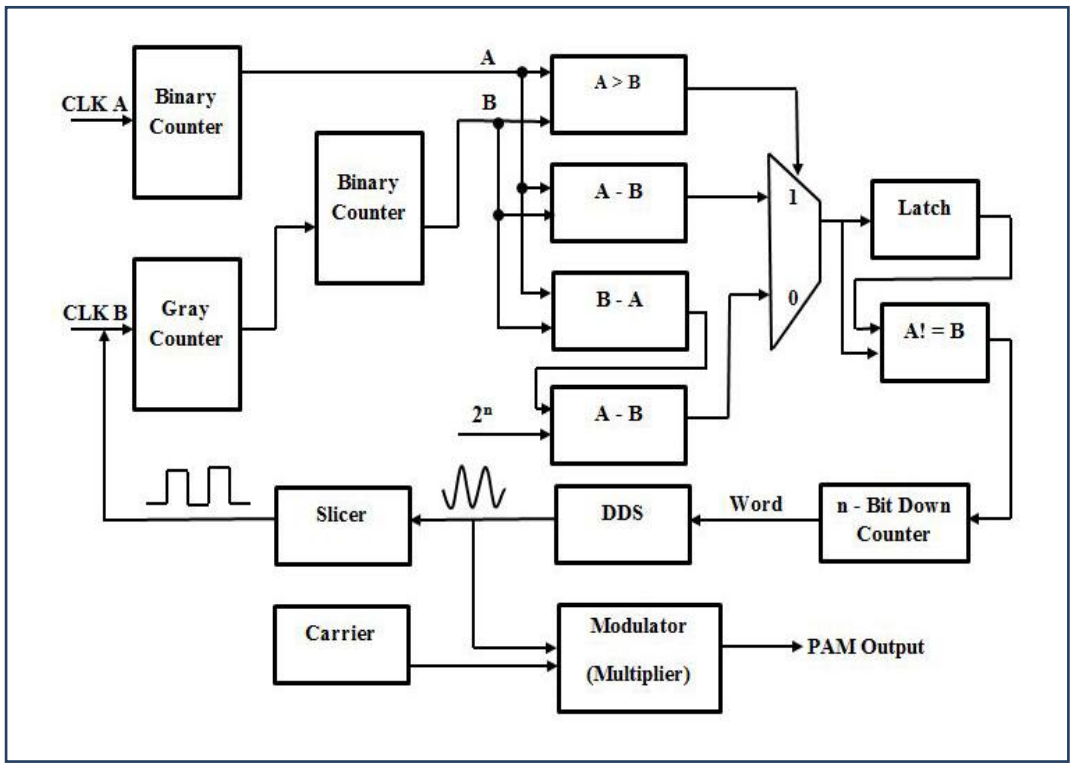

Fig. 1: Proposed FPGA Based Amplitude Modulation Scheme using DFL

Here the frequency is calculated from the counts of the counters according to the clock that is fed. The idea is to first make the differences between the clock as zero, that results in the frequency locking of the signal and to Pulse Amplitude Modulate this locked frequency signal using the PAM modulator section.

Fig. 1 is the proposed system. Here CLK A is the reference (desired) clock and CLK B is to get locked with the reference clock. Here CLK A is directly fed to a Binary Counter. The counter counts the period of the clock. The entire system is based on the difference of the counters. So CLK B cannot be fed directly to another Binary Counter. This is because if all the bits of counter B are in a state of transition, the difference between the counters cannot be limit with a one bit difference and it will result in large error and the required locking is not obtained. Hence in order to limit the counter difference as 'one bit' difference the CLK B is first fed in to a gay counter and after the count it is converted back into the binary count. The count of CLK A is A and that of CLK B is B. Then we find the difference between the counters and are fed to a latch. The comparator checks whether CLK A or CLK B is bigger. If the frequency of CLK A is bigger than CLK B then'B' is get subtracted from 'A' i.e., (A – B) otherwise the 2^n- (B-A) is performed; where 'n' is the bit of the counter. This is to disable Counter A for bigger counts of Counter B, else the negative difference is produced which increases the errors. The latch is used to store the difference for every particular clock.If the counter difference are not a then value of latch is '1', that indicates that frequency of clock B is not matched with that of reference clock. If A! = B the n-bit down counter decrements the value of word by a bit and the present word is fed to

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the Direct Digital Synthesiser. According to the incoming newly decremented word and sine table, DDS produce a sine wave that is closely matched with the reference clock. DDS has a phase accumulator section and a sine table.

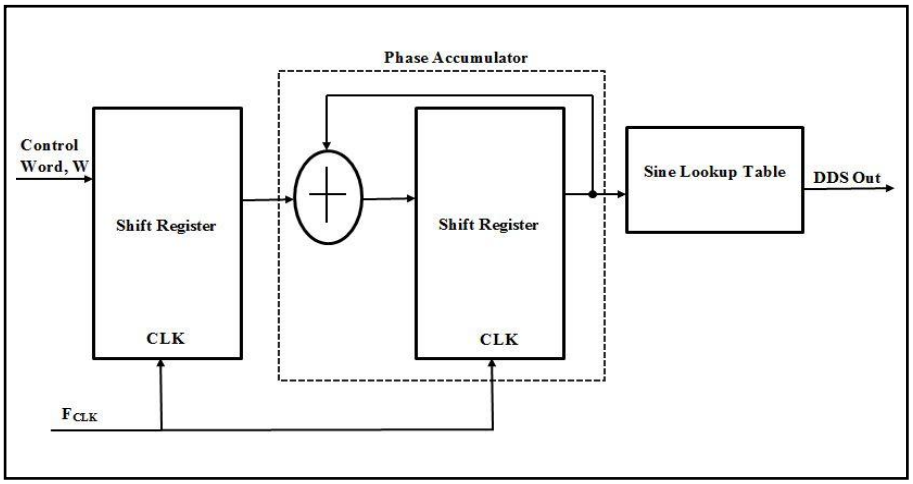

Fig. 2: Direct Digital Synthesiser

Fig. 2 Represents the Direct Digital Synthesiser. Here the DDS performs according to the control word from the n-bit down counter. At the rising edge of the clock the word from the n-bit down counter is added to the phase accumulator. At any instant the value of the accumulator is the phase of the sine wave; which is obtained according to the output (acts as read address of Sine Look up Table) of phase accumulator. That is according to the change in a control word; new sine wave is obtained based on the sine lookup table. The output frequency of the DDS is obtained by the equation

$$f_{clk} = Fclk \left(\frac{W}{2^v}\right) \quad (1)$$

Where f_{clk} the reference clock frequency, 'W' is the word and 'v' is the total bits of the counter.

The DDS output sine wave always changes according to the control word fed from the n-bit down counter. This sine wave is sliced in order to produce a pulse and this is again fed to the binary counter as new CLK B. This process repeats till the difference between count A and Count B becomes 'constant'. When the difference becomes constant the value of latch becomes '0' and the output from n-bit down converter gets disabled. These will in turn results in the production of a signal that is having same frequency that of reference signal. The value of the control word is obtained during simulation. Thus CLK B gets locked to CLK A.

After locking next aim is to Pulse Amplitude Modulate the locked signal. For that the locked sine wave before slicing is fed to the modulator. The carrier wave is a constant pulse and is also fed into the modulator. The modulator acts as a multiplier and multiplies the modulating locked frequency signal with that of the constant pulse carrier wave resulting in the output of Pulse Modulated Signal. Thus, whenever the signal gets locked the locked signal is pulse amplitude modulated and can be transmit to longer distance than present.

III. FUTURE SCOPE

Here we are simulating the system using a single clock. So along with Pulse Amplitude Modulation the technology for Pulse Phase Modulation (PPM) can also be implemented. According to our need; we can amplitude and pulse modulate the locked frequency signal simultaneously using a multiplexer. Counters eliminate the use of analog components. Thus this hardware can implemented in any high end operations and with the help of micro controller module we can formulate the things as our need. Thus this PAM and PPM modulation using DFL scheme will open a new era in the arena of RF Communication. Thus we can use same bandwidth for the same radio station in multiple countries. This also enhances the military security and the practically implemented system can be used in worse terrains.

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IV. RESULT AND DISCUSSION

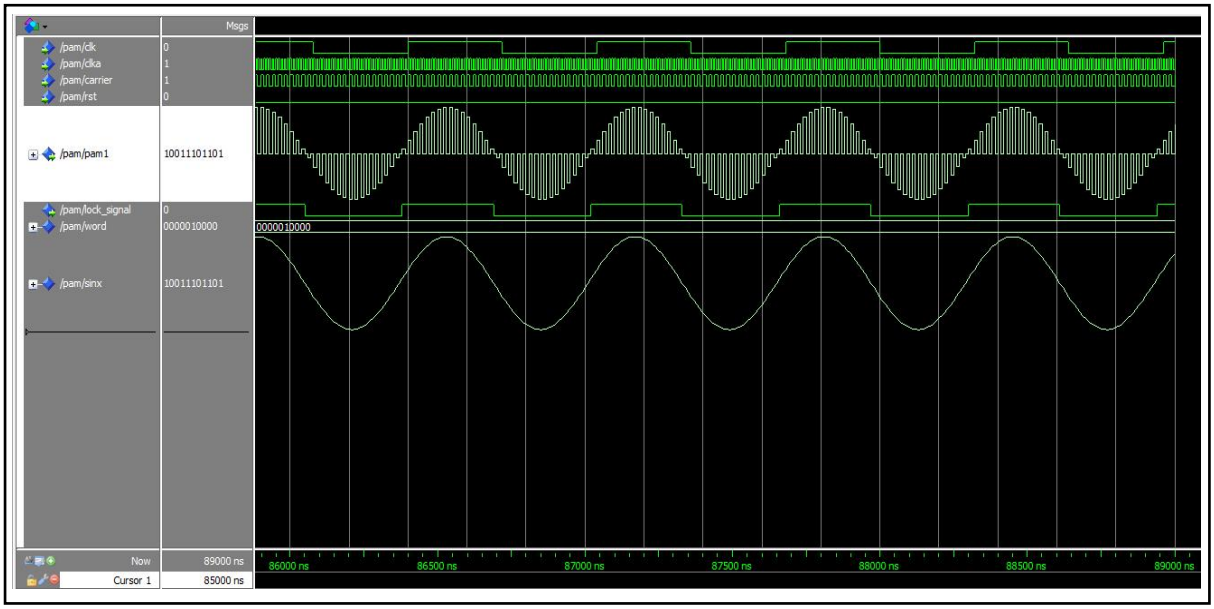

Fig. 3: Simulation Result of FPGA Based Pulse Amplitude Modulation Scheme Using DFL

Fig. 3 shows the simulation result of the entire system. Here 'clk' is the reference clock. 'clka' is the signal that is needed to be locked with 'clk'. 'rst' is the signal that is fed to clear the system initially. After the DFL operations clka gets locked with clk and is shown as lock signal. The signal is locked when the control word reaches '0000010000' and locked DDS output sine wave is represented as 'sinx'. This locked 'sinx' is fed to the PAM section along with the carrier signal shown as 'carrier' and the Pulse Amplitude Modulated Signal is obtained and is represented as 'pam1', which is the entire system output.

V. CONCLUSION

Thus this paper conveys the idea behind the implementation of FPGA based Pulse Amplitude Modulation Scheme using Digital Frequency Locking. Here an unknown signal frequency is getting locked with the desired signal frequency by using the counters and the counter differences. Then these locked signal is fed for Pulse Amplitude Modulation and the output of PAM is obtained that can be used for long distance RF Communication. As, a future scope the implementation of PPM signal along with PAM by DFL scheme is also proposed.

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