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Address Generator For WiMAX Deinterleaver with Optimized Multiplier Design

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ABSTRACT: In this brief, a low-complexity and novel techniques proposed to efficiently implement the address generation circuitry of the 2-D deinterleaver used in the WiMAX transreceiver using the Xilinx field-programmable gate array (FPGA). The floor function associated with the implementation of the steps, required for the permutation of the incoming bit stream in channel interleaver/deinterleaver for IEEE 802.16e standard is very difficult to implement in FPGA. A simple algorithm along with its mathematical background developed in this brief, eliminates the requirement of floor function and thereby allows low-complexity FPGA implementation. The use of an internal multiplier of FPGA and the sharing of resources for quadrature phase-shift keying, 16-quadrature-amplitude modulation (QAM), and 64-QAM modulations along with all possible code rates makes our approach to be novel and highly efficient when compared with conventional look-up table-based approach. The proposed approach exhibits significant improvement in the use of FPGA resources and Design of a customized multiplier which give more efficient and less complex system. Exhaustive simulation has been carried out to claim supremacy of our proposed work.

KEYWORDS: WIMAX, DE-INTERLEAVER,FPGA,QAM

.I. INTRODUCTION

BROADBAND wireless access (BWA) is continuously becoming a more challenging competitor to the conventional wired last mile access technologies [1]. IEEE has developed standards for mobile BWA (IEEE 802.16e) popularly referred to as mobile WiMAX [2]. The channel interleaver employed in the WiMAXt transceiver plays a vital role in minimizing the effect of burst error. In this brief, a novel, low-complexity, high-speed, and resource-efficient address generator for the channel deinterleaver used in the WiMAX transreceiver eliminating the requirement of floor function is proposed. SILICON COST of the permutation tables for interleaver implementation used in the conventional approaches can be very high if the device is supporting many variants inside a particular standard. Low cost on-the-fly address computation with supporting multiple variants has been a challenge due to presence of complex functions. Therefore a low cost and re-configurable architecture for address computation is always beneficial. WiMAX is being used in the communication industry with many variants in channel coding, like different block sizes and different modulation schemes (e.g. BPSK, QPSK, 16- QAM and 64-QAM). System level overview for WiMAX showing use of channel interleaver is shown in Fig. 1. The type of interleaver used here is the block interleaver.

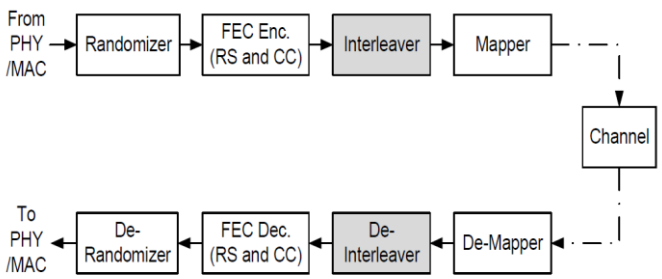

Fig 1: Overview of encoding in WiMAX channel

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The block interleaver can also be considered as a row-column matrix. In this case, data is written row-wise in a memory configured as a row-column matrix and then read column wise after applying certain intra-row and inter-row permutations. Very few works related to hardware implementation of the interleaver/deinterleaver used in a WiMAX system is available in the literature. The work in [3] demonstrates the grouping of incoming data streams into the block to reduce the frequency of memory access in a deinterleaver using a conventional look-up table (LUT)- based CMOS address generator for WiMAX. Khater et al. [4] has described a hardware description language (VHDL)- based implementation of address generator for IEEE 802.16e channel interleaver with only a 1/2 code rate. In [5], the authors have described a finite-state machine (FSM)-based address generator of the same interleaver for all permissible code rates and modulation schemes. Both [4] and [5] are tested on the field-programmable gate array (FPGA) platform. Asghar and Liu in [6] has made 2-D translation of the functions used in WiMAX channel deinterleaver to claim efficient hardware architecture. However, the derivations in [6] do not clearly explain the design issues, particularly for 64-quadrature-amplitude modulation (QAM). Hardware implementation of floor function is very complex and consumes abnormally large amount of resources [6]. Conventional LUT-based technique is found to be unattractive from many aspects such as slowness in operation, consumption of large logic resources leading to inefficiency in resource utilization, etc. A comparative study with a LUT-based technique confirms the superiority of our proposed design. As compared with the complicated and lengthy expressions, particularly for 16-QAM and 64-QAM, due to the 2-D translation in [6], a compact and user-friendly mathematical representation and subsequent algorithm is proposed. The mathematical expressions have formally been proven using [6]. Our proposed algorithm when realized by digital hardware results in low-complexity architecture for the address generator compared with prevailing technique.The basic objective and significance of this project are,

Objective

- To eliminate the conventional LUT method to improve the system.
- To study the WiMAXinterleaver and deinterleaver concepts.
- To study the implementation and improvisation of the existing equation to more simple form.
- To evaluate the issue that facing while practical implementation.
- To provides performance improvement by reducing interconnection delay, efficient resource utilization, and lesser power consumption due to the conventional multipliers.

Significance

- In previous study, derivations in 2D realization do not clearly explain the design issues, particularly for 64-quadrature-amplitude modulation (QAM); which made issues in practical implementation.
- Conventional LUT-based technique is found to be unattractive from many aspects such as slowness in operation, consumption of large logic resources leading to inefficiency in resource utilization.
- Previous study carries complicated and lengthy expressions, particularly for 16-QAM and 64-QAM, due to the 2-D translation.
- Any of the previous study not includes the multiplier designing factors which affects speed, resource utilization, and power consumption.

II. BASIC ALGORITHM

Interleaving Wimax

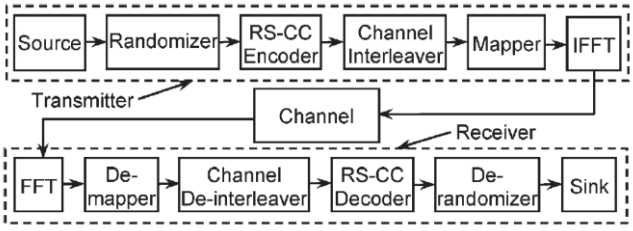

Fig 2: Block diagram of the WiMAX trans-receiver.

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The mandatory blocks of a WiMAX transreceiver are shown in Fig.2. Data stream received from a source is randomized before being encoded by two forward error correction (FEC) coding techniques, namely, Reed–Solomon (RS) and convolutional coding (CC). The channel interleaver permutes the encoded bit stream to reduce the effect of burst error. When convolutional turbo code (CTC) is used for FEC, being optional in WiMAX, the channel interleaver is not required, since CTC itself includes an interleaver within it [7]. Modulation and construction of orthogonal frequency-division multiplexing symbols are performed by the two subsequent blocks, namely, mapper and inverse fast Fourier transform of Fig.4.1. In the receiver, the blocks are organized in the reverse order enabling the restoration of the original data sequence at the output.

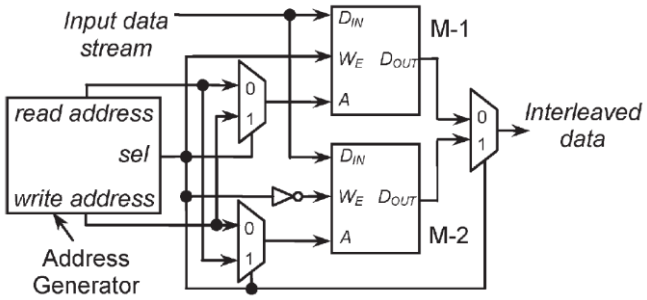

Fig 3: Block diagram of interleaver/deinterleaver structure.

Two-dimensional block interleaver/deinterleaver structure, which is used as a channel interleaver/deinterleaver in the WiMAX system, is described in Fig.4.2. It has two memory blocks, namely, M-1/2 and an address generator. In block interleaving, when one memory block is being written, the other one is read, and vice versa. When sel = 1, write-enabled signal WE of M-1 is active. During this period, the input data stream is written in M-1 as it receives the write addresses. Simultaneously, an interleaved data stream is read from M-2 as it is supplied with the read addresses. After the memory blocks are written/read up to the desired location as specified by interleaver depth, the status of sel signal is changed to swap the read/write operation.

PROPOSED ALGORITHM

Here, the proposed algorithm for address generator of the WiMAXdeinterleaver along with its mathematical background has been described.

N_{cbps}, code rate and modulation type	De-interleaver addresses				
N_{cbps} = 96-bits, ½ code rate, QPSK	0	16	32	48	64
	1	17	33	49	65
	2	18	34	50	66
	3	19	35	51	67
N_{cbps} = 192-bits, ½ code rate, 16-QAM	0	16	32	48	64
	17	1	49	33	81
	2	18	34	50	66
	19	3	51	35	83
N_{cbps} = 576-bits, ¾ code rate, 64-QAM	0	16	32	48	64
	17	33	1	65	81
	34	2	18	82	50
	3	19	35	51	67

TABLE 4: First four rows and five columns of deinterleaver sample addresses

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Row no.(j)	Column no. (i) →	0	1	2	3	4
0	N_{cbps} = 96-bits, ½ code rate, QPSK	*d*.0+0=0	*d*.1+0=16	*d*.2+0=32	*d*.3+0=48	*d*.4+0=64
1		*d*.0+1=1	*d*.1+1=17	*d*.2+1=33	*d*.3+1=49	*d*.4+1=65
2		*d*.0+2=2	*d*.1+2=18	*d*.2+2=34	*d*.3+2=50	*d*.4+2=66
3		*d*.0+3=3	*d*.1+3=19	*d*.2+3=35	*d*.3+3=51	*d*.4+3=67
0	N_{cbps} = 192-bits, ½ code rate, 16-QAM	*d*.0+0=0	*d*.1+0=16	*d*.2+0=32	*d*.3+0=48	*d*.4+0=64
1		*d*.1+1=17	*d*.0+1=1	*d*.3+1=49	*d*.2+1=33	*d*.5+1=81
2		*d*.0+2=2	*d*.1+2=18	*d*.2+2=34	*d*.3+2=50	*d*.4+2=66
3		*d*.1+3=19	*d*.0+3=3	*d*.3+3=51	*d*.2+3=35	*d*.5+3=83

TABLE 5: Determination of correlation between addresses

Table 4 shows the deinterleaver addresses for the first four rows and five columns of each modulation type. As d = 16 is chosen, the number of rows are fixed (= d) for all Ncbps, whereas the number of columns are given by Ncbps/d. A close examination of the addresses in Table 4.1 reveals that the correlation between them follows the manner, as shown in Table 5. The mathematical foundation of the correlation between the addresses, as derived in this brief, is represented by (5)–(6), i.e.,

$$k_{n,\text{QPSK}} = \{ d * i + j \quad \text{for } \forall j \text{ and } \forall i \tag{5}$$

$$k_{n,\text{16-QAM}} = \begin{cases} d * i + j & \text{for } j\%2 = 0 \text{ and for } \forall i \\ d * (i+1) + j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 0 \\ d * (i-1) + j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 1 \end{cases} \tag{6}$$

From Table 5 and the mathematical representation by (5)–(6), following three algorithms for the three modulation schemes are proposed. These algorithms eliminate the requirement of floor function while generating write addresses. These algorithms are also tested on Modelsim.

A. QPSK

initialize *N*cbps and *d*
for*j* = 0 to *d* − 1, *j* ++
for*i* = 0 to (*N*cbps/*d*) − 1, *i*++
kn= *d* ∗*i* + *j*
end for
end for

B. 16-QAM

initialize *N*cbps and *d*
for*j* = 0 to *d* − 1, *j* ++
for*i* = 0 to (*N*cbps/*d*) − 1, *i*++
if (*j* mod 2 = 0)
kn= *d* ∗*i* + *j*
else
if (*i*mod 2 = 0)
kn= *d* ∗(*i* + 1) + *j*
else
kn= *d* ∗(*i* − 1) + *j*

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end if
end if
end for
end for

III. DESIGN AND SIMULATION

TRANSFORMATION INTO CIRCUIT

In order to test the proposed algorithms for the address generator of the WiMAXdeinterleaver with all modulation schemes, transformations of these algorithms into digital circuits are made and are shown in Fig.6-7.

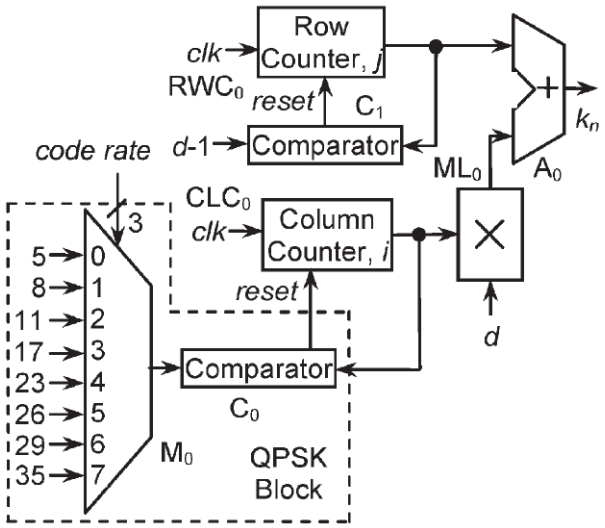

Fig 6: Hardware structure of the address generator for QPSK.

The QPSK hardware shown in Fig.6 has a row counter RWC0 to generate row numbers between 0 and d − 1. A column counter CLC0 with multiplexer M0 and comparator C0 generate the variable column numbers to implement permissible Ncbps. A multiplier ML0 and an adder A0 perform the desired operations to implement (5).

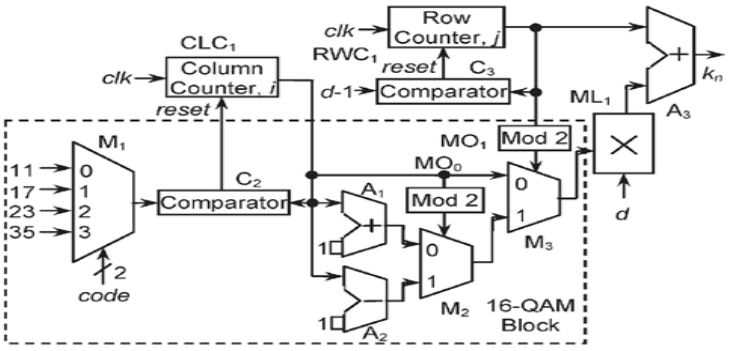

Fig 7: Hardware structure of the address generator for 16-QAM.

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The address generator for 16-QAM follows a similar structure, such as that of QPSK with few additional modules. These modules are designed with an incrementer, a decrementer, two modulo-2 blocks, and two multiplexers, as shown in Fig.7.

IV.SIMULATION RESULT

The proposed hardware of the address generator is converted into a VHDL program and Simulation results are obtained for all permissible modulation types and code rates using ModelSim SE-64 has been presented in Fig. 8

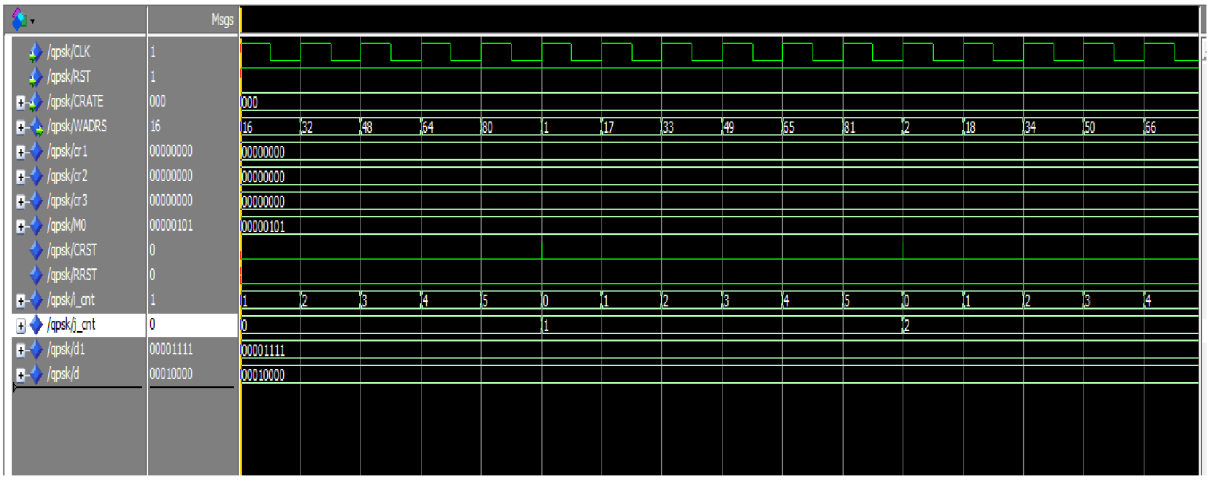

Fig 8: Simulation output for QPSK.

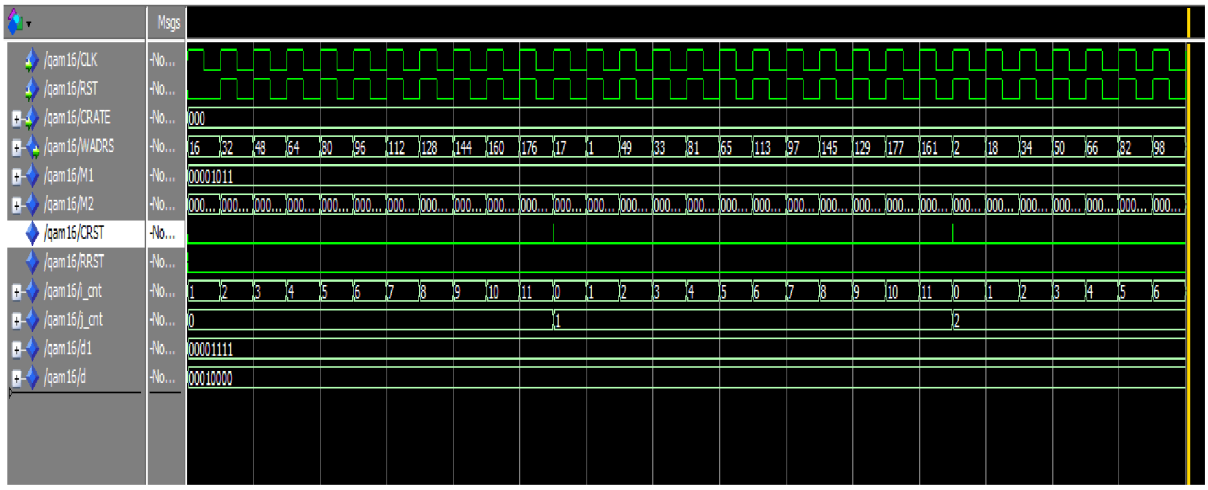

Fig 9: Simulation output for 16-QAM.

V. RESULT AND DISCUSSION

A detailed literature survey was done on related topics has proposed a novel algorithm along with its mathematical formulation, including proof for address generation circuitry of the WiMAX channel deinterleaver supporting all possible code rates for modulation patterns QPSK and 16-QAM as per IEEE 802.16e.

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So the further progression of my work includes 64-QAM and optimized Multiplier design to provide performance improvement by reducing interconnection delay, efficient resource utilization, and lesser power consumption. Also carry implementation and analysis of the same.

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