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Highly Efficient Deinter Leaver Address Generator and Dynamically Switchable Modulation for WIMAX

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ABSTRACT: WiMax promises to connect the "last mile" of broadband wireless communication services and offer the Internet to every corner of the world. The paper offers a novel approach, its mathematical formulation, and evidence that the address generating circuitry of the WiMAXchannel deinterleaver may support any conceivable coding rate and modulation patternin line with IEEE 802.16e. The suggested method results in an effective digital hardware circuit. On the Xilinx FPGA, the hardware is implemented using VHDL. Comparing our suggested strategy to recent work and a conventional LUT-based technique, we find that it greatly improves resource utilization andoperating frequency.

KEYWORDS: WiMAX(Worldwide Interoperability for Microwave Access), WiFi(Wireless Fidelity), Xilinx FPGA(field- programmable gate array), VHDL(very high- speed integrated circuit hardware description language)

I. INTRODUCTION

In order for WiMAX to function, the IEEE 802.16standard for BWA systems must be met. Within the2–11 GHz band, IEEE 802.16d, now known asIEEE 802.162004, specifies fixed BWA (FBWA) [2]. With the addition of mobility capabilities, the updated IEEE 802.16e standardizes mobile BWA (MBWA) in the 2 to 6 GHz frequency band. The usual data rate for IEEE 802.16e is 5 Mbps, and thebandwidth ranges from 1.25 to 20 MHz. Both IEEE802.16e and IEEE 802.162004 allow for non-line- of-sight (NLOS) communication. By using randomness, this strategy prevents the system from receiving lengthy sequences of 1s and 0s, which could disrupt the receiver's timing recovery. To make the data truly random, pseudo-random binary sequences (PRBS)add them modulo 2 to the PBRS's output [13]. Thenext step is to use convolutional coding (CC) and the Reed Solomon (RS) encoder to encrypt the bitsof random input. If you need to correct errors in a burst, use the former; if you need to correct errors randomly, use the later. The final step in RSCC encoding is to use a block interleave to interleave all of the encoded data bits.

Known as WiMAX, it stands for Worldwide Interoperability for Microwave Access. The WiMAX standard is based on the IEEE 802.16 group's wireless MAN standards. In the licenced exempt spectrum, it operates between the 2-11 GHz range, while in the licensed spectrum, it operates between the 10-66 GHz band. Connecting to the Internet and providing a wirelesslast-mile extension for cable and DSL internet access were the primary goals of its creation. Witha service area range of up to 50 km, IEEE 802.16 enables users to connect even when there is no direct line of sight (LOS) to a base station (BS). The system also provides shared data speeds of upto 70 Mbps, which is more than enough capacity for a large number of users simultaneously.

Most people, if not compelled to, think of DSL, T1,or cable modem when they need a network service,such as broadband connectivity. Internet service providers (ISPs) may be hesitant to deployhardware like optical fiber and cables in less densely inhabited areas because of the high cost ofconstructing a cable network's infrastructure.

Already mentioned are a few broadband access technologies that have been proposed: LMDS and MMDS. But back then, there was no universally accepted technical standard for LMDS and MMDS, and different manufacturers' air interfacesweren't compatible with one another, whichseverely limited the expansion of the communication industry as a

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whole.

By allowing for flexible adjustment of the channelband width between 1.5 and 20 MHz, WiMAX is able to make full use of the frequency spectrum resource in the distributed channel bandwidth, andits operating frequency ranges from 2 to 66 GHz (2-11 GHz for IEEE802.16 standards and 10-66 GHz for IEEE802.16a standards). The maximum range of WiMAX, which uses macro cells, is 50 km. The 20 MHz channel band width allows for data transmission speeds of up to 70 MB/s, with a maximum coverage of 3 to 5 kilometres in this case. With multi-sector technology, the system capacity can be enhanced to support over 60 business users or hundreds of family users of E1/T1 at the same time. WiMAX uses a number of cutting-edge technologies, including OFDM, receiving transmitting diversity, and adaptive modulation, to implement NLOS and ONLOS transmission. These technologies significantly increase wireless transmission efficiency in urban areas.

To meet the demands of different regional or worldwide telecommunications networks, the physical layer can support two kinds of wireless duplex multiple access: TDD/DMTA and FDD/TDMA. The user has the option to select between OFDM (256 points), single carrier (SC), and OFDMA (2048 points). The physical layer could change based on the transmission channel's performance.Of course-fed multiple-user (OFDM) is a technology for wireless networks that allows for very fast data transfers. Frequency response curves are typically not flat in wireless channels. The bonded channel is split into numerous orthogonal sub-channels in the frequency range such that eachsub-channel can use a sub carrier for modulation and be broadcast in parallel. As a result, narrow- band transmission is performed on these sub-channels with signal band widths that are smaller than the corresponding channel band widths, and each sub-channel remains relatively flat eventhough the non-flat channel has various frequencyoptions.

II. LITERATURE SURVEY

A literature review is a written report that aims to offer readers an awareness of the most recent research and conversations relevant to a specific subject or area of study. The results of a literature study can help us learn more about this area. Here we will learn about important concepts, research methods, and experimental processes that are relevant to your field. We will also look at real- world examples of researchers applying what you learn in class to address real-world issues. Anotheramazing thing about literature reviews is that theyhelp us grasp the presentation and debate of research findings in your particular subject as we read.

[5] There is a dearth of literature on the topic of WiMAX interleaver/deinterleaver hardwareimplementation. According to the research in [5], adeinterleaver that uses a conventional look-up table(LUT) CMOS address generator for WiMAX can reduce the frequency of memory accesses by organising incoming data streams into the block. Implementation of an address generator for an IEEE 802.16e channel interleaver with a 1/2 coding rate based on hardware description language (VHDL).

Due to their fundamentally complex capabilities, Asghar et al. are unable to maximize equipment production. Furthermore, the standard approach, like storing the altering tables in memory, is silicon-growing. This research shows that the WiMAX channel interleaver capacity may be improved in two dimensions, which makes it easierto process interleaver addresses instantaneouslyand decreases the overall equipment unpredictability.

The WiMAX channel interleaver is shown with a fully adjustable architecture for location age that consumes 1.1 k-entryways in total. In WiMAX, it frequently adapts to any square size and any balancing scheme. In order to meet the high transmission capacity requirements of WiMAX, the demonstrated architecture may keep operating at a repetition of 200 MHz. In this study, Kuo et al.compare and contrast 90-nm CMOS standard cell ASICs with field programmable gate arrays (FPGAs) in terms of logic thickness, circuit speed,and power consumption for center logic.

An improved FPGA-inserted asset-based memory and a constrained state machine-based location generator are components of the equipment model created by Bijoy Kumar Upadhya et al. In comparison to current FPGA procedures, the interleaver's restricted state machine-based location generator performs better in terms of maximum working repetition and FPGA asset utilization. Utilizing an FPGA's embedded memory has advantages over systems that rely on external memory, including faster access times, reduced circuit load up, and lower control use. Alsoincluded

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are evaluated control utilization and programming recreation for the whole interleaver as well as the location generator. Our architecture is based on the IEEE 802.16e standard, which is where all the WiMAX coding rates and modification plans are connected. Our method also lends itself to the computation ofinterleaver addresses.

III. METHODOLOGY

Various methods are used in this paper, such as expert opinions, literature reviews, contentvalidation, and focus groups. Additionally, it makes use of quantitative and qualitative perspectives. Furthermore, it is necessary to conduct a challenging construct validity evaluation that considers both structural and substantive factors. Research on conceptualizing and evaluating information needs has a long history. Towiden the scope of this, a methodology is given; avariant of the methodology suggested in this workhas been used in other disciplines with positive results.

The figure 1 shows the interleaving of encoded data using a block interleaver. How many bits (Ncbps) are encoded for each sub channel in an OFDM signal dictates the block size. The interleaver is called a two-step permutation in IEEE 802.16. Coded bits are mapped onto non- adjacent subcarriers when neighboring ones are present, according to the first. To avoid lengthy strings of unreliable bits, the second permutation maps close-coded bits alternatingly onto less- and more-important bits of the constellation. The Interleaver can be described using permutations that involve two steps. The first one makes sure that coded bits are mapped onto non-adjacent subcarriers when nearby ones are present.

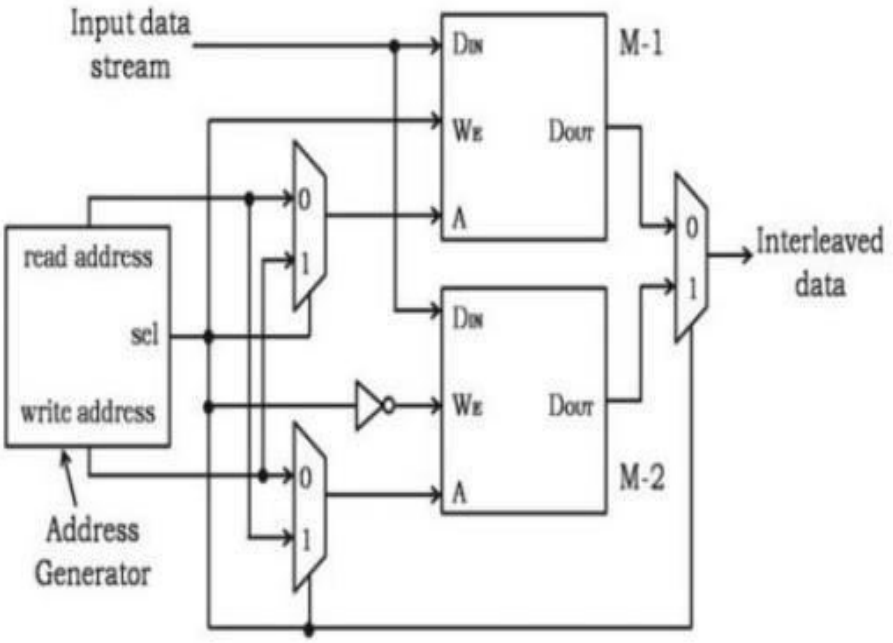

Fig 1 PROPOSED SYSTEM

Software details

Simulation: System-level testing is done using theI-sim logic simulator that is built into the system. The I-sim logic simulator carries out the followingto ensure that the module produces the correct outputs: 1) Logical verification; 2) Behavioural verification to look for logical and temporal problems; and 3) post-place & route simulation to look at module behaviour after it has been insertedinto the reconfigurable logic of the FPGA. A test bench programme that monitors and verifies the outputs of the item being tested uses simulated input signal waveforms.

Synthesis: Xilinx ISE enables the algorithm to execute up to 30% faster than competing programmes, which reduces project costs and post-placement errors that may emerge as a result of theFPGA fabric's increasing complexity.
The FPGA, an integrated circuit, contains a sizable number of identical logic cells, or "standard components," as

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Vol. 6, Issue 2, February 2017

depicted in Figure 2. When you combine these fundamental components to make the circuit, you get complex designs.

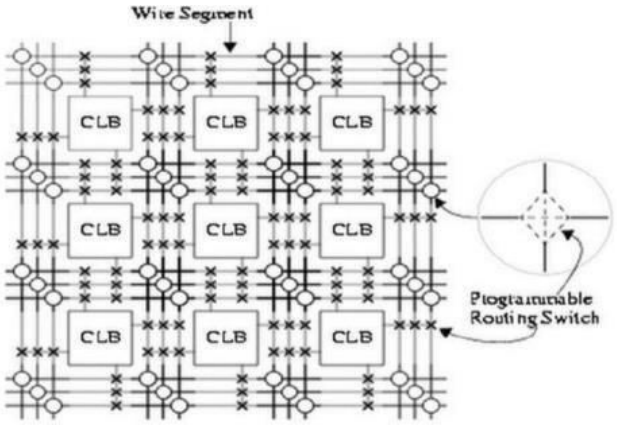

Fig 2 logic cells

HARDWARE REQUIREMENTS

After turning on the power supply, the Spartan-6 FPGA board needs to be programmed before it cancarry out any tasks. Any of the following configuration options are available for the FPGA. When the power is on, the PC can program the FPGA using the appropriate USB Programming port. BPI-UP can be used to transmit configuration files from non-volatile devices to the FPGA whilethe power is on, and the SPI port can be used to transfer files from non-volatile SPI PCM devices to the FPGA.

IV. RESULTS

An effective digital hardware circuit is createdfrom the suggested way. The Xilinx FPGA uses Verilog to implement the hardware. Both resource utilization and operational frequency are significantly enhanced by our proposed strategy when compared to current work and a typical LUT-based method

Table 1: Device Utilization of existing method

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	47	54576	0%
Number of Slice LUTs	132	27288	0%
Number of fully used LUT-FF pairs	47	132	35%
Number of bonded IOBs	30	218	13%
Number of BUFG/BUFGCTRLs/BUFHCEs	1	16	6%
Number of DSP48A1s	1	58	1%

As shown in table 1, this particular address generator uses fewer devices than the current models. Therefore, as indicated in the proposed method, table 2, the efficiency will rise as a result of the hardware's lower utilization. Additionally, this design's maximum operating frequency is higher than the result achieved for the design suggested in.

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Table 2: Proposed Method

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	13	94176	0%
Number of Slice LUTs	46	27288	0%
Number of fully used LUT-FF pairs	14	46	30%
Number of bonded IOBs	20	218	9%
Number of BUFG/BUFGCTRLs/BUFHCEs	1	16	6%

For each of the WiMAX-allowed modulation schemes, this modified address generator was modelled in Xilinx ISE, and the simulation resultswere acquired using ISim Simulator. The completeaddress generator's Register Transfer Level (RTL)Schematic is displayed in Figure 3 and 4.

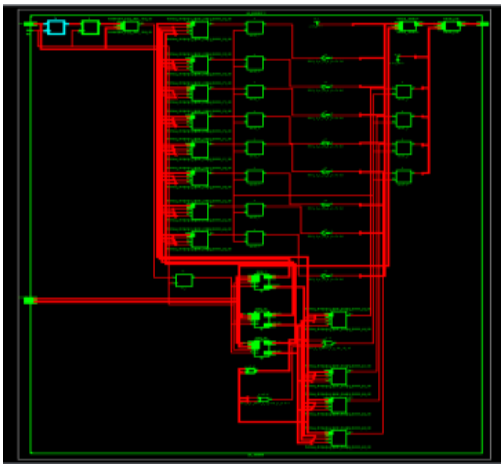

Fig 3: RTL Schematic of the existing method

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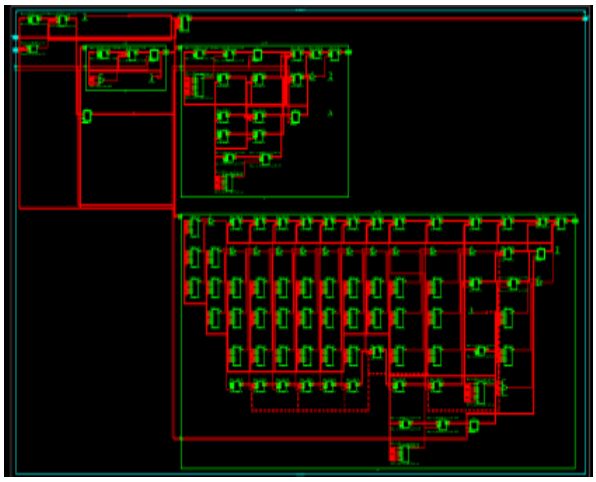

Fig 4: RTL Schematic of the proposed method

Existing RTL_TOP is as shown in fig 5.

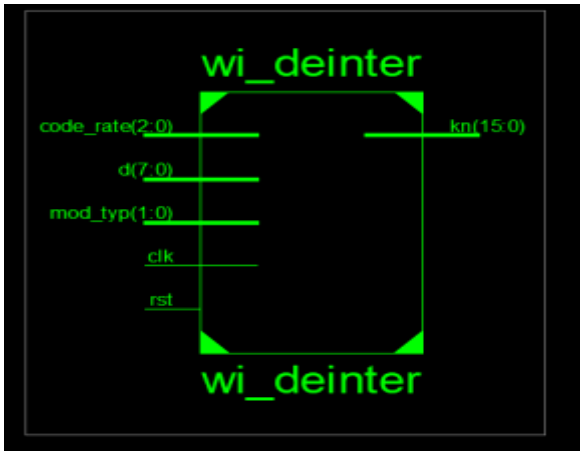

Fig 5: Existing RTL_TOP

RTL is used in the integrated circuit design cycle's logic design phase. An RTL description of the circuit is frequently transformed into a gate-level description of the circuit by a logic synthesis tool. The results of the synthesis are then used to construct a physical layout utilizing placement androuting tools. Next, a physical layout is built usingplacement and routing tools based on the synthesisresults. A base resistor links the input voltage source to the base of an RTL, and both stages sharean emitter. By converting the input voltage into current, the base resistor allows the tiny transistor's input voltage range to be extended to the logical "1" level.

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The inputs of an RTL circuit consist of resistors, whereas the outputs are made up of transistors. Thecomponents of the switching system are transistors. A connection is made between the ground and the transistor's emitter. The collector terminals can be linked to the supply through the resistor RC. The collector resistance is a passive pull-up resistor.

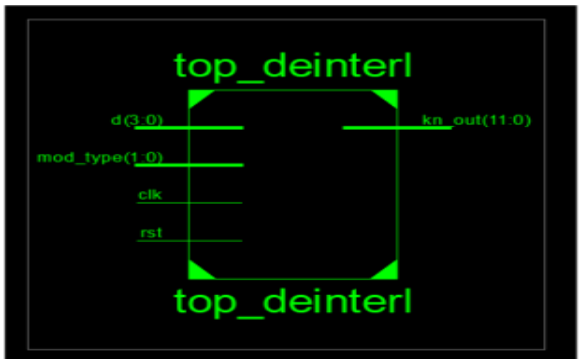

Fig 6:Proposed RTL_TOP

The simulation comparison between existing and the proposed methodology are as shown in figures7 (a) to 7 (d)

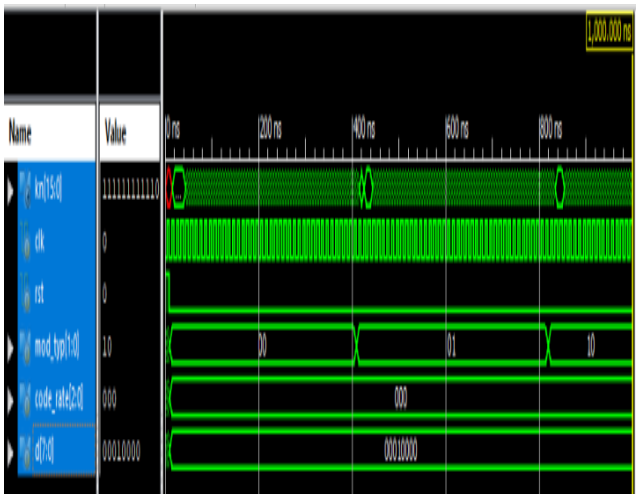

Fig 7(a): Simulation results for Existing method

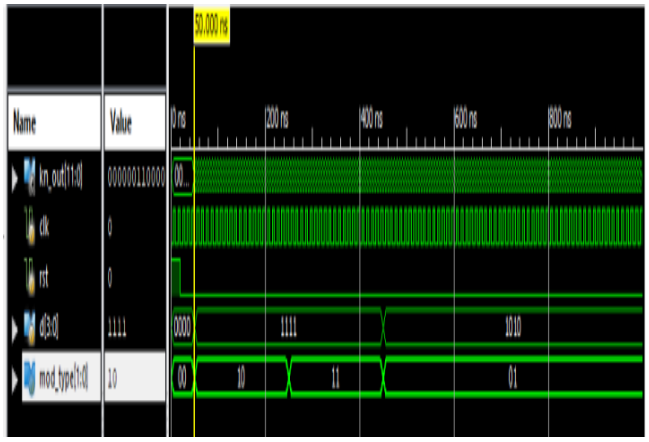

Fig 7(b):Simulation results for Proposed method

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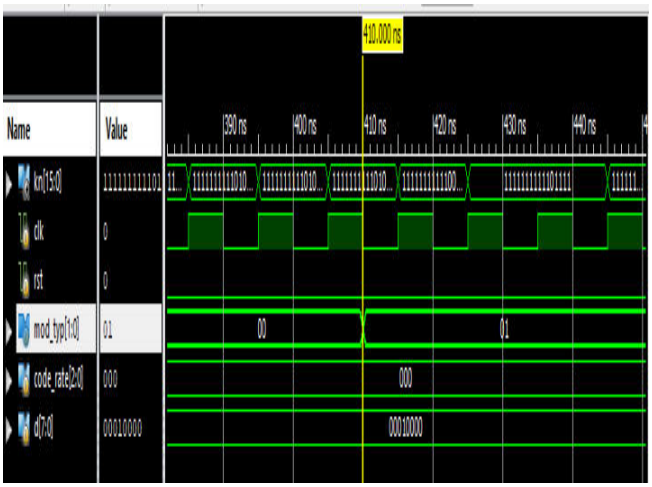

Fig 7(c): Existing method

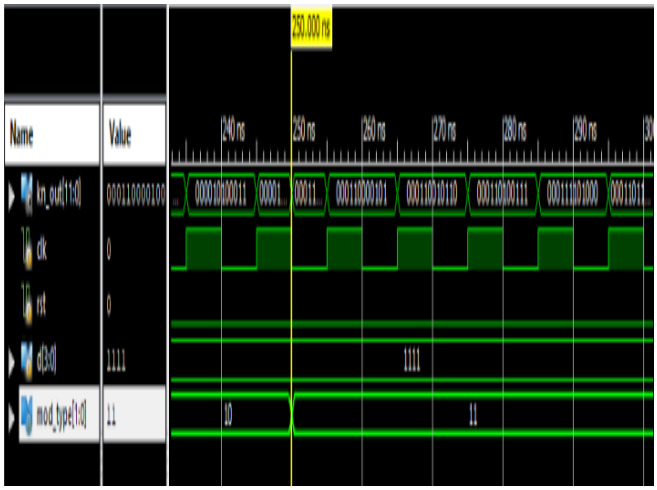

Fig 7(d): Proposed method5.

V. CONCLUSION

A deinter leaver consists of two main modules: random access memory (RAM) and an address generator. Using Modelsim, we tested the address generator that is built using the Mealy machine. The design for FPGA implementation was synthesized using an ISE Spartan chip from Xilinx. For this method to work, it needed some novel algorithmic programming, mathematical formulation, and proof of concept for WiMAX channel deinter leaver address generating circuitry that could handle any possible code speed and modulation pattern according to IEEE 802.16e. . One outcome of the suggested method is a digital hardware circuit with integrated components. Xilinx FPGA hardware is built using Verilog HDL.The suggested research significantly improves upon the conventional LUT-based method in termsof both resource potency and operationalfrequency.

By including the floor function into the permutation formula specified by IEEE 802.16, the operating frequency and hardware requirements have been successfully decreased. The deinterleaver's circuit has been generalized by our proposed method to take a wide range of Interleaving Depth (Ncpbs), which makes itsuitable for future improvements.

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REFERENCES

[1]https://www.gaussianwaves.com/2010/10/interl eavers-and-deinterleavers-2/
[2] B. Sklar, Digital Communications Fundamentals and Applications,Englewood Cliffs, New Jersey: Prentice Hall, 1988.
[3] A. J. Viterbi, "Spread Spectrum Communications – Myths and Realities," IEEE Communications Magazine, vol. 17, No. 5, pp. 11- 18, May 1979.
[4] Praveena K P. Aparna Bhavani V " Address Generation Based WIMAX Deinterleaver using FPGA " International Journal of Engineering Research & Technology (IJERT) Vol. 2 Issue 12, December - 2013 IJERT ISSN: 2278-0181.
[5] Omar Rafique, Gangadharaiah S.L. "Hardware Efficient WiMAX Deinterleaver Capable of Address Generation for Random Interleaving Depths" International Journal of Engineering Trends and Technology (IJETT) – Volume 10 Number 4 - Apr 2014
[6] Upadhyaya, B.K., & Sanyal, S.K. Novel design of WiMAX multimode interleaver for efficient FPGA implementation using finite state machine based address generator.
[7] B. K. Upadhyaya and S. K. Sanyal, "Efficient FPGA Implementation of Address Generator for WiMAX Deinterleaver," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 8, pp. 492-496, Aug. 2013, doi: 10.1109/TCSII.2013.2268372.
[8] Naykodi, Mallikarjun. (2014). DESIGN AND IMPLEMENTATION OFADDRESSGENERATOR FOR WIMAX DEINTERLEAVER ON FPGA. International Journal of Research in Engineering and Technology.03.139-142.10.15623/ijret.2014.0315025.
[9] Shilpa Marathe and M. Zahid Alam " Design of Wimax Interleaver using Finite State Machine" International Journal of Electrical, Electronics ISSN No. (Online) : 2277-2626 and Computer Engineering 1(2): 60-64(2012)
[10] Wani, Faheem & Chandel, Tarana. (2016). Efficient Implementation of Address Generator for WiMAX Deinterleaver with Different Modulation Schemes.
[11] A. Ghosh, David R.Wolter J G. Andrews, Runhua Chen, Broadband Wireless Access with WiMax/802.16:Current Performance Benchmarks and Future Potential, IEEE Communication Magazine, Feb 2005.
[12] Deepak Bhardwaj, S P Singh, V K Pandey "VHDL Implementation of Efficient Multimode Block Interleaver for WiMAX", IJECSE, 2012.
[13] Khater, A. A., Khairy, M. M.,& Habib, S. E.D. (2009). Efficient FPGA implementation for the IEEE 802.16e interleaver. In Proceedings of International Conference on Microelectronics (pp. 181–184). Marrakech, Morocco.
[14] Upadhyaya, B. K., Misra, I. S., & Sanyal, S.K. (2010). Novel design of address generator for WiMAX multimode interleaver using FPGA based finite state machine. In Proceedings of 13th International Conference on Computer and Information Technology (pp. 153–158). Dhaka, Bangladesh.
[15] Venkatachalam., N. K., Lakshminarayanan, G., & Sellathurai, M. (2016). Low complexity and area efficient reconfigurable multimode interleaver address generator for multistandard radios. IET Comput Digit Tech, 10(2), 59–68
[16] K. H. Teo, Z. Tao and J. Zhang, "The Mobile Broadband WiMAX Standard," IEEE Signal Processing Magazine, September, 2007, pp. 144148.
[17] A. Ghosh, D. R. Wolter, J. G. Andrews and R. Chen, "Broadband Wireless Access with WiMAX/802.16: Current Performance Benchmarks and Future Potential," IEEE Commun. Mag., vol. 43, Feb. 2005, pp. 129–36.