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Reconfigurable FIR Filter Design using DA Algorithm for Sand Monitoring System

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ABSTRACT: In the oil industry Sand analysing system is used toovercome the problem of equipment deterioration and production failure. For the measurement of sand production in oil and gas systems the effective design and implementation is done using FPGA as real time application. The analysing system consists of two acoustic sensors for the measurement of assessing the impact of sand along with one Doppler sensor to measure the pace of sand particles. For the actual time information acquisition and processing the system is implemented using FPGA. For the high accuracy measurement of sand production Fully Parallel, Fully Serial and DA architecture are implemented. DA architecture has better performance than other architectures as it uses Multiplier-less technology which increases the speed of the system (136.049 MHz). The proposed cost effective sand analysing system can achieve high accuracy.

KEYWORDS: Distributive Arithmetic (DA), Finite Impulse Response (FIR) filter, Reconfigurable filter, Field Programmable Gate Array(FPGA).

I.INTRODUCTION

In the oil organizations, to shield the gear from the harm brought on by sand disintegration system utilizes the sand examining framework to enhance the unwavering quality and precision. Sand disintegration can be observed and distinguished by the Acoustic based and Doppler based framework. To maintain a strategic distance from the breaking down component into the pipe the system utilizes acoustic based system. The measure of sand creation which is measured by examining the effect brought on because of the striking of sand on the dividers of pipe. The sand gathering rate is measured in gram/sec. The disintegration based strategy utilized as a part of the framework is to investigate the divergence in the insubordination as stream of oil goes from the sensor based funnels. To store the uniqueness in the disobedience of the components (examining) which was brought about in light of the diminishing in their width because of sand disintegration.This framework examinations straightforwardly the particles and not delicate to the clamour[1, 2].

For the sand dissecting system has two strategies yet both have a few inadequacies. In acoustic based framework, as it is inhumane to temperature so it can't achieve the genuine time dissecting, as here the data is gathered at MHz level and data is handled utilizing signal preparing device. Encourage, in framework which depends on disintegration, that framework is unmanageable for the long keep running as it is very delicate to the temperature and precision. The consistent handling of the data is unrealistic because of the huge accumulated dataand which is to be prepared in a short interim of time. The acoustic based framework is affected by the ecological commotion as wind blow and rain drops, operation of compressors and pumps. This business investigating framework brings about the imperfect sand location brought about by close-by unsettling influences in the field, advancing the false ready.

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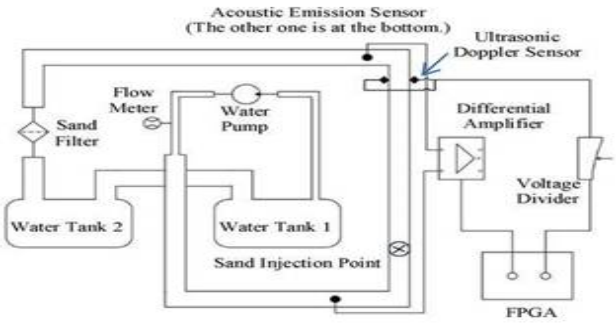

Fig.1. Sand Monitoring System[1]

The field programmable entryway exhibit (FPGA) is profoundly reconfigurable and quick, permitting fast prototyping of new strategies and direct the framework for appraisal and real world applications. It is actualized for such a broad utilization of infinite impulse response (IIR) channel application, ionizing radiation discovery , and vibrational studies for modern applications for ecological mindfulness , among others[3]-[5]. To effortlessly coordinate the modules, a FPGA based outline is utilized for a compelling framework, used to grasp the data handling utilized by different control and dissecting framework. To direct the control and examining for different applications coordinated frameworks in light of FPGA are utilized, for example, reconfiguration and blame recognition for power electronic converters , data securing and breaking down for multichannel frameworks, investigation and dissecting of wavelet bundles[6, 7].

II.DISTRIBUTED ARITHMETIC ALGORITHM

Distributed Arithmetic (DA) is a slow technique due to its bitserial nature. When the number of vector elements is somewhat same as of wordsize, DA is very fast, as it `places'ROM look-ups over the explicit multiplications, which is an efficient technique for the implementation of Field Programmable Gate Arrays (FPGAs). In DA, multiplications are rearranged and mixed such that, the arithmetic becomes "distributed" through the structure rather than being "lumped" Area savings from using DA can be up to 80% in DSP hardware designs. While distributed arithmetic technique itself has been around for more than 30 years, interest in this has been invigorated by the use of Field Programmable Gate Arrays (FPGAs) for DSP because of DA implementation in FPGAs, one can exploit memory in FPGAs to execute the MAC operation [8, 9].

DA based algorithm is used when long convolution and large order filter is to implemented. In various convolutions one input is sample and another is fixed. The DSP algorithm uses DA computation for digital convolution. In this method it saves the pre-calculated results in the memory element so as to produce quicker outputs as compare to multiplier- accumulator based design. But memory requirement is increased with increase in convolution order. Due to the systolic decomposition scheme for the DA computation it provides area time trade off because due to smaller address length the memory size is reduced but complexity and latency is increased[10].

Distributed algorithm is used for the realisation of FIR and IIR filter. It performs dot product and weighted sum of products operations. It is a influential tool for FPGA design because it reduces the size of parallel hardware multiply – accumulate. The constant coefficient of FIR filter are stored in Look-up-table in DA algorithm .2^k is the size of look up table filter tap is indicated by k , due to increase in filter taps number LUT size also increases offset binary code(OBC) is used to reduce the size of LUT. In many Applications MAC(Multiplier and Accumulator) based FIR filter is used but in DA based method MAC is replaced by LUT causes power and area efficiency. Using DA based method multiplier fewer Filters is designed using FPGA. Distributed arithmetic computation is bit serial, it replaces multiply and accumulate operations by set of addition along with shifting operations. The fundamental operations required are a series of look-up tables, subtraction, additions and shifts of the input data sequence. all possible partial products are stored in the Look Up Table (LUT) over the filter coefficient space[11].

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Field Programmable Gate Array: It is a coordinated circuit which is utilized by the prerequisite of the client. FPGAs execution in different fields and its proficiency makes it appropriate for operable in different fields.It can join million numbers of doors, memory squares and DSP units. Its simple programming makes it dependable for the use. It underpins parallelism because of which many number of procedures should be possible at the same time. An opportunity to-showcase is diminished which is thought to be its greatest accomplishment. FPGA can be customized utilizing the VERILOG Language and HDL Language for the specific applications. In FPGA, its throughput limit is high as contrast with the traditional processors like DSP and its acknowledgment cost is additionally less. FPGA likewise contains different pieces like ALUfor the AND and XOR operation, flip-flops as memory elements, interconnections using wires, logic blocks. Soft Microprocessor can be implemented by FPGA like Altera Nios II and Xilinx Micro blaze. FPGA can also be used as controlling device and A/D conversion control module, synchronization and modulating signal generation module [12].

III. FIR FILTER DESIGN SIMULATION

Generally digitals filters can be implemented using two methods: Finite Impulse Response(FIR) and Infinite Impulse Response(IIR). FIR filters are generally non-recursive in nature, of the form

$$y(n)=h(0)x(n) + h(1)x(n-\mathbf{1)} +\ldots+ \mathbf{h(n}-1)x(1) + h(n)x(0) \qquad (1)$$

Fir filter is generally stable and its phase can be exactly linear.

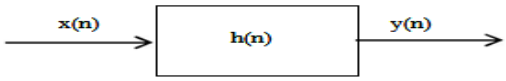

Figure 2: Block Diagram of FIR filter.

FIR is generally BIBO (**"**bounded-input, bounded-output**"**) stable[12].In FIR filter no nonzero pole exist in the transfer function. It is simple to realize and can be intended to have linear phase property but on the other hand IIR filter is recursive in nature and sometimes not stable. In IIR filter nonzero pole exists in the transfer function and Lowers the filter order than a FIR filter. It generally has nonlinear phase property.

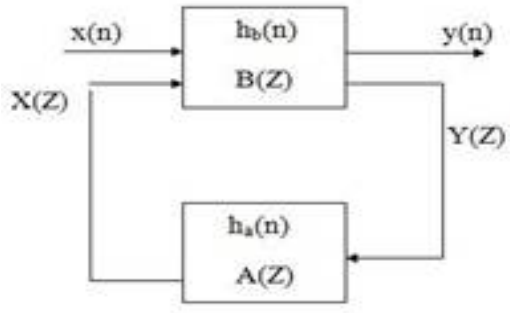

Fig 3: Block diagram of IIR Filter.

The filter which is to be designed in the paper is FIR band stop filter implemented on Kaiser Window having Filter Order 78 **and Shape Parameter(β) given as 3.872, Sampling**
Frequency(F_s)is given as 1200 kHz and first cut off frequency is 510 kHz and other cut off frequency is 550 kHz.

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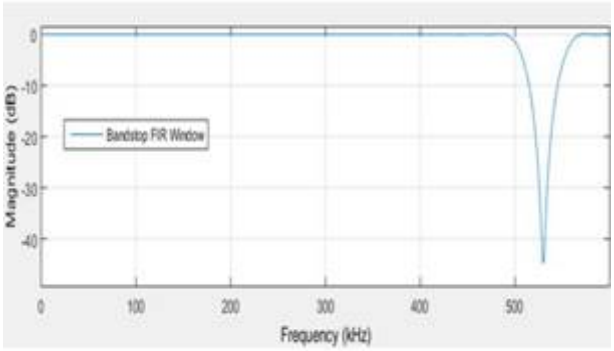

Fig. 4: Magnitude Response of FIR Filter

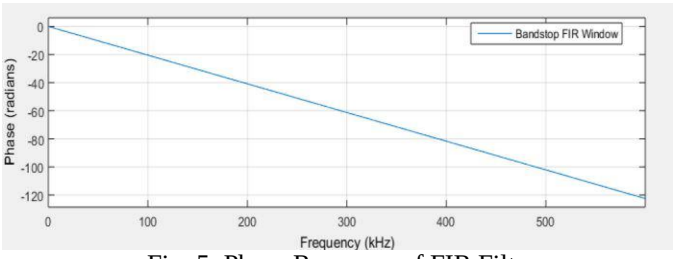

Fig. 5: Phase Response of FIR Filter

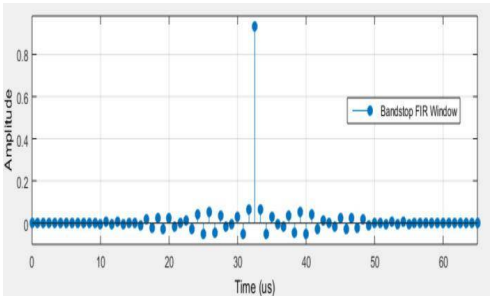

Fig. 6: Impulse Response of FIR Filter

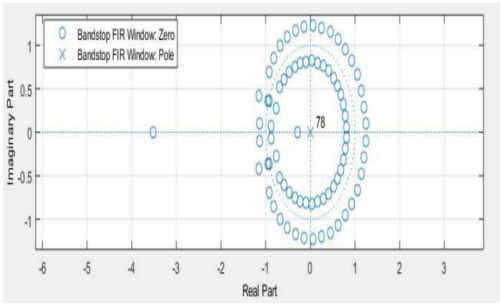

Fig. 7: Pole-Zero Response of FIR Filter

IV.HARDWARE SYNTHESIS

For better results, proper selection of methodology is required. The selection of parameters and the architecture used plays a vital role in designing. The hardware can be synthesized in various ways like by using different architecture like fully parallel, fully serial, DA, etc and by varying different parameters of the filter o be designed. In this paper, system is using DA, fully parallel and fully serial architecture for the designing of filter.

Distributive Arithmetic: Distributed Arithmetic (DA) is aslow technique due to its bit serial nature. When the number of vector elements is somewhat same as of word size[11], DA is very fast, as it `places' ROM look-ups over the explicit multiplications, which is an efficient technique for the implementation of Field Programmable Gate Arrays (FPGAs). In DA, multiplications are rearranged and mixed such that, the arithmetic becomes **"**distributed**"** through the structure rather than being **"**lumped**" „** Area savings from using DA can be up to 80% in DSP hardware designs **„** While distributed arithmetic technique itself has been around for more than 30years, interest in this has been

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invigorated by the use of Field Programmable Gate Arrays (FPGAs) for DSP **„** because of DA implementation in FPGAs, one can exploit memory in FPGAs to execute the MAC operation [14].
DA based algorithm is used when long convolution and large order filter is to implemented

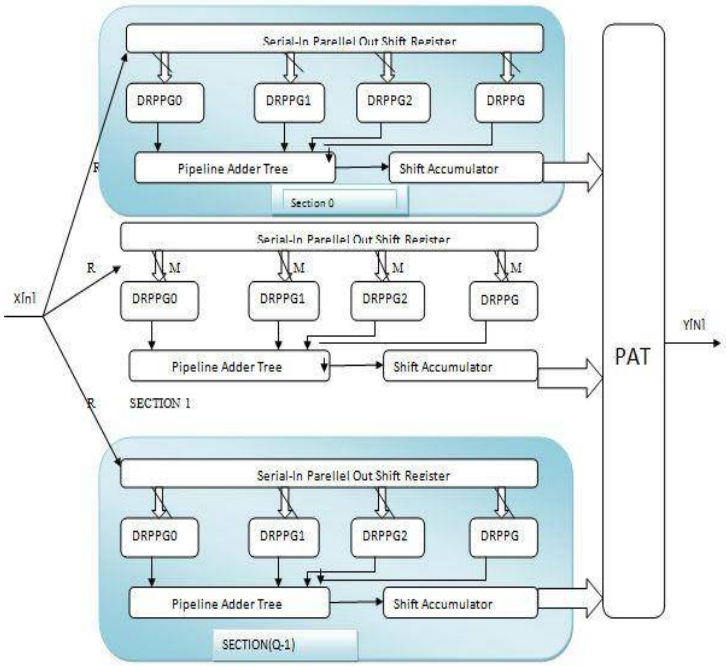

Fig.8: DA Algorithm for FIR Filter[14]

Fully Parallel FIR filter design: In fully parallel architecture,it is basically designed fr the cost effective circuits having smaller filter order, which in turns requires less number of multipliers to carry out the equation of filter[14,15].
Mathematically, the transfer function is given by:

$$\mathbf{H(z) = C + \sum H_k(z)} \qquad (2)$$

(Summation varies from n=1 to k.)
In equation (2), it is generally the basic equation representation of the FIR filter. The k in the above equation is the integer part of (N+1)/2.
The fully parallel architectures are basically used for high speed operable filter designing.

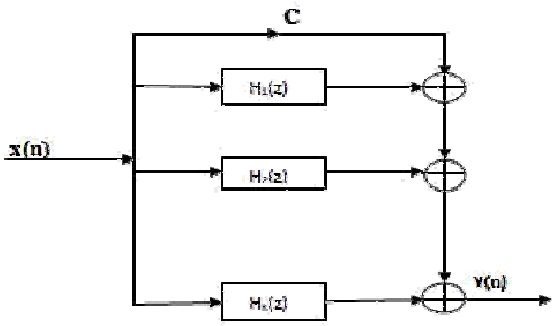

Fig. 9: Parallel-Form of IIR filter

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Fully serial: In fully serial architecture, it is very simple forimplementation purpose, as in this architecture the output of one stage becomes the input of next stage[17, 18].

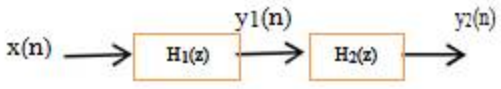

Fig. 10: Serial form of FIR filter

The fully serial architecture is quite slow in nature as it follows step wise operation.
The design is realized on Xilinx Spartan 3AN XC700AN device of FPGA in Verilog Language. On the basis of figure 12 comparison the speed of different architecture as frequency of DA architecture is more than fully serial and fully parallel architecture. In figure 10 there is a comparison of number of slices flip-flop used and number of LUTs used is depicted between DA, Fully Serial and Fully Parallel Architecture.

V. RESULTS

Table 1. Utilization Table

Resources	Fully serial	Fully parallel	DA
No of slice ff	557	1166	3018
4 input LUTs	344	784	4963
Bonded IOBs	28	28	52
MULT 18x18 SIOs	1/20	20/20	-
Frequency	74.478MHz	124.331MHz	136.049MHz

Table 1

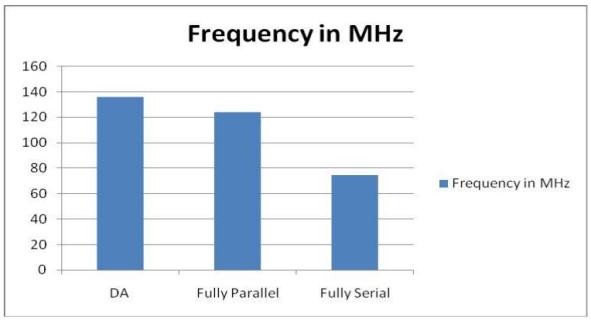

Fig. 11: Speed Comparison of different architecture

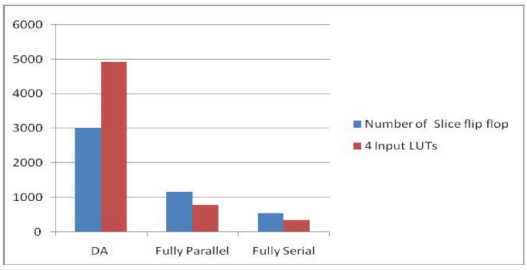

Fig.12: Resource Comparison different architectures

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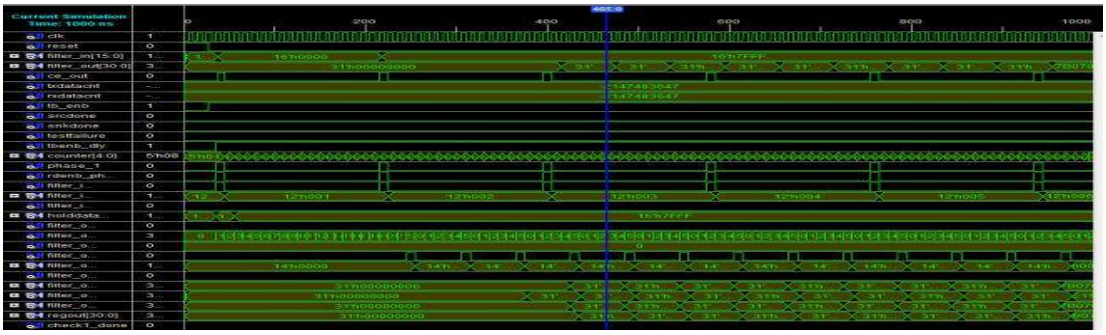

Fig. 13: Input Waveform for DA architecture

VI.CONCLUSION

The proposed method compares fully serial, fully parallel and DA architecture and found that the DA based filter is more speedy in terms of frequency (136.049MHz) and also uses multiplier less feature. The DA architecture also utilizes less time for the operation i.e. 7.350ns. In case of fully serial architecture the number of LUTs required will be less and also number of slice flipflop requires is smallest in fully serial architecture as compared to DA. Area efficiency will be high using fully serial method but speed of operation is less. This proposed filter is used in high accuracy measurement of sand production system.

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