ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 4, April 2017

Design & Post Layout Simulations of Low Power CMOS Cell Structure Based on Energy Efficient Adiabatic Logic

Kamlesh Kumar Dwivedi[1], Virendra Kumar Yadav[2], Dr.Kulbhushan Gupta[3]

Assistant Professor, Dept. of ECE, Madhu Vachaspati Institute of Engineering & Technology, Allahabad, India[1]

PG Student [VLSI], Dept. of ECE, Shambhunath Institute of Engineering & Technology, Allahabad, India[2]

Director, Madhu Vachaspati Institute of Engineering & Technology, Allahabad, India[3]

ABSTRACT: The number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Then, to limit the power dissipation, alternative solutions at each level of abstraction are proposed.

This paper work demonstrates the low power dissipation of Adiabatic Logic by presenting the results of designing various design/ cell units employing Adiabatic Logic circuit techniques. A family of full-custom conventional CMOS Logic and an Adiabatic Logic units for example, an inverter, a two-input NAND gate , a two-input NOR gate etc, were designed in Mentor Graphics IC Design Architect using standard **TSMC 0.35 *μm* technology**, laid out in Mentor Graphics IC Station.

All the circuit simulations has been done using various schematics of the structures and post-layout simulations are also being done after they all have been laid-out by considering all the basic design rules and by running the LVS program. Finally, the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done to show the amount of power dissipated by the two logic families.

KEYWORDS: Adiabatic logic, Energy Efficient, Low power, CMOS Inverter, CMOS NAND Gate, Power Dissipation.

I. INTRODUCTION

The primary goal of this paper is to demonstrate a circuit level design approach, for use in designs which demand extreme low power dissipation.

This paper is divided into four sections. Section I deals the introduction part. Section II explains the Physical Layout Design and Post Layout Design Simulations. In section III discusses about Design and analysis of low power CMOS cell design. Conclusion is given in the section IV.

Why Low Power Circuits Design is Important?

Thanks to integrated circuit technology, electronic devices have greatly decreased in size and mass over the past few decades. Most of us routinely carry or wear electronics every day. While VLSI (Very Large Scale Integration) technology, particularly CMOS, has enjoyed the rapid exponential growth characterized by Moore's Law, energy storage technology (mainly batteries) has grown much more slowly.

Power dissipation in CMOS device:

CMOS is the logic family preferred in many designs due to following reasons: - (a) Impeccable noise margins. (b) Perfect logic levels. (c) Negligible static power dissipation. (d) Gives good performance in most cases. (e) Easy to get a

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 4, April 2017

functional circuits. (f) Lot of tools available to automate the design process. There are different types of power dissipation in CMOS.

1. **Static Power Dissipation:** Static power dissipation can however result from degenerated voltage levels at the inputs to static gates. Bus contention, signal conflicts due to multiple drivers, leakage current drawn continuously from the power supply also result in static power dissipation.
2. **Dynamic Power Dissipation:** Dynamic power dissipation is caused by charging and discharging of capacitances. The charging process draws energy equal to $C_{VDD}2$ from the power supply. Half of this is dissipated immediately in the PMOS transistors and the interconnect, while the other half is stored on the load capacitance
3. **Short Circuit Power Dissipation**: It is caused by the flow of short circuit current between supply and ground during switching or transition in signal values when NMOS and PMOS both on.

Principle of Adiabatic Circuits:

The term "adiabatic" refers to a thermodynamic process that exchanges no energy with the environment, and hence no energy or power dissipation occurs. Adiabatic technology is used to reduce the power or energy dissipation during the switching process and further reuse some of the energy by recycling it from the load capacitance. For reusing the energy, the adiabatic circuit uses the principle of Constant current source power supply. For reducing power dissipation it uses the principle of Trapezoidal or sinusoidal power supply voltage.

Different Adiabatic Logic Families:

Practical adiabatic families can be classified as either partially adiabatic or fully adiabatic. In Partially adiabatic circuits, some charge is allowed to be transferred to the ground, while in a fully adiabatic circuits, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization.
Popular Partially Adiabatic families include the following:

(a) Efficient Charge Recovery Logic (ECRL).
(b) 2N-2N2P Adiabatic Logic.
(c) Positive Feedback Adiabatic Logic (PFAL).
(d) NMOS Energy Recovery Logic (NERL).
(e) Clocked Adiabatic Logic (CAL).
(f) True Single-Phase Adiabatic Logic (TSEL).
(g) Source-coupled Adiabatic Logic (SCAL).

Some Fully adiabatic logic families include:

(a) Pass Transistor Adiabatic Logic (PAL).
(b) Split- Rail Charge Recovery Logic (SCRL).

II. PHYSICAL LAYOUT DESIGN AND POST LAYOUT DESIGN

This chapter discusses the designs of different layouts for all the proposed structures, which are designed in Mentor Graphics IC Station **TSMC 0.35 micron Technology** and the **Layout versus Schematic (LVS)** program was executed to perform a comparison of the schematic to the physical layout.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 4, April 2017

Layout versus schematic (LVS) design rules:

The Layout Versus Schematic (LVS) is the class of electronic design automation (EDA) verification software that determines whether a particular integrated circuit layout corresponds to the original schematic of circuit diagram of the design.

A successful Design rule check (DRC) ensures that the layout conforms to the rules designed / required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is where an LVS check is used. LVS checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. The software then compares them with the schematic or circuit diagram. In most cases the layout will not pass LVS the first time requiring the layout engineer to examine the LVS software's reports and make changes to the layout.

Post-Layout Design:

Post layout simulation is mainly used to verify the complete design. It verifies all design constraints after their creation. Post layout simulation also comes in handy when comparing simulation versus measurements. This is important to ensure that the constraints created by Pre layout simulation are based on sound modelling of the PCB.

Difference between Physical layout and Post layout:

The main difference between physical layout and post layout is that pre layout simulations takes place before completing the PCB layout, while post layout simulations use the complete PCB layout as their basis.
In pre layout and post layout, we translate physical parameters in to circuit elements and other mathematical models for simulation. However, for physical layout simulation, we must build up a circuit schematic to include all elements of the simulation. Post layout simulation involves extraction of physical information from the routed board.

III. DESIGN AND ANALYSIS OF LOW POWER CMOS CELL STRUCTURES:

(A) Design and simulation for a CMOS Inverter:

The first basic cell which the VLSI designers implements and analyse is the basic CMOS Inverter. Here also this paper work starts with the designing of the basic CMOS Inverter of minimum transistor size. The standard TSMC 0.35 μm CMOS technologies have been used and a load capacitance of 4 fF is used. The transient analysis is done by use of the ELDO Simulator of Mentor Graphics Corporation. The basic structure of a CMOS Inverter is shown in Figure below

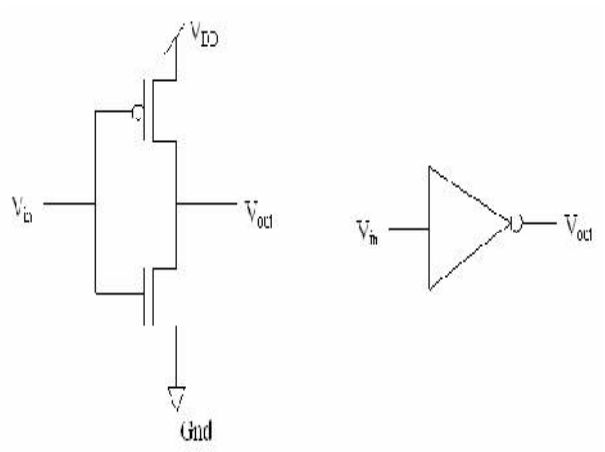

Figure 1. Basic Structure of CMOS Inverter.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 4, April 2017

The transient simulation results are as shown in the Figure -2 below.

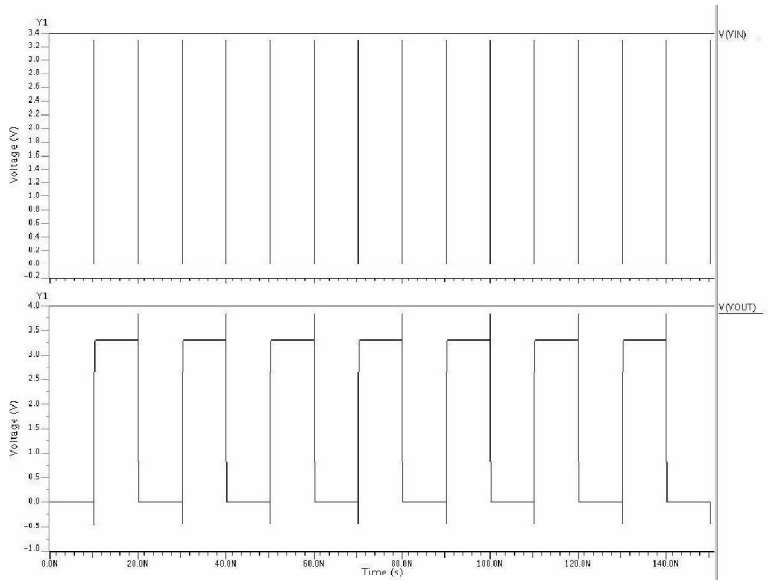

Figure 2. Simulation Results of CMOS Inverter:
(a) Input Signal,
(b) Voltage Waveform of Output Signal

LAYOUT CELL DESIGN OF A CMOS INVERTER AS SHOW IN FIGURE 3:

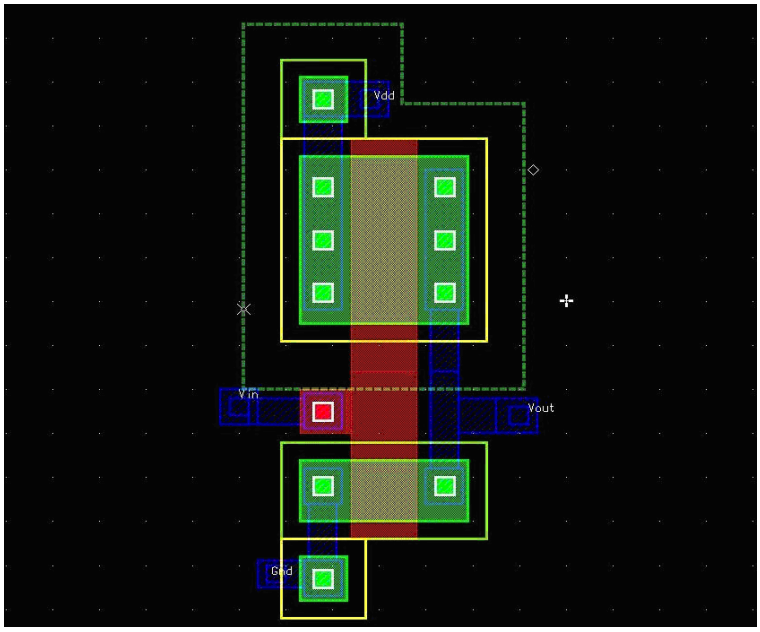

Figure 3. Layout of CMOS Inverter.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 4, April 2017

Figure 4, below shows the post-layout result of the transient analysis for an adiabatic inverter.

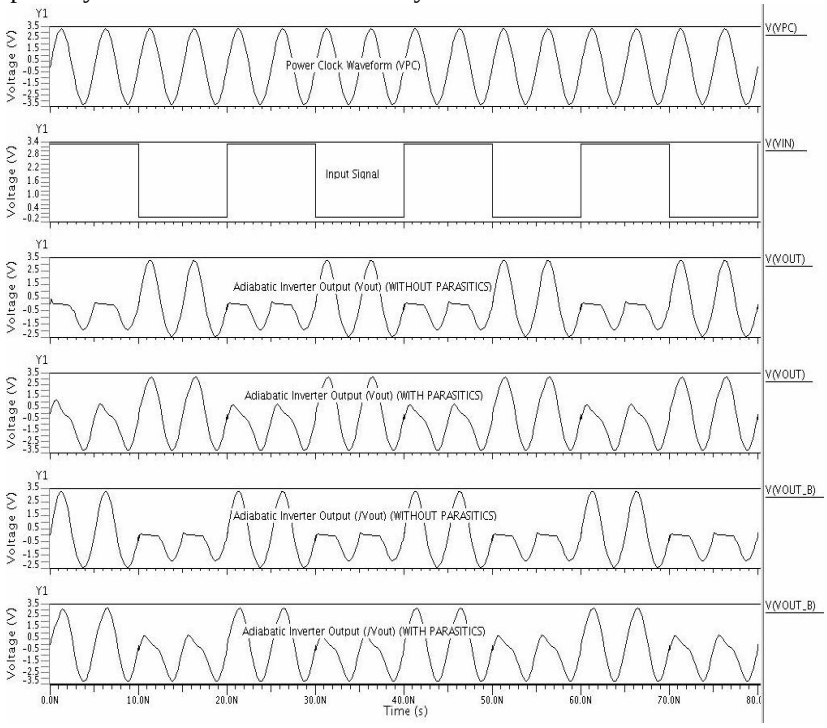

Figure 4. Post Layout Simulation – Transient Analysis for an Adiabatic Inverter.

(B) Design and simulation for a CMOS NAND gate:

The next basic cell to consider is the CMOS-based Two-Input NAND Gate, designed and simulated in the standard TSMC 0.35 μm CMOS Technology and with a load capacitance of 5 fF. The minimum sized NMOS and PMOS transistors have been used for the transient simulations.

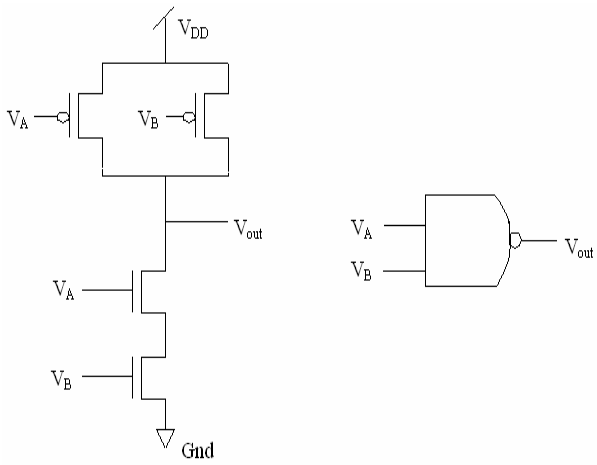

Figure 5. Basic Structure of a Two-Input CMOS NAND Gate.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 4, April 2017

The transient simulation results are as shown in the Figure 6, below.

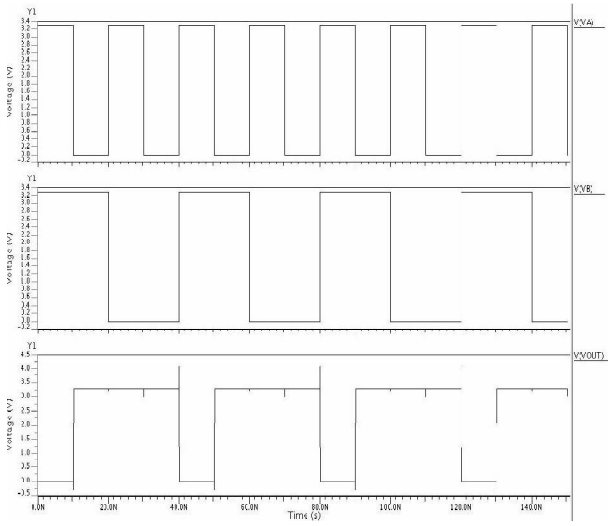

Figure 6. Simulation Results of Two-Input CMOS NAND Gate:
(a) Input Signal (VA),
(b) Input Signal (VB),
(c) Voltage Waveform of Output Signal (NAND Output).

LAYOUT CELL DESIGN OF A CMOS NAND GATE AS SHOW IN FIGURE 7:

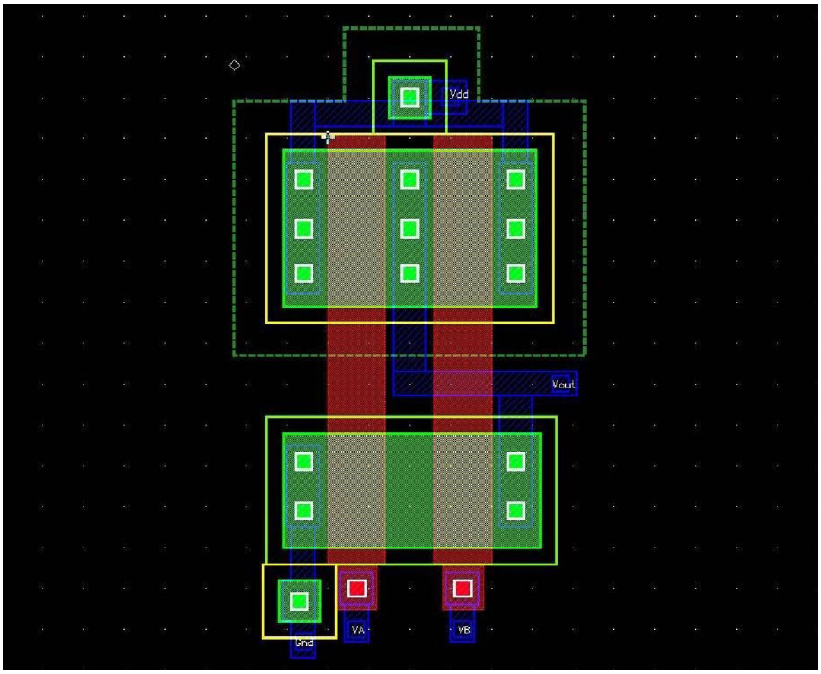

Figure 7. Layout of Two- Input CMOS NAND gate

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 4, April 2017

Figure 8, below shows the post-layout result of the transient analysis for an Adiabatic CMOS NAND Gate.

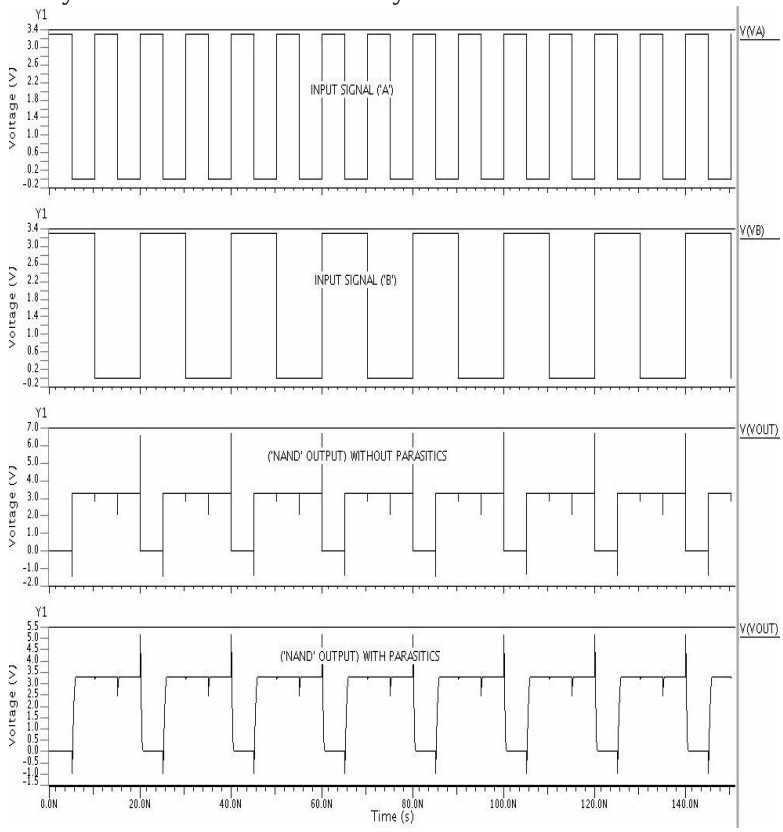

Figure 8. Post Layout Simulation – Transient Analysis for a Two-Input CMOS NAND Gate.

IV. CONCLUSION

This paper was focused on the design of low power CMOS cell structures, which is the main contribution of this work. The design of low power CMOS cell structures uses fully complementary CMOS logic style and an adiabatic PFAL logic style. The basic principle behind implementing various design units in the two logic styles is to compare them with reference to the average power dissipated by all of them.

The analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done. It was found that the adiabatic PFAL logic style is advantageous in applications where power reduction is of prime importance as in high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of adiabatic logic, the energy savings of up to 76 % to 90 % can be reached.

Circuit simulations show that the adiabatic design units can save energy by a factor of 10 at 50 MHz and about 2 at 250 MHz, as compared to logically equivalent conventional CMOS implementation.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 4, April 2017

REFERENCES

[1] N.Anuar, Y. Takahashi, T. Sekine, "Adiabatic logic versus CMOS for low power application" IEEE, Proc.ITC-CSCC2009, july2009, pp.302-305.
[2] Gaurav Singh, Ravi Kumar, Manoj Kumar Sharma, "Comparative Analysis of Conventional CMOS and Energy Efficient Adiabatic Logic Circuits" IJETAE, Volume3, Issue9, September2013
[3] Mukesh Tiwari, Jai Karan Singh, Yashasvi Vaidhya, " Adiabatic Positive Feedback Charge Recovery Logic For Low Power CMOS Design" IJCTEE, Volume2, Issue5, October 2012
[4] Anamika Mishra, Anju Jaiswal, A. Jaiswal, A.K.Niketa "Design and Analysis of Conventional CMOS and Energy Efficient Adiabatic Logic for Low Power VLSI Application" IJEAT, Volume3, Issue 12, May 2014
[5] P .Vijayasalini. Nirmal Kumar, S.P Dhivya "Design and analysis of Low power Multiplier and 4:2 Compressor Using Adiabatic Logic", IJETAE, Volume3, Issue1, Januery2013.
[6] B.Dilli Kumar. Bharathi, "Design of Energy Efficient Arithmetic Circuits Using Charge Recovery Adiabatic Logic" IJEATAT, volume4, issue1-2013.
[7] M. Sowjanya, S.Abdul Malik, "Efficiency of Adiabatic Logic for Low power VLSI Using Cascaded ECRL and PFAL Inverter "IJERAA, Vlume3, Issue4, Jul Aug2013.
[8]Samik Samanta, Member of IEEE "Power Efficient VLSI Inverter Design Using Adiabatic Logic and Estimation of Power Dissipation using VLSI-EDA Tool "IJCCT Volume2, Issue2, 3, 4, 2010.
[9]Shipra Upadhyay, RA Mishra, RK Nagaria, SP Singh and Amit Shukla, "Triangular Power Supply Based Adiabatic Logic Family" WASJ, IDOSI, 2013.
[10]J. M. RABAEY, AND M. PEDRAM, "Low Power Design Methodologies, "Kluwer Academic Publishers, 2002
[11]H. J. M. VEENDRICK, "Short-circuit Dissipation of Static CMOS Circuitry andits Impact on the Design of Buffer Circuits,"IEEE JSSC, pp. 468-473, August 1984
[12]A. Chandrakasan, S. Sheng and R. Brodersen, (1992)"Low-power CMOS digital design," IEEE Journal of Solid State Circuits, Vol. 27.
[13]Maksimovic D., Oklobdzija V.G., Nikolic B., Current K.W., "Clocked CMOS adiabatic logic with integrated single phase power clock supply". IEEE Transaction on very large scale integration system, 2000, 8,(4), pp.460-463.
[14]Kramer A.Denker J.S., Flower B., Moroney J., "Second-order adiabatic computation with 2N-2P and 2N-2N-2P logic circuit". Proc. Intern. Symp. Low power design, 1995, pp. 191-196
[15] Hu Jianping; Cen Lizhang; Liu Xiao; "A new type of low power adiabatic circuit with complementary pass-transistor logic" ASIC, 2003. Proc. 5th international Conference on Vol.2, Oct.2003, pp.1235-1238