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Prediction of Ventricular Arrhythmia for ECG System Using FPGA

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ABSTRACT: In this paper quadratic spline wavelet(QSW) method is used to remove the noise from the ECG signal. Ripple carry adder and array multiplier are used in QSW.ECG signal is generated by using MATLAB. In existing method ventricular arrhythmia could be predicted by using unique set of ECG featuers and naive bayes classifier. The PQRST wave were investigated to obtain the fiducial point. The proposed method is used to predict the ventricular arrhythmia before its occurrence using low power based ECG processor. An ECG-based processor that is used for the prediction of ventricular arrhythmia will detect the features of the ECG and detects the arrhythmia. Observations are verified by simulating QSW program using QUARTUS II(9.1) tool. The main aim of this project is to reduce the power consumption and time. The total power dissipation of quadratic spline wavelet block is 105.28mW.

KEYWORDS: Quadratic Spline Wavelet (QSW); Electro cardio Gram(ECG); PQRST; QUARTUS; MATLAB.

I. INTRODUCTION

The ECG signal is one of the most widely used diagnostic tools in clinical medicine[1, 2]. In embedded system due to advancement, portable instruments are used for ECG rhythm monitoring, diagnosis and heart beat classification with more complex digital signal processing (DSP) algorithms [3]. In USA per year 300000 death occurs, due to sudden cardiac arrest and it leads to ventricular arrhythmias including ventricular tachycardia(VT) or ventricular fibrillation(VF) [4]. Ventricular arrhythmia is said to be an abnormal ECG waveform and its lead to 75%-85% of sudden death in persons who suffer from heart diseases [4]. In most cases, ventricular arrhythmias are occurred by hupertension, coronary heart disease or cardiomyopathy and if not properly treated immediate death occurs [5].

VT is a fast rhythm which occurs more than three consecutive heart beat originating from the ventricles approximately at a rate above 100 beats/min [6]. VF is another kind of rhythm originating from the ventricles differentiated by disorganized process of ventricles which leads to improper blood circulation, degeneration of ECG signal indicates no electrical activity of heart or even into a pulseless flat ECG signal. The best prediction against sudden death from ventricular arrhythmia is impalantable cardioverter defibrillator. Normal standard diagnosis method for ventricular arrhythmia is monitoring ECG signal for long time. The onset of ventricular arrhythmia can be predicted by extracting information about different P-QRS-T waves which includes amplitude, waveform morphologies and intervals. Even small noise in ECG signal can robust the entire system. There are various methods are used for the noise filtering. In this paper quadrature spline wavelet (QSW) is used. QSW remove noise from the

ECG signal by using delay element ,ripple carry adder,array multiplier and shift registers. In general, ECG signal is measured from the body surface through electrodes which produces voltage due to the electrical activity of the heart. ECG signal is commonly characterized by intervals, waves(P,Q,R,S and T) and segments. The waves Q,R and S are called as QRS complex. In 12-lead ECG, each individual lead indicates different view of a single ECG waveform[7][8].



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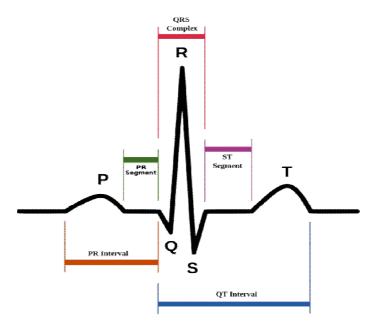


Figure 1. ECG Signal

If any cardiac pathology is absent, then ST-segment will be at the same level of the PR-segment. The elevation of the ST-segment cause infraction or ischemia. The practical technique for monitoring ischemia is continuous analysis of ST-segment deviations[7][9].

II. LITERATURE REVIEW

For detection of ventricular fibrillation J Pardey [10] presented a technique using binary sequences. To obtain the threshold crossing interval binary sequences are used. The combination of Lempel-Ziv complexity measurement and threshold crossing interval are given as the input to the neural network classifier.

Bo-Yu Shiu, et al [11] introduces a low-power low-noise ECG acquisition system for identifying heart disorders. The ECG signal is obtained along with an analog front-end circuit and offset and also baseline drift is eliminated simultaneously. The digital signal processing (DSP) unit is used to eliminate the ECG interferences. ST segment also used to identify the heart disorders. The ECG front end chip has been fabricated using CMOS TSMC 90nm technology. The total power consumed was 40.3μ W. DSP algorithms are implemented in FPGA kit. The obtained results indicates that the specificity and sensitivity of ST segment after eliminating EMG is 93.1% and 96.6% respectively.

Shuenn-Yuh Lee, et.al [12] proposed a classification system and a low-power bio signal acquisition for body sensor networks. It consists of three main classification:1) a signal digitization and acquisition—using a high pass delta modulator based biosignal processor(BSP), 2) short range wireless transmission using a low power super-regenerative on-off keying transceiver, 3) electrocardiogram (ECG) classification using digital signal processor (DSP). The DSP and transmitter circuits act as a body-end circuits, operated by using two 605 mAH zinc-air batteries for over 80 days and the total power consumption is $586.5 \mu W$. RF receiver and digital signal processoe act as a receiver-end circuits which can be integrated with personal computers or mobile phones and the power consumption should be less than 1mW. By using diagnosis control and digital signal processing based on wavelet transform ,the percentage of ECG classification and heart beat detection are near to 97.25% and 99.44% respectively. In this chips are fabricated in CMOS process with TSMC 0.18 μ m standard.

Jiapu Pan and Willis J. Tompkins [13] proposed an algorithm for detection of the QRS complex in ECG signal. In general QRS complexes depends on the amplitude, slope, and width. The false detection in ECG signal due to different types of interferences can be eliminated by using digital band pass filter. This filtering allow to use of low threshold and hence it also increasing the detection sensitivity. If changes occurs in heart rate and QRS morphology then this



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algorithm automatically changes the threshold and parameters periodically. This algorithm accurately detects 99.3% of the QRS complexes for standard 24 h MIT/BIH arrhythmia database.

III. EXISTING METHOD

In existing method unlike other system, it aims to develop an ECG signal, processing and analysing on the same single chip itself. The comparison of normal method existing method is shown in the following fig2.

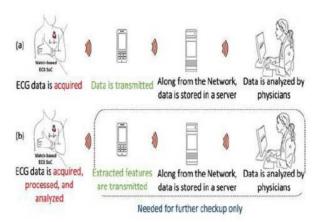


Figure 2. comparison between (a) normally implemented method (b) existing method

The existing system consists of three parts which includes preprocessing, feature extraction, and classification as shown in Fig. 3. In the preprocessing stage, it performs three process: 1) filtering of ECG signal; 2) detecting QRS complex; 3) delineation of T and P waves. The noise along with the ECG signal is removed by ECG filtering and used for further processing. Afterwords, Pan and Tompkins (PAT) algorithm is used for the QRS complex detection [13].

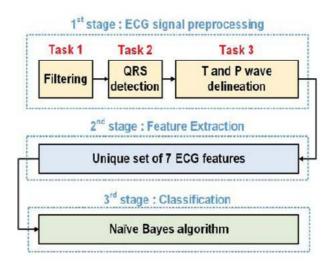


Figure 3. Existing ventricular arrhythmia prediction system

The fiducial points such as P onset, P peak, P offset, T onset, T peak, and T offset corresponding to T and P waves were delineated. To obtain the fiducial points exactly ,adaptive search windows and thresholds were used.



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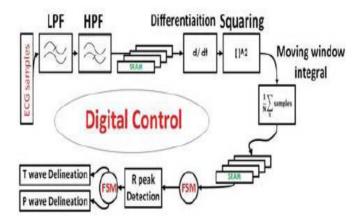


Figure 4. Block diagram of preprocessing stage, that includes filtering, QRS detection, and P and T wave delineation.

In preprocessing ,the ECG signal is filtered to remove low frequency characteristics of P and T waves, interference from power lines, baseline drift and high frequency attenuated with electromyographic noise. To detect the QRS complex PAT algorithm is used.PAT algorithm is based on amplitude threshold method which defines the fact that R peak have higher amplitude than the other ECG peaks [13]. This PAT algorithm is capable of extracting R peak in each heart beat .T and P waves were delineated by using adaptive search windows and adaptive threshold inorder to extract them accurately from noise peak.

Al	Algorithm 1 Training Gaussian Naive Bayes Classifier 1: procedure TrainNaiveBayes		
1:			
2:	$X \leftarrow \text{Extract Feature}$		
3:	$N \leftarrow Count \ Values$		
4:	for each $c \in Class$		
5:	do $N_c \leftarrow$ Count Values in c		
6:	prior [c] $\leftarrow \frac{N_c}{N}$		
7:	do $\mu \leftarrow \sum\limits_{i=1}^{N_c} (X_i)$		
8:	$\mathbf{do} \ \sigma^2 \leftarrow \frac{1}{N_c} \sum_{i=1}^{N_c} (X_i - \mu)^2$		
9:			
0:	do condprob $[v][c] \leftarrow LUT$		
1:	return prior, condprob		



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Algorithm 2 Testing Gaussian Naive Bayes Classifier 1: procedure TESTNAIVEBAYES (PRIOR, CONDPROB) 2: Z ← Extract Feature 3: for each c ∈ Class 4: do c = condprob [c][Z] ← LUT 5: return argmax c

The existing method predicts the ventricular arrhythmia 3h before its onset.

IV. PROPOSED SYSTEM

In proposed system to remove noise from the ECG signal ,a noise-tolerant algorithm using a combination of both template matching approach and short-term autocorrelation. The proposed method is implemented in hardware to obtain both low power consumption and noise tolerance.

Heartbeat Detection Algorithms

The general approach for determining R peak is R- wave with threshold. But nowadays different approaches have been implemented for calculating noise tolerant threshold. In wearable healthcare systems due to noise from muscles and electrode movements, false detection and misdetection will occurs. The noise generation is due to limiting the size and the power consumption of electrodes.

To avoid incorrect detection, template matching and autocorrelation are used because these algorithms use similar waveforms of QRS complex and these algorithm have no threshold calculation. The existing system proposed a short-term autocorrelation (STAC) method for heart rate detection. The proposed system implemented combination of two algorithms such as quadratic spline wavelet (QSW) filter and two-stage STAC based heartbeat detection to remove the noise from the ECG signal.

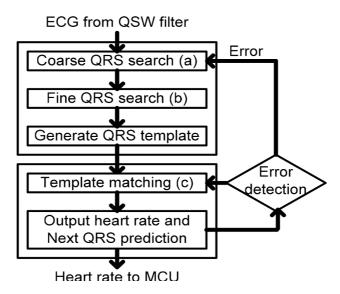


Figure 5. Flow chart of heart beat detection algorithm



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For low power noise reduction in ECG signal ,the most commonly used method is QSW.QSW is capable of eliminating the baseline wander and the hum-noise . But these noise are difficult to remove by using QSW because they have similar frequency range of QRS complex. Therefore to overcome this problem, noise tolerant heart beat detection algorithm is proposed in the next stage.

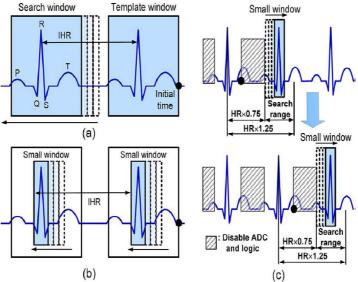


Figure 6. Algorithm overview of coarse-fine QRS template generation and template matching with QRS prediction (a) Coarse QRS search (b) Fine QRS search (c) Template matching.

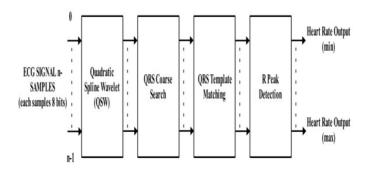


Figure 7.Block diagram of heartbeat detector

A block diagram of heart beat detector is shown in the figure 7, which is implemented in FPGA consisting of various blocks such as summer, subtractor, register, and accumulators. For every time interval four samples (each sample contains 8 bit) enters the block. The bits are subjected to wavelet transform filter for removing of noise. Then the noise removed samples are given as the inputs to the course and fine search blocks where the samples are compared with the QRS template. The R-peaks are detected and heart rate will be analysed. The sampling frequency of the heart beat detector is 360 Hz.



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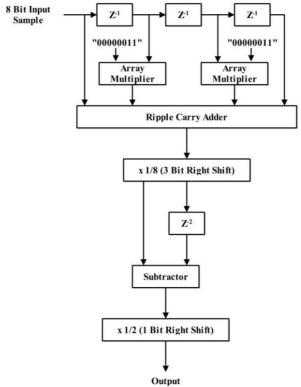


Figure 8. Block diagram of Quadrature Spline Wavelet

V. RESULT AND CONCLUSION

In this project, a fully integrated FPGA based digital unit for the prediction of ventricular arrhythmia that combines a unique set of ECG features is proposed.ECG signal is generated by simulating program using MATLAB.QSW program is simulated to analysis power dissipation , time consumption and removable of noise in ECG signal.

Table 1. Timing Analysis

ТҮРЕ	POWER DISSIPATION
Total thermal power	105.28mW
dissipation	
Core dynamic thermal power	11.17mW
dissipation	
Core static thermal power	47.42mW
dissipation	
I/O thermal power dissipation	46.69mW

Table 2. Power Analysis



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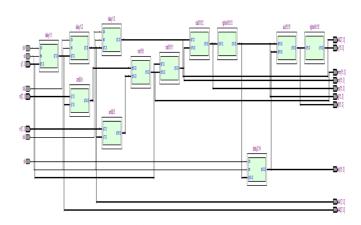


Figure 9. Netlist of Quadrature Spline Wavelet

TYPE	ACTUAL TIME
Worst case clock set up	31.324nS
time(tsu)	
Worst case clock to o/p delay	38.630nS
time(tco)	
Worst case pin to pin delay	41.266nS
time(tpd)	
Worst case threshold(th)	-3.771nS

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