ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

*An ISO 3297: 2007 Certified Organization* *Volume 5, Special Issue 1, March 2016*

National Conference on RecentTrends inElectronics and InstrumentationEngineering (NCRTE 2K16)

1st& 2nd March 2016

Organized by

Department of Electronics &Instrumentation Engineering, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

# Energy Efficient Low Power Fir Filter Using Razor Flip Flop

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**ABSTRACT***:* Energy efficient low power FIR Filter using Razor FlipFlop, which aims to the increase energy efficiency in digital signal processing data paths without loss of robustness.. Timing errors are detected using razor flip-flop on critical paths and it is used to control a dynamic voltage scaling control loop.The FIR filter using razor for every bit and the error bit is generated and one can overcome the error with the filter. The proposed filter can be used for any DSP/ASIC application.The proposed FIR filter is designed using Spice software andthe outcomes are compared with conventional FIR filter to show the significant improvement in its efficiency in terms of Voltage.

**KEYWORDS***:* FIR Filter, Razor Flip Flop, Spice

## I.INTRODUCTION

The fast-growing market of portable systems with thelimited batterylife requires for continued advancedin lowenergydesign. In this paper, we present the novel techniques that exploit special properties of DSP systems to reduce the energyconsumption. In conventional DSPdesigns, as in the other digitaldesign flows, timing correctness of all the operations are guaranteedby construction. Since in many DSP applications the bestquality of signal is not necessary but it is possible totolerate some of timing errors induced by lower *VDD*. If the scaling of roughvoltage can be made possible with only asmall, bounded quality loss and it can be lead to significantly reducedenergy consumption[1][2].

The following no of approaches is used to find DVS in DSP circuits,
Dynamic voltage scaling approach (conventional method)
In situ approach
Algorithmic Noise Tolerance (ANT) approach
Significance driven computation approach

## II.RAZOR FLIP FLOP

The key idea of the Razorwas to purposely operatethe circuit at the sub-critical voltage and reduce the operating voltage by analyzing the errorrate. This eliminates the need for conservative voltage margins. The trade-off would bebetween the power penalties incurred from error correction against the additional powerattained from working at a lower supply voltage[3][4].

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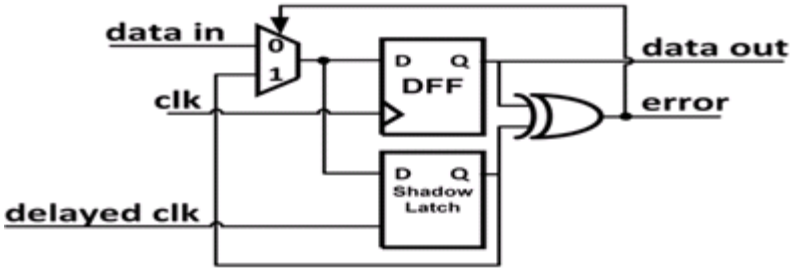


**Fig 1. Razor FlipFlop**

Razor relies a combination of architectural and circuit-level methods for efficient error monitoring and correction of delay path failures. Fig 1 illustrates the concept for thepipeline stage. Socalled the shadow latch, controlled by delayed clock, augments each flipflop in the design. For the given clock pulse, if the combinational logic, meets the setup time for the main flip-flop for the clocks rising edge, then both the main flip-flop andshadow latch was latch the correct data. In Razor, the error signal at the XORgates output remains low, leaving the pipelines operation unaltered. If the combinational logic doesn't complete its computation in time, the main flip-flop will have latch an incorrect value, while the shadow latch will have latch the late-arriving correct value. The error signal would then go high, prompting restoration of the value from the shadow flip-flop latch into the main flip-flop[3][5].The Razor Flip-flop response is given in Fig 2.

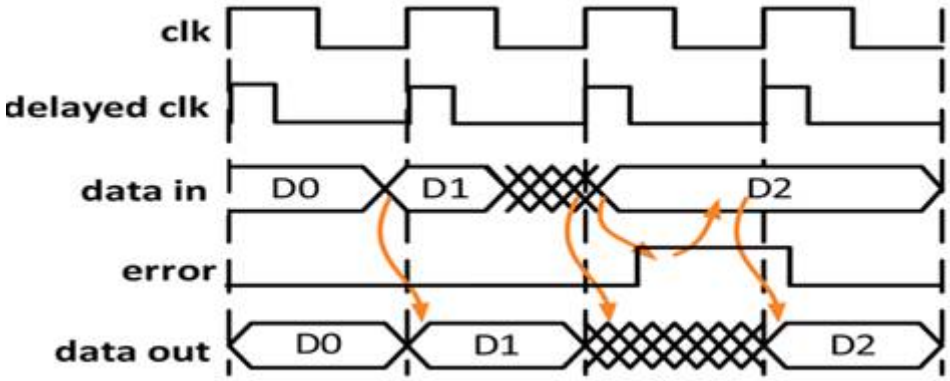


**Fig.2 Razor FlipFlop waveform**

## III.FIR FILTER

"FIR" means "Finite Impulse Response". In Signal processing, a Finite Impulse Response **(FIR)** filter is a filter whose impulse response or response to any finite length inputis finite duration.

In the normal case, the response is finite because there is no feedback in the FIR filter. A poor feedback guarantees the impulse response will be more finite. The FIR filter evaluates an output from a group of input samples. The group of input samples is manifold by a group of coefficients and then added together to generate the output as shown in Fig 3.

FIR filters are a key class of DSP functions. Efficient implementation in terms of silicon area and power consumption can be challenging for high-throughput programmable FIR accelerators, since they require many parallel Multiply-Accumulate (MAC) operations. An FIR filter is usually implemented by using a series of delays, multipliers, and adders to create the filter's output i.e.

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$$y[n] = \sum_{k=-M_1}^{M_2} b_k x[n-k]$$

Where both $M_1$ and $M_2$ are finite.

Theimplementation in software would involve sequential execution of FIR filters permits the filter functions to be processed in the same time that increases processing rate but less supple for changes. Thus, the proposed system offers both the flexibility and capability to create custom high performance systems.[7][8].

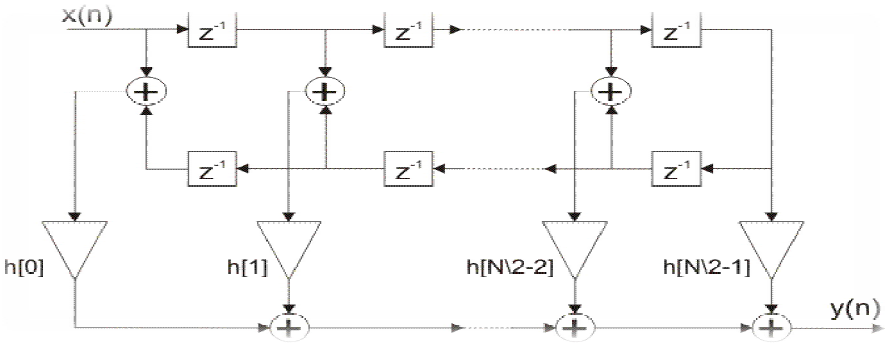


**Fig 3. Linear Phase FIR Filter**

Razor Flip-flops are added in the critical path in FIR Filter which is used to detect the timing error. Our proposed approach adds logic to each pipeline stage such that the individual multiply-accumulate operations, isolated by Razor flip-flop stages, prevent an erroneous tap contribution into the adder chain by bypassing the stage output using a Multiplexer and a delay register.

## IV.RESULT AND DISCUSSION

We have designed Razor Flip Flop in Spice software. In that two D flip flop have been implemented for the design one main Flip Flop and another is shadow flip flop. Shadow flip flop is driven by a delayed clock pulse created using inverter output of main and shadow flip flop is compared using a XOR gate, output of the XOR gate is error signal which is the expected timing delay during the process CLK is the clock pulse, D is the data input to main and shadow flip flop. Q is the output of main flip flop, X is the output of shadow flip flop, ERROR is the expected timing delay. If the output of main and shadow flip flops are identical the XOR will be zero, if outputs are different it gives high output which is required error signal is shown in Fig 4 and Fig 5. The Response of FIR Filter and FIR Based Razor and response is shown in Fig 6,7 and Fig 8.

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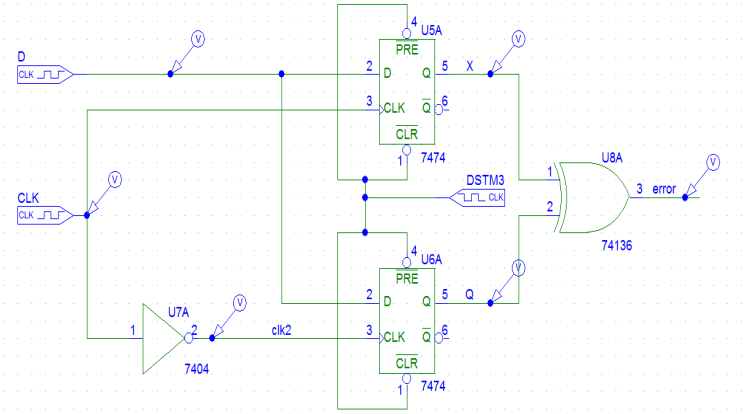


Fig 4.Razor FlipFlop


Fig 5 Response of Razor

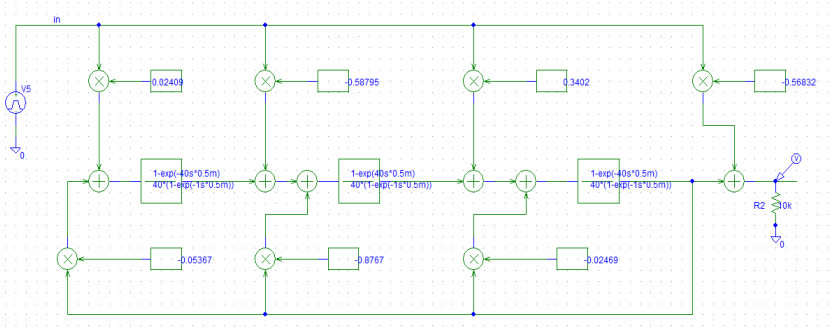


Fig 6 FIR using Spice

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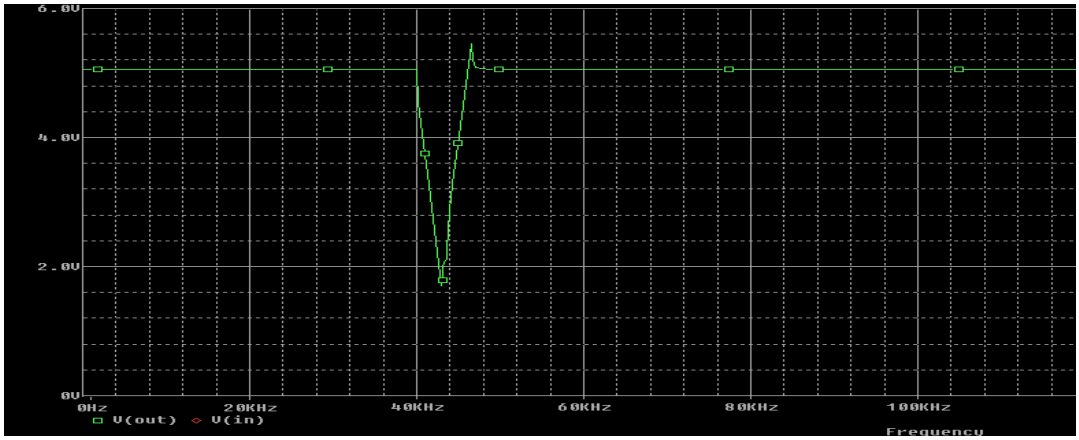


**Fig 7: Simulation result of FIR Filter**

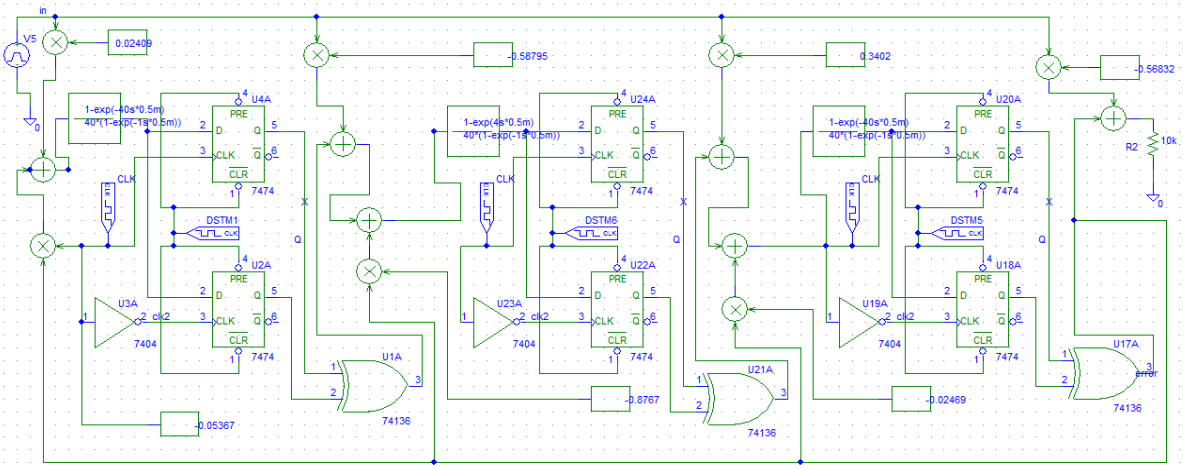


**Fig8 FIR based Razor Flip Flop using Spice**

| WITHOUT RFF(VOLTAGE) | WITH RFF(VOLTAGE) |
|---|---|
| 5.1 | 4.7 |
| 3.9 | 3.4 |
| 1.7 | 1.2 |
| 3.9 | 1.8 |

**Table 1 Comparison of voltage in FIR with and without Razor Flip Flop**

## V.CONCLUSION

In many DSP applications numbers of complex multiplications are involved in FFT processor and Filter implementation, in which high speed performance is the main target. However, this may be achieved at the expense of area, power dissipation, propagation delay and accuracy. The FIR filter is designed using Razor for every bit, the error bit is generated and one can overcome the error with the filter. The designed Filter can be used for any DSP application.The results show that Razor based method used to reduce the Voltage and Filter efficiently in digital signal processing algorithms is achieved without error.

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