ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Volume 5, Special Issue 1, March 2016*

National Conference on Recent Trends in Electronics and Instrumentation Engineering (NCRTE 2K16)

1st& 2nd March 2016

Organized by

Department of Electronics &Instrumentation Engineering, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

Design and Implementation of High Speed Vedic Multiplier for DSP Applications

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ABSTRACT: Multiplication is a basic important function in any arithmetic operations. Multiplication requires extensively more resources for hardware and processing time than addition and subtraction. Digital signal processors (DSPs) are the technology that is universal in engineering Discipline. Multiplication speed is very important in DSPs for digital FIR filter, convolution, Fourier transforms etc. This paper gives information of algorithms of Vedic Mathematics for efficient high performance FIR Filter by implementing new multiplier hardware to improve the speed, power and area.The reconfigurable Vedic multiplier has been designed and implemented on an FPGA based system.The architecture is simulated and synthesized in ModelsimSoftware.

KEYWORDS:FIR, VHDL, MODELSIM.

I.INTRODUCTION

Multiplication used in Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filtering and in ALU of advanced processor. Since low power multiplication performances dominates the execution time of most DSP algorithms, so there is a requirement of high speed and low power multiplier. Multiplication time is still the principal factor in determining the overall performance of a DSP chip.

The requirement for high speed processing and low power has as a greater demand as a result of expanding signal processing applications. Higher throughput arithmetic operations are important to realize the preferred performance for any processor. This is required in many real-time signal and image processing applications to meet the dead time. One of the solutions for arithmetic operations in such applications is multiplication and fast multiplier circuit has been a subject of interest over period of time. Reducing the time delay and power utilization are very necessary requirements for many applications [1] [2].

In general binary multiplication can be done by several techniques. The basic three stages involved for multiplication are partial products generation, column compression and final addition. There are number of techniques that to perform binary multiplication. In specific, the choice is based upon factors such as area, and design complexity. More efficient corresponding approach uses some sort of array or tree of full adders to sum partial products. Array multiplier, Booth Multiplier and Wallace Tree multipliers [6] are some of the standard approaches to have hardware implementation of multiplier which are suitable for VLSI implementation.Multiplier based on Vedic Mathematics is the fastest with low power consumption to be implemented in FIR filter using VLSI.

II. LITERATURE REVIEW

This section discusses the researchers have done many work on applications of Vedic mathematics in DSP application. The comparison for conventional and Vedic mathematics is done in VLSI for DSP with respect to efficiency complexity and performance analysis has been presented in [4].It shows that Vedic mathematical approach is fast and simple. Nikhilam Sutra" and UrdhvaTiryagbhyam Sutra' multiplication techniques are proposed in [5]. 16 X 16 multiplier using ,UrdhvaTiryagbhyam Sutra is presented and using 'Nikhilam Sutra' 16X16 multiplier modules uses two 8x8 modules , one 16 bit carry save adder and two 17 bit full adder stages are implemented to verify the function. The carry save adder increases the speed of partial products. The multiplier is implemented in SPARTAN 2 FPGA Device

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XC2S30-5pq208. The presented method shows speed improvements in [3]. The 'UrdhvaTiryagbhyam Sutra' and 'Nikhilam Sutra' multiplication techniques are found to be speedy when magnitudes of both operands are more than half of their maximum values. A floating point multiplier with 24X24 bit integer multiplication operation is presented using vedic algorithm, improvement in speed, efficiency and power has improved by using this sutra. A low power Multiplier is presented in [7].

The implemented multiplier is based on the ancient technique. Here the Urdhvatiryakbhyam sutra and Nikhilam sutras are used for multiplication. This technique is compared with the modern multiplier to highlight the performance in the Vedic Multipliers. To test the Vedic multiplier BIST (Built In Self-Test) is implemented and it is found Fault free. The results are compared with the Booth's Multiplier in terms of parameters like power and time delay. The multiplier is implemented using VHDL . The simulation results are presented based on power and time delay. A new architecture on Indian Vedic mathematics is proposed in [11]. The synthesis results with lower hardware requirement is achieved.

III. METHODS AND PERFORMANCES

The efficiency of the multiplier is determined by its speed. In a system design, the performance of the system is determined by speed, area and power requirement. Vedic mathematics [3] was based from the ancient Indian scriptures (Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of study on Vedas. Vedic mathematics is essentially based on sixteen principles or word-formulae which are termed as sutras. This is a very attractive field and presents some valuable algorithms which can be useful to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time.

These are the 16 basic sutra of Vedic mathematic:

- (AnurupyeS) Shunyamanyat -If one is in ratio, the other is zero.
- ChalanaKalanabyham -Differences and similarities.
- EkadhikinaPurvena- By one more than the previous One.
- EkanyunenaPurvena - By one less than the previous one.
- Gunakasamuchyah-Factors of the sum is equal to the sum of factors.
- Gunitasamuchyah-The product of sum is equal to sum of the product.
- NikhilamNavatashcaramamDashatah -All from 9 and last from 10.
- ParaavartyaYojayet-Transpose and adjust.
- Puranapuranabyham - By the completion no completion.
- Sankalana- vyavakalanabhyam -By addition and by subtraction.
- ShesanyankenaCharamena- The remainders by the last digit.
- ShunyamSaamyasamuccaye -When the sum is same then sum is zero.
- Sopaantyadvayamantyam -The ultimate and twice the penultimate.
- Urdhva-tiryakbhyam -Vertically and crosswise.
- Vyashtisamanstih -Part and Whole.
- Yaavadunam- Whatever the extent of its deficiency.

Thus, integrating Vedic mathematics for the multiplier design will enhance the speed of multiplication operation.

IV.FIR FILTER DESIGN TECHNIQUES

FIR filters are predominantly useful for applications where accurate linear phase response is required. The FIR filter is commonly implemented in a non-recursive way, which guarantee a stable filter [8].

1) The window method
2) The frequency sampling technique
3) Optimal filter design methods the FIR filter architecture is shown in Fig 1.

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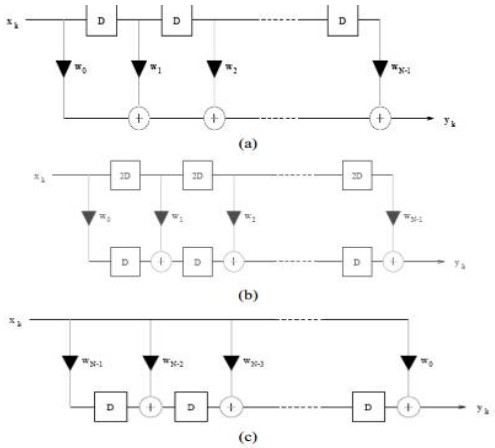

Fig 1. FIR Filter Architecture, (a) canonical form, (b) pipelined, (c) inverted form.

V.DESIGN OF HIGH SPEED VEDIC MULTIPLIER IN FIR FILTER

In this section the analysis of Vedic multiplier is compared for high performance for implementing it in FIR filter. The Vedic multiplier "UrdhvaTiryagbhyam" sutra (algorithm) is designed based on is a general multiplication formula it means that "Vertically and Crosswise" [9][10] and it is used for the multiplication of two decimal numbers. The advantage of this sutra is Partial products generation is done by parallel addition. The design of n x n bit numbers can be generalized by this sutra. The partial products and their sums in parallel of this multiplier are independent of clock frequency of the processor while calculating. Let us consider the multiplication of two decimal for this multiplication scheme, numbers (325 × 728). Line diagram for the multiplication is shown in Fig. 2.

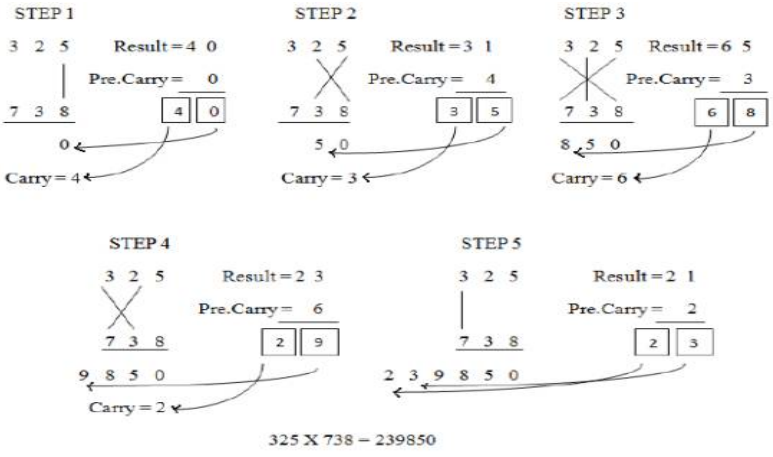

Fig 2.Multipication process of a decimal no

NikhilamNavatashcaramamDashatah Vedic algorithm is done by "All from 9 and last from 10" and it is more required for large numbers. Anurupye sutra is done by "if one is in ratio, then the other is in zero operation". Digital signal processing (DSP) application is the fastest technology blooming that is important in almost multi- discipline. Therefore, tremendous improvement contribution is to be made in the engineering community. Fast ALU operations are of extreme importance in DSP for digital filters, discrete Fast Fourier transforms etc.

Nikhilam Sutra algorithm means "all from 9 and last from 10" multiplication operation. It is applicable for all cases of multiplication but it is more performance for large numbers. Complexity increases for small numbers. The

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multiplication operation is carried by found out the compliment of the large number from its nearest base. Hence the complexity is reduced for larger original no [12].
Nikhilam Sutra performs subtraction of a two number from its nearest power base i.e. 10, 100, 1000, etc. The difference is calculated from the power of 10 is called as Base. It is seen that the difference between the base and the number is Positive and hence it is called as NIKHILAM.

The Nikhilam sutra is used to design both binary and decimal number system. The subtraction result of multiplicand and multiplier is represented by taking 2"s compliment of those two numbers. The right hand side (RHS) part of the product is implemented using 8x8 bit multiplier. The left hand side (LHS) part of the product is implemented using 8-bit carry save adder. If there is carry in RHS of product then it is added to LHS of product. The multiplication of 97 and 94 using Nikhilam sutra is shown in Fig.3.

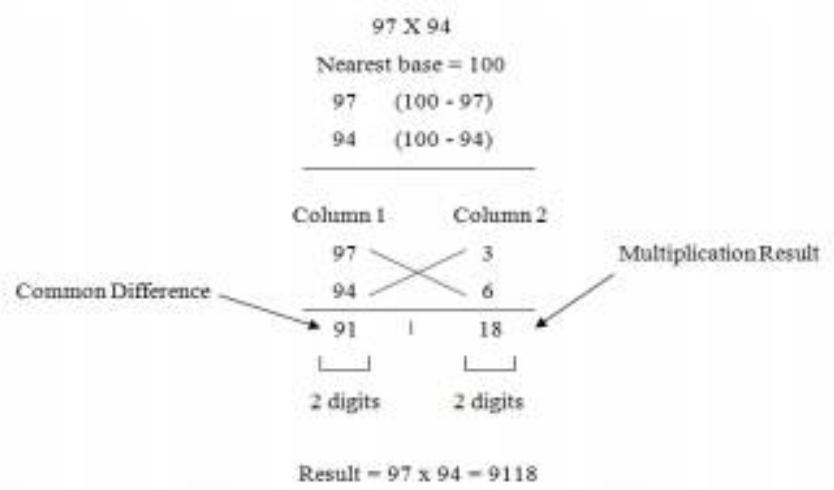

Fig 3. Multiplication steps using NikhilamNavatashcaramamDashatah

The upa-Sutra Anurupye means 'proportionality'. This Sutra is used to find products of two numbers. The Common bases are 50, 60, 200 etc. (multiples of powers of10).Fig.4shows theStructure of Anurupye Vedic Multiplier

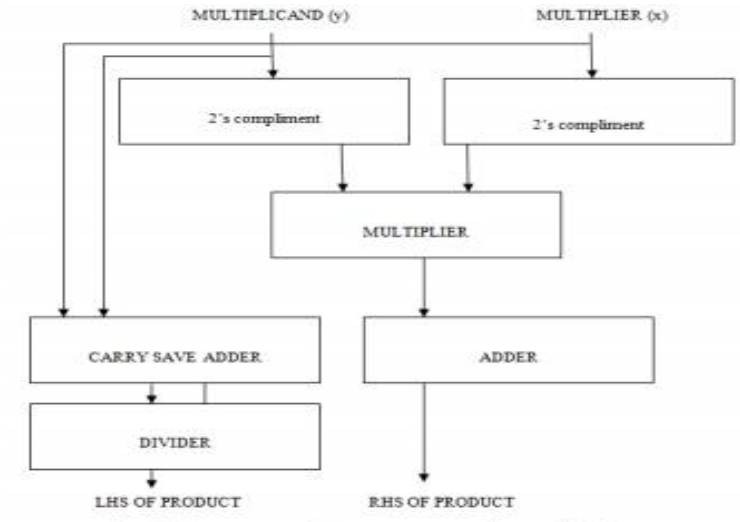

Fig.4 Structure of Anurupye Vedic Multiplier

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The Anurupye sutra is illustrated by consider the multiplication of two decimal numbers 58 x 48 by Anurupye method as shown in Fig 5.

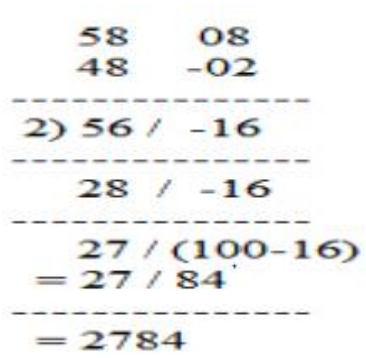

Fig.5 Multiplication Steps using Anurupye

VI.RESULT AND DISCUSSION

The Output window for 8x8 Anurupye Vedic Multiplier which was implemented in FIR filter is shown in Fig.7. It performs multiplication of two decimal numbers 58 x 48 by Anurupye method.

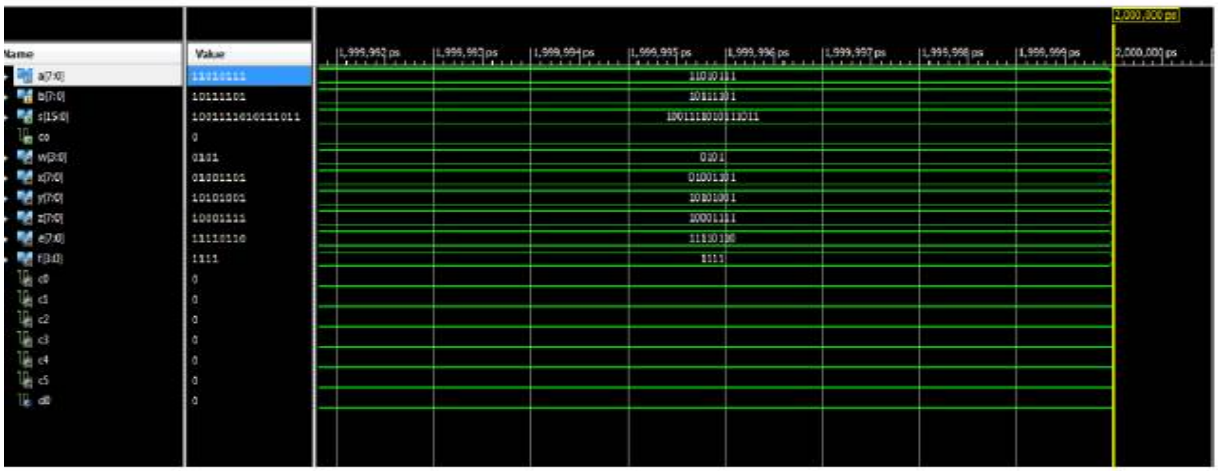

Fig.7 Result of 8x8 Anurupye Vedic Multiplier implemented in FIR filter.

The performance analysis of Vedic multiplier with high speed and low delay are explained as in Table No.1.

Vedic multiplier Design in FFT	Time Constraint (Delay)
8x8 Multiplication using Nikihilam Sutra	25.19 ns
8x8 Multiplication using Anurupye Sutra	17ns

Table No.1 Performance of Vedic Multiplierin FIR.

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VII.CONCLUSION

Using Vedic multiplier Urdhvatiryabhyam and NikhilamNavatashcaramamDashatah sutras, multipliers were designed. Anurupye Vedic multiplier on FIR is made efficient than all other Vedic multiplier such as Urdhvatiryabhyam and NikhilamNavatashcaramamDashatah sutras by more decrease in estimation time duration. Anurupye is used for multiplication of larger numbers. This can be used for design of Digital filters. These methods can be used to solve research problems and reducesdifficulty of digital FIR and IIR filters.

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