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Design and Analysis of 64 bit Multiplier using Carry Look Ahead Logic for Low Latency and Optimized Power Delay Product

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ABSTRACT: Increasing demand of portable electronics in the market has moved the companies to design the products in deep submicron technology. As the industry is scaling the technology to deep submicron, many issues are faced to meet the design specifications like latency, power and area generally. Adders and multipliers are considered very important part of any VLSI design and for the better performance of the device, these combinational designs should meet all the constraints on the specified technology. In this paper, the design of 64 bit multiplier is presented using carry look ahead logic and certain techniques for dynamic power reduction. Carry look ahead logic is considered to be the faster logic and providing the power reduction techniques to the design results in low power delay product and leads to an optimized design of multiplier. In this paper, multiplier design is implemented on technology independent platform using VHDL programming.

KEYWORDS: VHDL, CLA, VLSI, power delay product, ISE, FPGA, Latency

I.INTRODUCTION

Combinational circuits are the heart of electronic devices. Among these combinational circuits the adders and multipliers are of great importance as these are used at the multiple levels for calculations in functioning of the devices. Various logics can be implemented for the design of multiplier like booth algorithms, carry look ahead logic. But the main issue is to design an adder having less delay, low power consumption and reduced chip area. In past, the major challenge for VLSI designer was to reduce chip area by using efficient optimization techniques. Then the next phase is to increase the speed of operation to achieve fast calculations as, in today's microprocessors millions of instructions are executed per second. Speed of operation is one of the major constraints in designing VLSI designs. But nowadays most of commercial electronic products are portable like mobile, laptops etc and require larger battery backups. Hence the requirement extends to design the devices in optimized manner to meet the best possible constraints according to requirement of the market. So, lot of research is going on to reduce power consumption. Thus, there are three performance parameters on which a VLSI designer has to optimize their design i.e. area, speed and power. It is very difficult to achieve all constraints for particular design, therefore depending on demand or application some compromise between constraints has to be made. Many researchers have done work on these constraints. A reconfigurable approach of CLA and carry select logic is proposed for low latency design of adder [2]. A 64 bit reconfigurable adder technique is used [6]. Switching activity reduction technique is also used for the low power design of multiplier [9].

II.CARRY LOOK AHEAD LOGIC

This logic is based on the fact that at every step of calculation, we have no need to wait for the previous carry. So a serial chain gets converted to a parallel chain reducing the latency to a larger extent and making this logic faster among the others at cost of some increment in hardware for the additional CLA logic. In this algorithm carry for the next stages is calculated in advance based on input signals. Carry look ahead logic uses the concepts of generating and propagating carries. Generation and propagation logic are given as follows.

$$\mathbf{G_i = A_i \text{ AND } B_i} \qquad (1)$$

$$\mathbf{P_i = A_i \text{ XOR } B_i} \qquad (2)$$

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Where, G_i and P_i are generate and propagate logic for ithstage, A and B are the inputs.
Carry for the next stages is calculated using the following relation

$$\mathbf{C_{i+1} = (P_i \text{ AND } Ci) \text{ OR } G_i (3)}$$

Where, C_i is carry of ithstage and C_{i+1} is carry of next stage. The main aim of this logic is to remove the dependency of eachstage from the carry of previous stage and parallel computation can be done using the initial carry only. Hardware penaltyfor this CLA logic is of additional AND gates and OR gates. Number of additional AND gated required is given by

$$\textbf{No. of additional AND gates for CLA} = n^*(n+1)/2 \qquad \textbf{(4)}$$

Number of additional OR gated is given by

$$\textbf{No. of additional OR gates for CLA} = n \qquad \textbf{(5)}$$

Where n is the total number of inputs provided.
For the designing of multiplier using above explained logic, shifting techniques needed to apply. Each bit of single input is multiplied with the other 32 bit input and after that shifting of these results are performed and finally adding up these using look ahead logic [3]. Carry look ahead logic for 4 bit adder is shown in figure1.

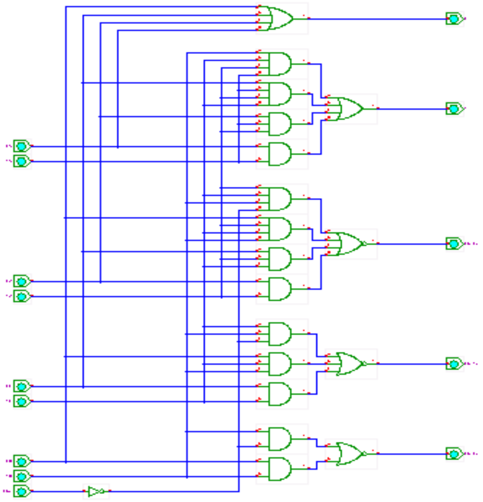

Figure 1. CLA logic

III.METHODOLOGY

For designing carry look ahead logic based multiplier, the methodology followed is as follows.

- Developing a piece of code in VHDL for generation and propagation logic.
- Developing code for CLA logic for 64 bits using above behavioral designs.
- Developing code for multiplier with two inputs of 1 bit and 32 bit respectively.
- Extending the code for 64 bit multiplier using shifting techniques and CLA adders.
- Synthesizing and implementing the design on FPGA board.
- Simulating the design by maximizing switching activity on input nets.
- Calculating the power using Xpower Analyzer tools and calculating power delay product for fastest and slowest path.

IV.SOFTWARE DESCRIPTION

- Xilinx ISE Design Suit 12.4: VHDL codes are written and synthesized using Xilinx suit. It provides the platform for generation of RTL schematic and implementing the design by following the steps of translation, mapping, placement and routing and finally a Bitstream file is generated to interface the design with FPGA board.

- ISIM simulator: ISIM is used to simulate the design for functional verification. No timing information is included in it. Simulation Activity file (SAIF) is also invoked through the ISIM simulator by maximizing switching activity on the inputs.
- Xpower Analyzer: Power estimation for the design is achieved using Xpower Analyzer, which provides both Quiescent as well as dynamic power for typical, min and max conditions at a particular ambient temperature and frequency.
- FPGA Development board: Xilinx Spartan-3E kit is used for implementing the design on hardware. But only a few combinations of inputs is tested on the board due to limited number of IOs available on the board.

V. SYNTHESIZE AND SIMULATION RESULTS

RTL (Register Transfer logic) view: RTL view of the design is shown in figure2. RTL basically provides the information of design by connecting all the blocks with one another in a regular hierarchy. Various blocks of the design are represented as LUTs (look up tables) and are connected with each other thorough the nets or wires. This RTL is extracted by the synthesizer tool from the HDL code. Netlist information can be extracted from it.

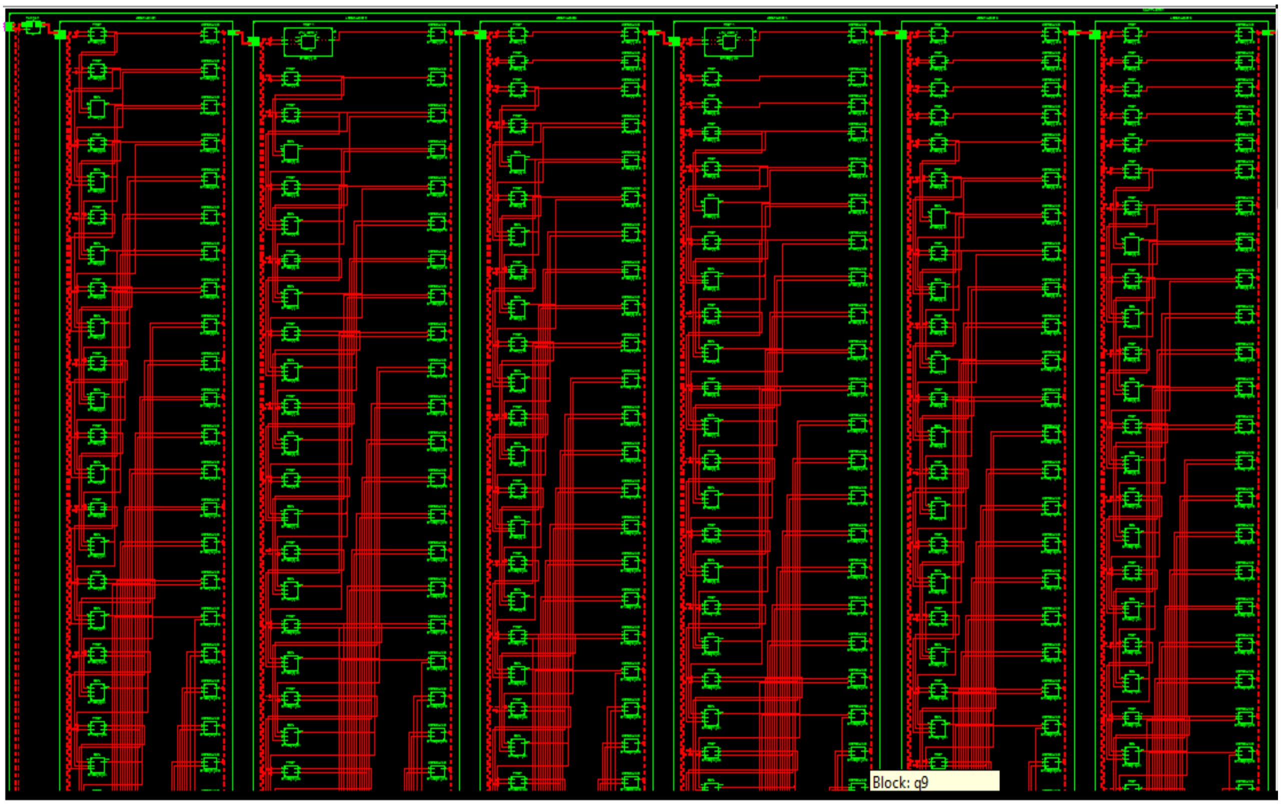

Figure 2. RTL view of designed multiplier

Technology view of the design is also shown in Figure 3. This differs from the simple RTL view because it makes use of some additional MOS devices for the technology driven design. HDL provides us a technology independent platform but after all design process, we need to map the design to a particular nanometer technology for which some additional devices are added into the technology view of design.

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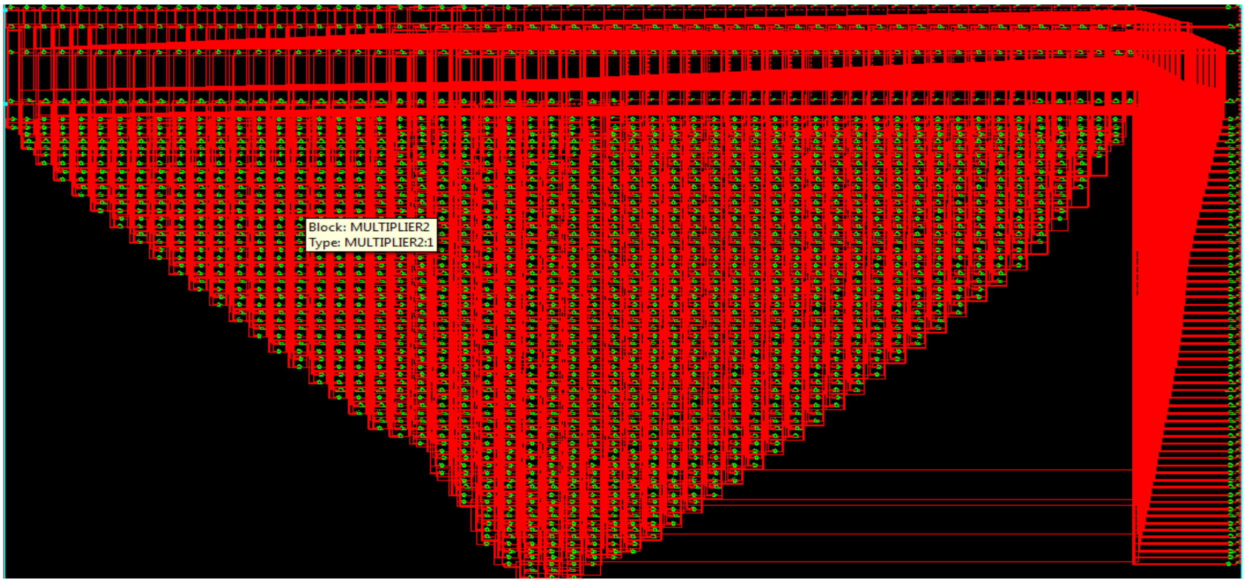
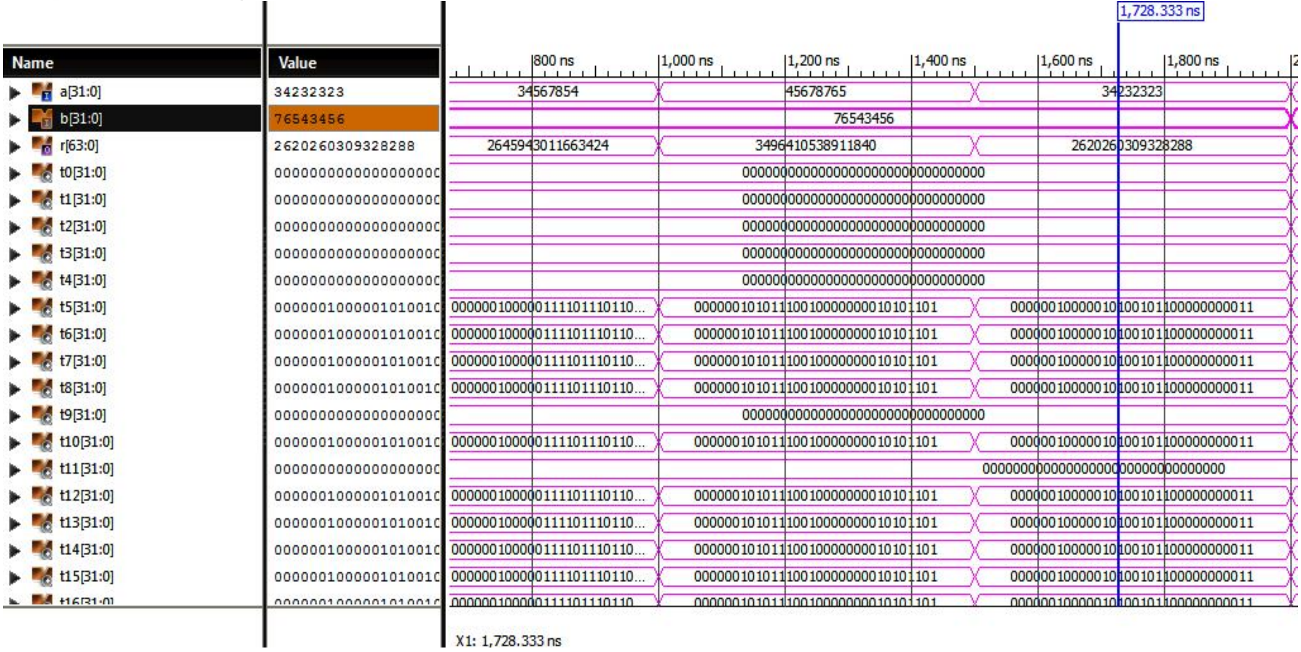


Figure 3. Technology View of designed multiplier

Simulation Waveforms: Simulation is done using ISIM simulator in the Xilinx IDE 12.4 and the response obtained by providing the various inputs is shown in figure4 and figure5. Values of two inputs and output are described in unsigned decimal format. Each cycle is operated for 1 us of time. A large no of transitions are provided to input ports, so to have the maximum switching activity to generate SAIF (Simulation Activity File), which accounts for the dynamic power dissipation in the design.



Name	Value
a[31:0]	34232323
b[31:0]	76543456
r[63:0]	2620260309328288
t0[31:0]	0000000000000000000
t1[31:0]	0000000000000000000
t2[31:0]	0000000000000000000
t3[31:0]	0000000000000000000
t4[31:0]	0000000000000000000
t5[31:0]	0000001000001010010
t6[31:0]	0000001000001010010
t7[31:0]	0000001000001010010
t8[31:0]	0000001000001010010
t9[31:0]	0000000000000000000
t10[31:0]	0000001000001010010
t11[31:0]	0000000000000000000
t12[31:0]	0000001000001010010
t13[31:0]	0000001000001010010
t14[31:0]	0000001000001010010
t15[31:0]	0000001000001010010
t16[31:0]	0000001000001010010

Figure 4. Waveforms1 of 64 bit multiplierusing CLA logic

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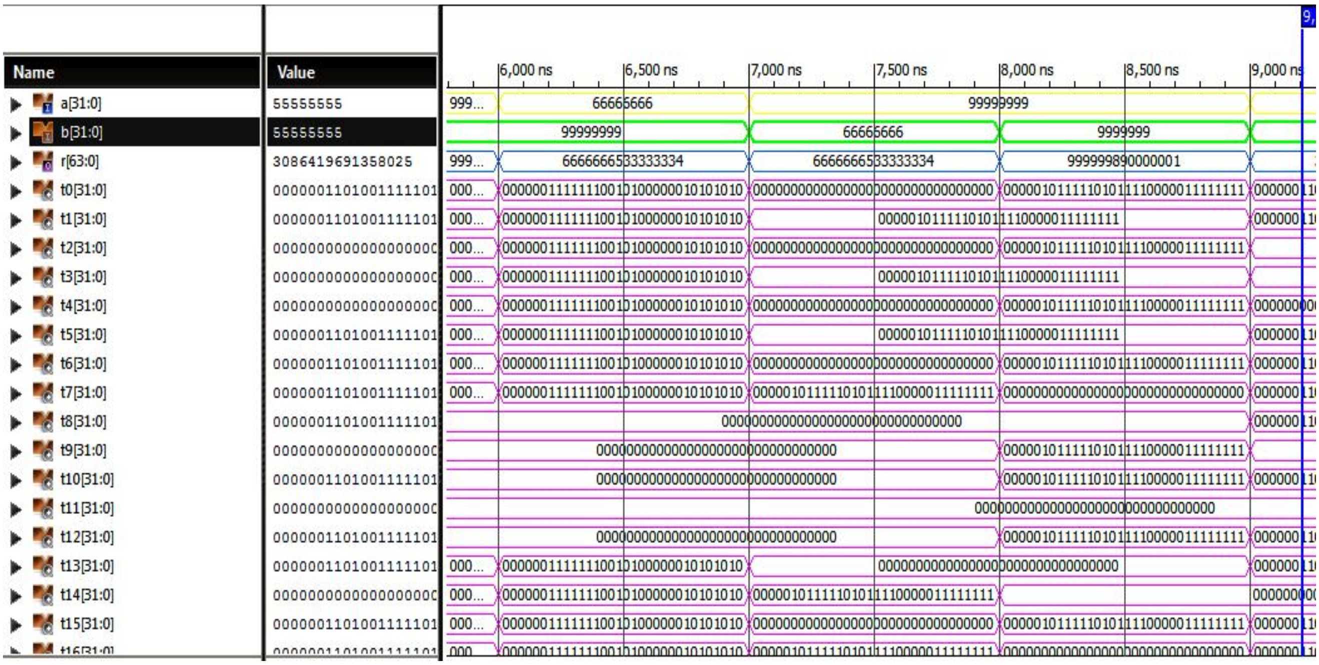

Name	Value
a[31:0]	55555555
b[31:0]	55555555
r[63:0]	3086419691358025
t0[31:0]	0000001101001111101
t1[31:0]	0000001101001111101
t2[31:0]	0000000000000000000
t3[31:0]	0000000000000000000
t4[31:0]	0000000000000000000
t5[31:0]	0000001101001111101
t6[31:0]	0000001101001111101
t7[31:0]	0000001101001111101
t8[31:0]	0000001101001111101
t9[31:0]	0000000000000000000
t10[31:0]	0000001101001111101
t11[31:0]	0000000000000000000
t12[31:0]	0000001101001111101
t13[31:0]	0000001101001111101
t14[31:0]	0000000000000000000
t15[31:0]	0000001101001111101
t16[31:0]	0000001101001111101

Figure 5. Waveforms2 of 64 bit multiplier using CLA logic

VI. RESULT REPORTS AND DISCUSSIONS

Power calculation: Both dynamic and static powers are calculated using Xpower analyzer by providing design file (.ncd), settings file(.xpa), physical constraints file (.pcf) for static power dissipation and Simulation activity file (.saif) for dynamic power dissipation. Power supplies provided are taken for the typical case. Power supply voltages and currents are given in Table 1 and the corresponding power dissipations (Quiescent and Dynamic) is given in Table 2.

Table1 supply voltage and currents

Supply Source	Supply Voltage	Quiescent Current (mA)	Dynamic Current (mA)	Total Current (mA)
Vccint	1.140	62.07	0.10	62.16
Vccaux	2.125	45.00	0.03	45.03
Vcco25	2.125	3.00	0.52	3.52

Table2 Power dissipation report

Quiescent Power(mW)	Dynamic Power (mW)	Total Power (mW)
173.52	1.40	174.93

Delay (Latency): Delay is calculated from net to net (i.e. from input net to output net). Hence in this design a large number of combinations are possible as two 32 bits inputs and one 64 bit output is there. Delay can be mapped from any single input to single output net. Table4 gives the information of delay for the slowest and fastest net among all the nets available in the design.

Table4 Net to Net delay

	Input Pin	Output Pin	Delay (nsec)
Fastest Net	A<0>	R<1>	10.575
Slowest Net	A<1>	R<62>	160.899

Power Delay Product (Figure of Merit): PDP is simply calculated by multiplying the power dissipation on a net to its latency. Generally one value of the PDP is taken for the design. To meet all the required specifications, net with the maximum latency is considered (critical path). In this design the PDP is **28.146 nj**(nano joules).

Device Utilization: Table3 describes the utilization of device used for the design. Total 128 IOs are there in the design. It shows the amount of hardware being used in the design.

Table3 Device Utilization Summary

Device Information		% utilization
No. of slices	1169 out of 14752	7%
No. of 4 input LUTs	2054 out of 29504	6%
No. of IOs	128	
No. of bonded IOBs	119 out of 250	47%

VII. CONCLUSION

Faster, smaller and high power backup devices are the requirement of today’s world and the process begins from the basic modules of the design. Being a very important part of the chip designing, multiplier’s performance parameters need to be improved. CLA logic presented in this papers is used for the design of high speed and low power 64 bit multiplier. An optimized power delay product is calculated. Xilinx ISE is used for VHDL code generation and ISIM simulator is used for simulation of design. Power is calculated using Xpower Analyzer. The total power dissipation obtained for the min conditions of power supply is 174.93 mW. Delay calculated on the slowest and fastest nets are 160.899 and 10.575 respectively. PDP for the critical net comes out to be 28.146 nano joules.

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BIOGRAPHY

Gaurav Vashisht is pursuing his Master's degree in "VLSI Design" from CDAC, Mohali (Punjab). He received his bachelor's degree (Electronics and communication) from DAV Institute of Engineering and Technology, Jalandhar (Punjab). He is also working in Cadence Design Systems in product validation of EDA tools. His research interests include Low power VLSI design, Characterization of digital libraries in nanotechnology and Regression analysis for EDA tools. He is engaged in HDL coding of AMBA buses and low power techniques for deep submicron processes.

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