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An Efficient Single-Stage Integrated Double Buck AC/DC Converter

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ABSTRAT: The aim of this project is to design an efficient single-stage integrated double buck AC-DC converter and to improve the speed of response of the converter. The converter which integrates a buck-type power factor correction cell with a buck-type DC–DC output cell in a special way. High input power factor can be obtained automatically by operating the PFC cell inductor in discontinuous conduction mode (DCM), where the well and tight output voltage is regulated by the DC-DC cell. The converter has two switches which are controlled using fuzzy logic controller. The advantages of this converter are low voltage stress across the dc-link capacitor, low current stress of the switch, high step down input to output conversion ratio, low cost and size. These characteristics makes the converter cost-efficient, easy-to-design, and suitable for the low-power and non-isolated applications. Simulation and experimental results are also presented.

KEYWORDS: IBUBU Converter, PI Controller, Power Factor Correction, Fuzzy Controller, Transformer-less.

I. INTRODUCTION

Due to the stringent current-harmonic regulations, which are imposed on single phase ac/dc power supplies, inclusion of a power-factor-correction (PFC) circuit in the power-supply design becomes mandatory. The research on single stage PFC ac/dc converters can be carried out by early 1990s. Single-Stage power-factor-corrected ac/dc converters, which combine a power factor correction (PFC) circuit and a dc/dc regulator circuit and share a common set of active power switches[1]-[3]. The aims are to reduce the converter size, control circuitry, and, thus, cost. The SS ac/dc converter reduces cost, size, and complexity in the control loop by combining a PFC cell with a post-dc/dc cell and using one common set of switching-control signal. It is a very attractive solution in low power application where the manufacturing cost and size of converter are the major issues. The underlying principle for the SS ac/dc conversion is to force the PFC cell inductor operating in discontinuous conduction mode (DCM) to achieve high power factor automatically without any control loop, whereas the well and tight output regulation is done by post-dc/dc cell working in DCM or continuous conduction mode (CCM).Therefore, only one control loop is needed for the whole circuit. The absence of transformer reduces the component counts and cost of the converter

In this paper, it propose an efficient converter with high power factor, high step down feature and low voltage stress in the bus capacitor. So the ultimate aim of doing this project is to improve the efficiency and improve the speed of response of the converter. The efficiency improvement of the converter is done by replacing the losy diode by a switch and the speed of the converter is improved by using fuzzy logic controller instead of PI controller. When a converter is said to be good, it must have high PF, low THD, high efficiency and have low cost. The proposed converter satisfies these entire standards and is shown in the last section of the paper.

II. SINGLE-STAGE PFC CONVERTER

Power factor correction (PFC) techniques have become increasingly important since several regulations that are used to limit harmonic injection to the power utilities have been enacted recently. A two-stage scheme results in high power factor and fast response output voltage regulation by using two independent controllers and optimized power stages. The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications. An SS scheme combines the PFC cell and dc/dc power conversion cell into one stage, and typically uses only one controller and shares power switches. Although

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the single-stage scheme is attractive in low cost and low power applications due to its simplified power stage and control circuit.

III. PROPOSED CIRCUIT DIAGRAM AND ITS OPERATING PRINCIPLE

DC-DC converters can be used as switching mode regulators to convert an unregulated dc voltage to a regulated dc output voltage. The working of Single Stage double buck converter topology is explained by discussing the various modes of operation of the converter.The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L_1 , D_1 ,D_a, C_o , and C_b) and a buck dc/dc cell (L_2 , S_1 , S_2 , D_a , C_o , and C_B) is illustrated in Fig. 3.1. Both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0.

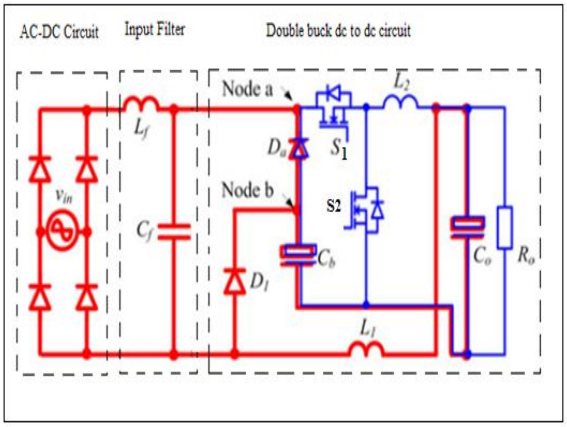
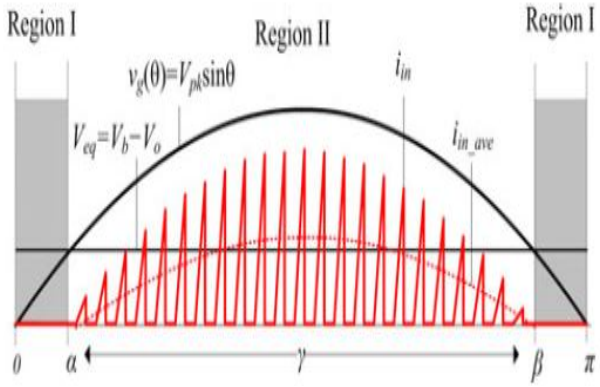


Fig 3.1 Proposed IBuBuBo SS ac/dc converter



3.2. Input voltage and current waveform

Due to the characteristic of buck PFC cell, there are two operating modes in the circuit. The proposed converter includes a buck-type PFC cell, therefore, two working regions can be found within half of line cycle period, as shown in Fig. 3.2. With the proposed integration, the equivalent voltage Veq = Vb−Vo acts as the sink of the PFC cell, the rectifier does not conduct when vg (θ) < Veq , this interval is defined as Region I. Oppositely, if vg (θ) > Veq , the rectifier conducts and a input current i_{in} appears. This interval is defined as Region II.

A. OPERATIONAL MODES IN REGION I

The circuit operation over a switching period can be divided into three stages and the corresponding sequence is Fig. 3.3, 3.4 and 3.5. The key waveforms are shown in Fig. 3.6.

M1 (t_0− t_1) (period M1 in Fig. 3.4) [see Fig. 3.3(a)]: Switch S_1 is turned ON, the voltage applied on L_2 is Veq = Vb−Vo, iL_2 increases linearly from zero with the slope Veq /L_2 ; on the other hand, the voltage applied on the rectifier diodes is vg (θ)−Veq . Noticing vg (θ) < Veq in this region, the rectifier is blocked, there is no current flowing through L_1, $i_{L1} = i_{in} = 0$. This mode will persist until S is turned OFF at t_1.

M2(t_1− t_2) (period M2 in Fig. 3.4) [see Fig. 3.3(b)]: Switch S_1 is turned OFF, iL_2 is freewheeling through S_2 (since S2 is turned on), i_{L2} decreases linearly with the slope Vo /L_2. The current flowing through Cb and S is now zero; in the PFC cell, i_{L1} and i_{in} are also zero, which is the same as M1. This mode will persist until iL_2 decreases to zero at t_2.

M3(t_2 − t3) (period M3 in Fig. 3.4) [see Fig. 3.3(c)]: Once iL2 decreases to zero, it keeps zero until S is turned ON again. In this mode, only the energy in Co is released to Ro, the currents flowing through L_1, L_2, Cb , and S are all zero. Obviously, the dc–dc cell is actually a buck converter working in the DCM, while the PFC cell is deactivated during this region.

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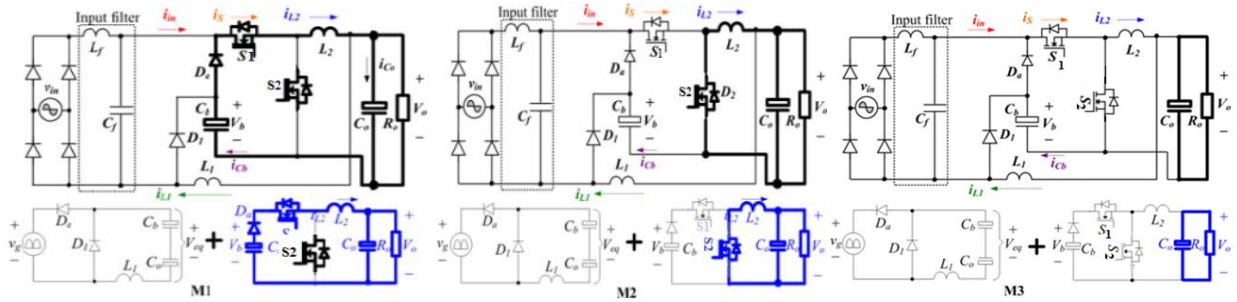


(a) (b) (c)

Fig. 3.3 Circuit operation stages of region II of the proposed ac/dc converter.

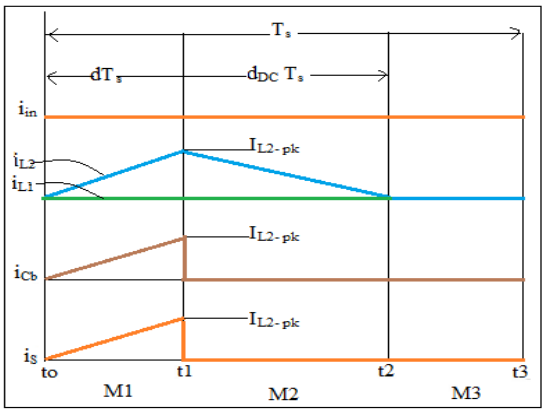


Fig.3.4. Key waveforms of the proposed circuit in region II

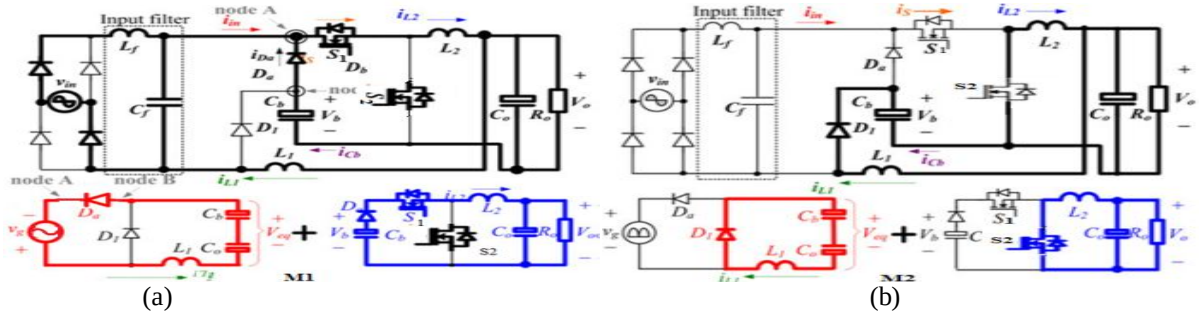
B. OPERATIONAL MODES IN REGION II

M1(t_0–t_1) (period M1 in Fig. 3.6) [see Fig. 3.5(a)]: When S1 is turned ON in this case, the voltage across L2 is Veq = Vb−Vo, which is the same as that in M1. And since D_a also conducts, nodes a and b have the same voltage levels, it means the voltage applied on L_1 is vg (θ)−Veq. Noticing vg (θ) > Veq, the rectifier is conducted and iL_1 begins to increase linearly from zero with the slope [vg (θ) − Veq]/L1. This mode is persisting only when D_a is conducting. It means $i_S > i_{in}$, or equivalently $i_{L2} > i_{L1}$ must be satisfied, This mode will persist until t_1 when S is turned OFF.

M2 (t_1–t_2) (period M2 in Fig. 3.6) [see Fig. 3.5(b)]: S1 is turned OFF. In the dc–dc cell, i_{L2} is freewheeling through S_2, the voltage applied on L_2 is −Vo, therefore i_{L2} decreases linearly with the slope −Vo /L2 , and finally reaches zero at t2 . In the PFC cell, i_{L1} is freewheeling through D_1, the voltage applied on L_1 is −Veq, i_{L1} decreases with the slope −Veq /L1. In this mode, i_{in} keeps zero and i_{Cb} always equals to $-i_{L1}$.

M3 (t_2–t_3) (period M3 in Fig. 3.6 [see Fig. 3.5(c)]: i_{L2} has decreased to zero, i_{L1} keeps decreasing because the voltage applied on L_1 is still Veq. i_{L1} will finally reach zero at t3.

M4 (t_3–t_4) (period M4 in Fig. 3.6) [see Fig. 3.5(d)]: Both i_{L1} and i_{L2} are zero, the circuit state goes to M3, as that in region I.



(a) (b)

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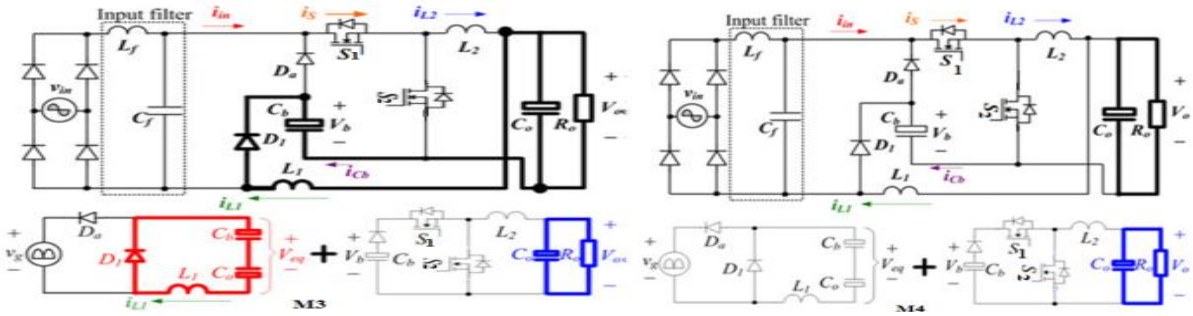

(c) (d)

Fig. 3.5 Circuit operation stages of region II of the proposed ac/dc converter.

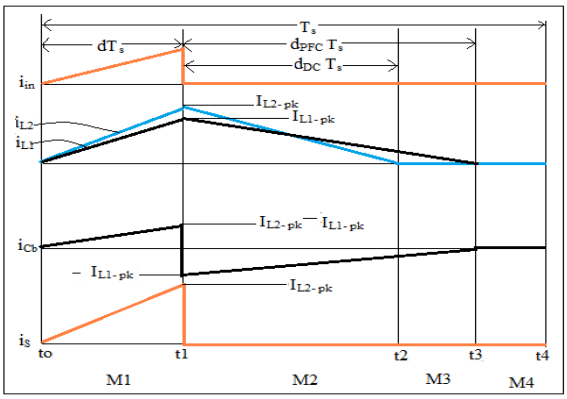

Fig.3.6. Key waveforms of the proposed circuit in region II

IV. DESIGN OF IBUBU CONVERTER

The IBuBu converter is designed as follows for simulation in Matlab 2014.
The input voltage of the converter can be varied between (90-270)Vrms.
Let the input voltage be, Vin = 120Vrms
Switching frequency = 20 kHz
Output power = 10W
Switch control = Closed loop PI control
In order to design the circuit components, first find the Peak-input to equivalent sink ratio Mpe

$$Mpe = \frac{Veq}{Vpk} \quad \text{, where } Veq = Vb - Vo \qquad (1)$$

$$vg(\theta) = |vin| = Vpk \sin\theta \quad \theta \in [0, \pi] \qquad (2)$$

dead angles, $\alpha = \arcsin(V_{equ} \div V_{pk})$

$$\beta = \pi - \alpha = \pi - \arcsin(V_{equ} \div V_{pk}) \qquad (3)$$

The duty ratio of the IBuBu converter be:

$$d < \frac{V_o}{V_o + M_{pe} V_{pk}} \text{ and } d < M_{pe} \qquad (4)$$

To find the value of inductor, use the following equations

$$L = \frac{2\pi M_{pe}^2}{\pi - 2\arcsin M_{pe} - 2.M_{pe}\sqrt{1 - M_{pe}^2}} \qquad (5)$$

The value of bus capacitor (Cb) and output capacitor (Co) can be found out using equation:

$$Cb = \frac{2Po * thold\_up}{Vb_{Max}^2 - Vb_{Min}^2} \qquad (6)$$

Current flows through the inductor L_1 is calculated by

$$I_{L1\_pk} = I_{in\_pk} = \frac{vg(\theta) - V_{eq}}{L1} dTs \qquad (7)$$

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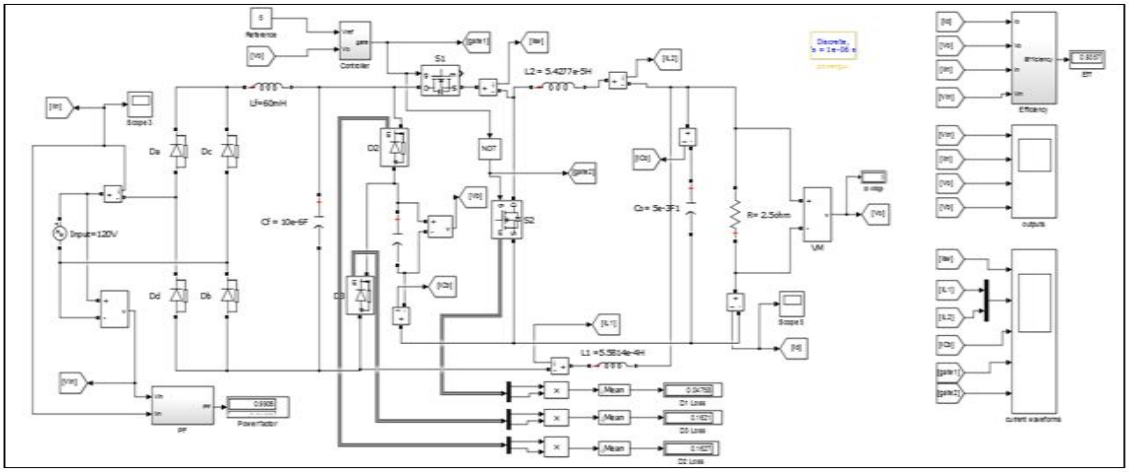
$$I_{L2\_pk} = \frac{V_{eq}}{L2} dTs \qquad (8)$$

V. SIMULATION AND HARDWARE RESULTS

The simulation and verification of an ac-dc converter is done in Matlab/simulink. Fig 5.1 shows the simulation of the modified single stage integrated double buck converter. The switch of the modified converter is controlled using fuzzy logic controller instead of PI controller. The simulation results of the modified converter shows that the efficiency of the converter is greater than 93%. As compared to the conventional converter the efficiency of the proposed converter increases from 10 to 15%.



5.1 Simulation of proposed converter

In this model there are three subsystem blocks. They are power factor block, efficiency block and controller block. Each block is shown in fig 5.2, 5.3 and 5.4 respectively.

A. SUBSYSTEMS

a) Power Factor Block

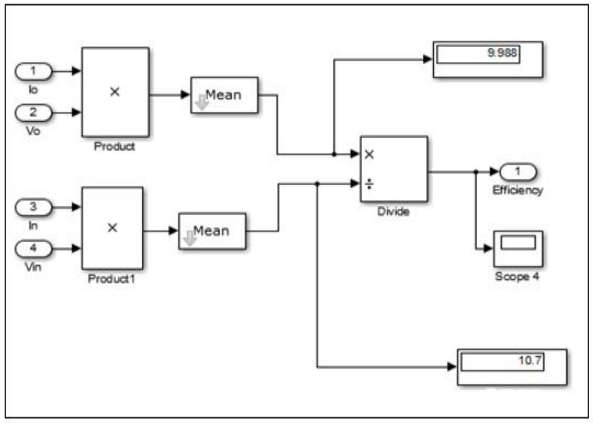


Fig 5.2 Block diagram for calculating power factor

b) Efficiency block

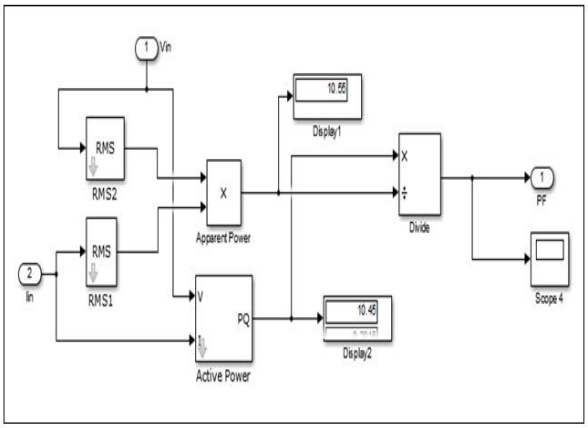


Fig 5.3 Block diagram for calculating efficiency

c) Fuzzy Logic controller block

Figure 5.4 shows the simulation block of fuzzy logic controller. The two inputs to the fuzzy controller are:

1. Error = Vref- Vo
2. Delta error (change in error) = Present error- Previous error

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These inputs are fuzzified, evaluated based on the rules defined and defuzzified by Mamdani FIS to produce the output. Details of fuzzy logic are explained in the next section.

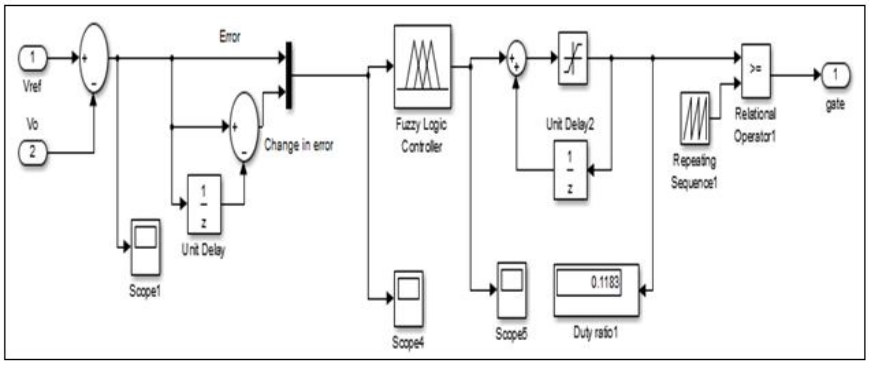

Fig 5.4 Block diagram of fuzzy logic controller

B. SIMULATION RESULTS OF THE MODIFIED CONVERTER

a) Voltage waveforms

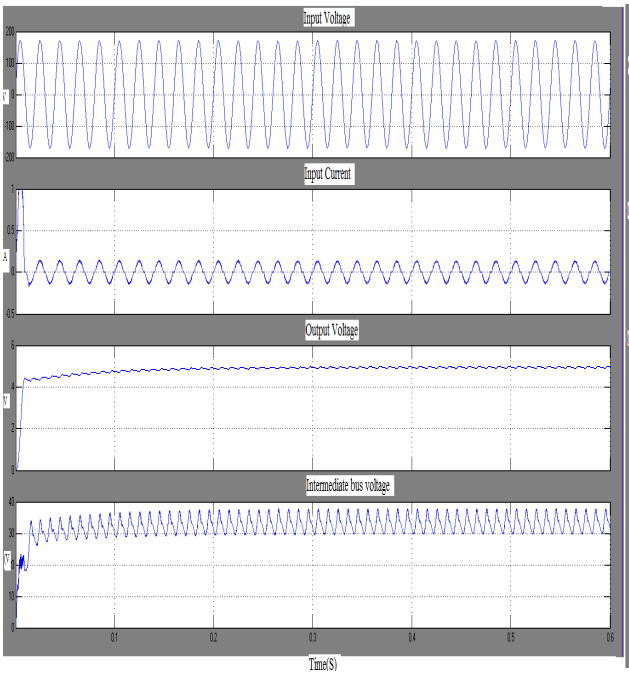

Fig 5.5 Simulation results of the modified converter

b) Current Waveforms

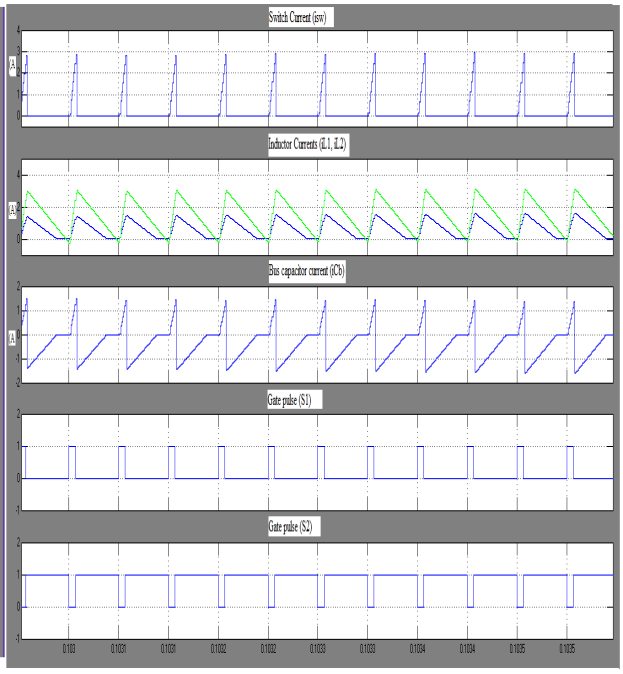

Fig 5.6 Current waveforms of the modified converter

The waveform above shows the voltage and current wave forms of each component. From fig it is clearly seen that high AC input (120Vrms) is stepped down to low DC output voltage (5V) without using high step down transformer and have low intermediate bus voltage, usually (39V) for a given 120V AC.

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c) Power Factor

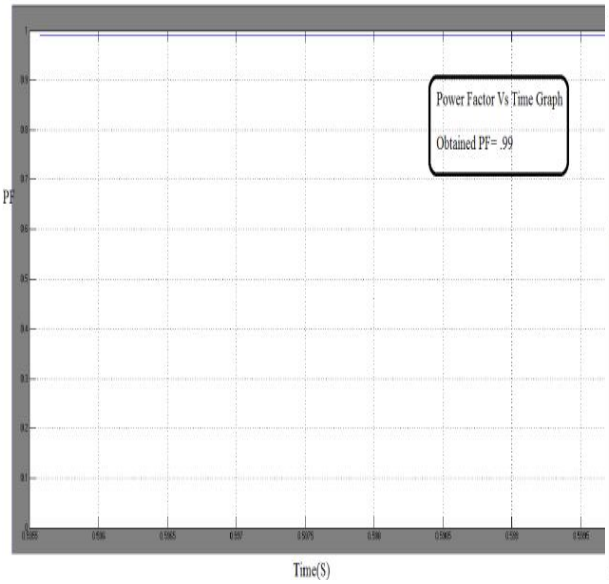

Fig 5.7 Power factor of the modified converter

d) Total Harmonic Distortion

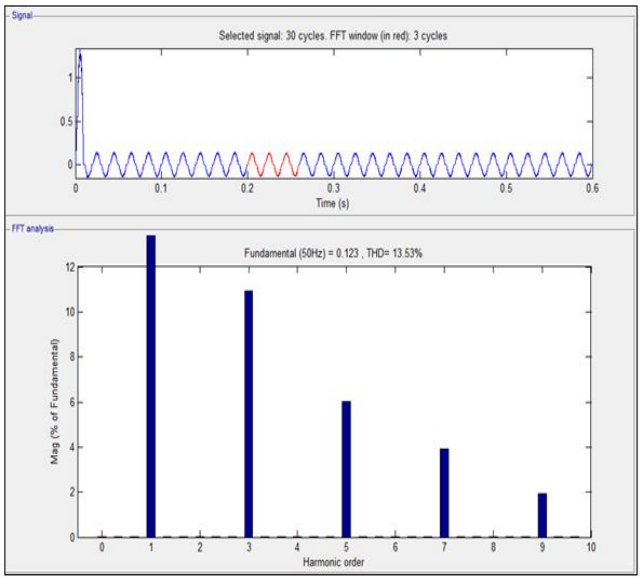

Fig 5.8 THD of the modified converter

As shown the power factor of the modified AC-DC converter is .99. ie, high power factor is automatically achieved by operating the PFC cell in discontinuous conduction mode. To ensure the THD of the input current, IEC61000-3-2 Class C standard is followed in the entire operational range in IBuBu converter. The THD of the proposed converter is 13.53%.

e) Efficiency

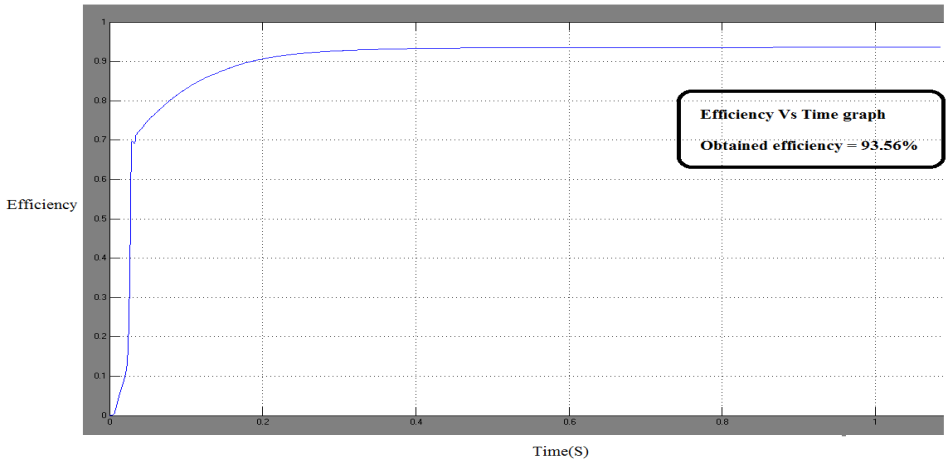

Fig 5.9 Efficiency of the modified converter

Efficiency of the proposed converter is shown in fig 5.9. From the fig, it can be seen that the efficiency is 93.56% which is 11.56% higher than the conventional IBuBu converter.

C. HARDWARE RESULTS

The main components of hardware is AC-DC converter, DC-DC converter, voltage regulator, DSPIC microcontroller for controlling the switching of the dc-dc converter and a driver circuit is used in between the MOSFET and DSPIC microcontroller. Power supply is provided for each of these components according to their requirements.

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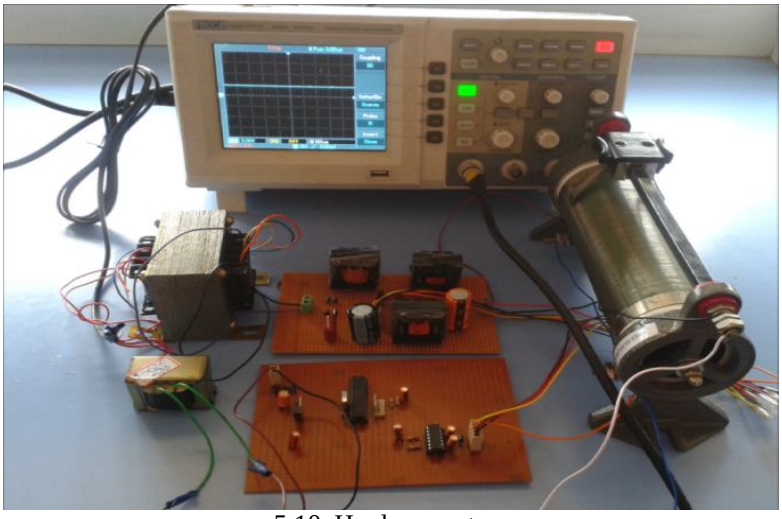

5.10. Hardware setup

The DCM current waveform and voltage waveform observed acrosss various components in the circuit with closed loop gate control for D=11.8% are given below:

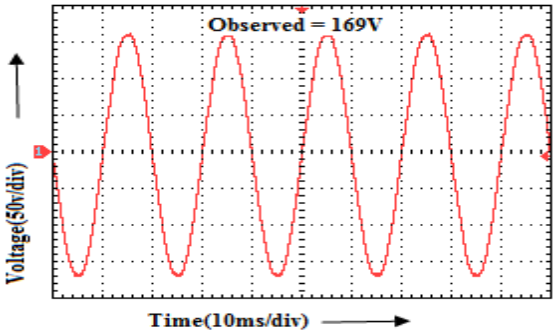

Fig 5.11 Input supply voltage

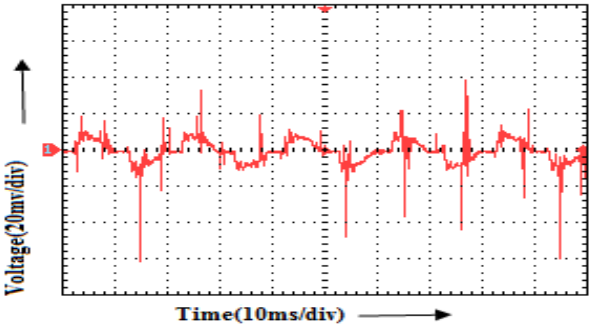

Fig 5.12 Input current

Fig 5.11 and 5.12 shows the input voltage (120 Vrms) and DCM input current respectively.

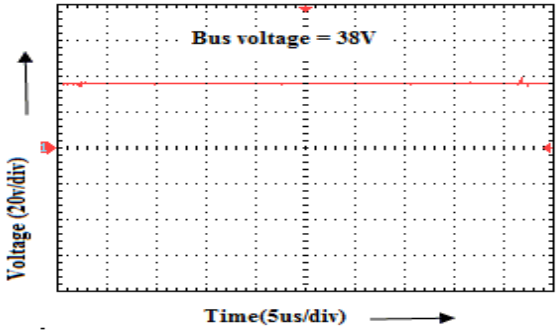

Fig 5.12. Intermediate Bus Voltage

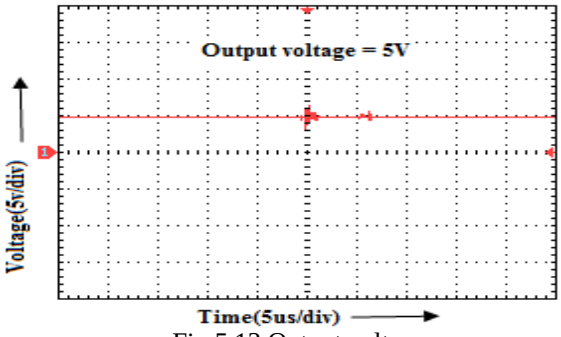

Fig 5.13 Output voltage

From results shown above, it can be seen that high AC input (120Vrms) is step down to low DC output voltage (5V) without using a high stepdown transformer and the voltage stress of the bus capacitor is reduced by reducing the bus voltage(usually 38V) and proved that the converter is operated in DCM.

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VI. CONCLUSION

An efficient single stage double buck AC-DC converter was designed and hardware implementation of the same was done. The proposed IBuBu converter has the following advantages: The efficiency of the converter is improved by 10-15%, by replacing the diode by a switch. Due to the integration of two buck cell, a high step-down feature is obtained, the buck PFC cell leads to a low dc link capacitor voltage not greater than 160V, voltage stress is low, the switch in the converter needs to handle the current of the DC-DC cell, current stress is low, high power factor and low total harmonic distortion, low cost and small size, replacement of PI controller with fuzzy logic controller improves the speed of response of the converter.

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BIOGRAPHY

First author: **Preethy G Nair** was born in Kerala. She received the B.Tech degree in Electrical and Electronics from Ilahia College of Engineering and Technology, Mulavoor, Muvattupuzha, affiliated to Mahatma Gandhi University, Kerala in 2011. She worked at Intrans Electro Components Pvt Ltd from 2011-2013. She is currently pursuing his M.Tech degree in Power Electronics from Sree Narayana Gurukulam College of Engineering, Kadayirippu, Kerala. She attended and presented a paper "Design and Implementation of a Battery Charger using an "Ultrasparse Matrix Rectifier with ANN Control" in an International Conference on Emerging Trends in Engineering and Management at SNGCE, Kadayirippu on December 2014. She also published a paper "A Transformerless Single-Stage Single Switch AC/DC Converter with High Power Factor, Regulated Bus and Output Voltages" on an international journal (ISJSET) on June 2015.

Second author: **Loveleen K.V** was born in Kerala. She is currently working as an Assistant Professor in the Department of Electrical and Electronics Engineering, Sree Narayana Gurukulam College of Engineering, Kadayirippu, Kerala. She received B.Tech degree from Amritha Institute of Technology and Science, Ettimadai, Coimbatore, Tamilnadu and received his M.Tech degree from Nehru College of Engineering and Research Centre, Pampadi, Ottapalam, Palakkad, Kerala.