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Leakage Power in CMOS and Its Reduction Techniques

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ABSTRACT:The Power efficiency is the major concern in the field of integrated electronics. With the increase in number of transistors in a chip every year, the complexity of the chip increases and which in turn leads to increase in power consumption levels.Consequently the decrease in transistor gate length as well as path length also led to the increase in resistance of the chip escalating the power usage. So, reduction of power consumption levels has become a desperate task for the researchers all around the world. Leveraging the power includes many techniques like optimizing the logic-design, enhancing the clock distribution network and importantly reduction of power dissipation.Coming to the point of power dissipation,leakage power is one of the major source.Leakage power is primarily the result of unwanted subthreshold current in the transistor channel when the transistor is turned off. Practically, the leakage power has become inevitable.The only thing we are able to do is to reduce the leakage power to some extent.In this paperwe are going to discuss the sources of leakage power and two techniques for mitigating the leakage power which are Transistor stacking and self- adjustable voltage level circuit.

KEYWORDS: Transistor stacking, self-adjustable voltage level circuit, leakage power, clock distribution network, sub threshold current, logic optimisation.

I. INTRODUCTION

With the increase in technological advancements of semiconductor device industry, power consumption has become one of the crucial topics to be addressed. For instance, the mobile devices, which became very popular now-a-days, lacked the efficiency in power expenditure forcing the multinational electronic industries to focus on developing power efficient devices. The factors that pull us towards building low power design circuits are: growth of battery powered systems, cost, environmental efforts, need for mobility, portability and reliability of users. The aim to improve the performance is accomplished often by scaling the CMOS devices. But, because of scaling technology, the power density increases by 40% with every generation. To decrease the power density, there always exists a trade-off between different aspects such as area or delay or high performance and hence, there is no universal technique to design an ideal device. Therefore, the design of every device is based on its application and product needs.

IC Design space:

The primary concern for IC design space has changed from area and speed to power, speed and complexity.

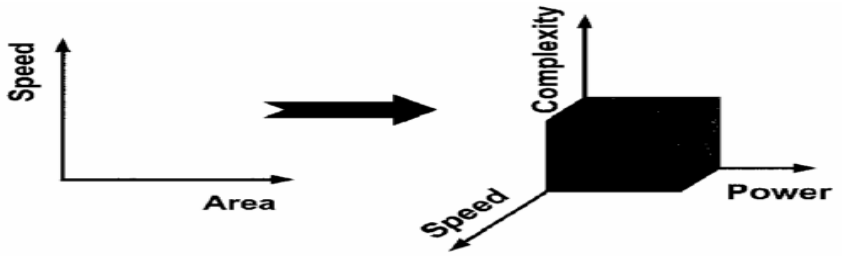

Fig. 1. IC design space

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As shown in IC design space, when complex circuits or high speed is required, the power consumption will be high. In a circuit, power consumption will be high at different stages and leakage power is one among the top causes of power loss because leakage power makes up to 50% of the total power consumption especially in latest high-performance microprocessors. Thus, leakage power has become the key for low-power design and so, different techniques for leakage power reduction are discussed here.

The paper is organised as follows: Section II deals with the power dissipation due to leakage, section III describes about the leakage reduction techniques where transistor stacking and self-adjustable voltage level circuit are discussed in-depth and section IV gives the conclusion.

II. POWER DISSIPATION DUE TO LEAKAGE

The total power dissipation could be expressed as

$P_{dissipation} = 1/2\ CV_{DD}^2.F.N + Qsc\ VDD.\ En + I_{leak}..\ V_{DD}$

The third term in the above equation represents static power dissipation due to leakage current (I_{leak}). This shows that the leakage power has a substantial effect over the power dissipation.

The following are the leakages in Nanoscale CMOS:
I1: Reverse bias pn junction (both ON & OFF)
I2: Sub-threshold leakage (OFF)
I3: Oxide tunneling current (both ON & OFF)
I4: Gate current due to hot carrier injection (both ON & OFF)
I5: Gate induced drain leakage (OFF)
I6: Channel punch through current (OFF)

The below figures shows the leakage currents in CMOS

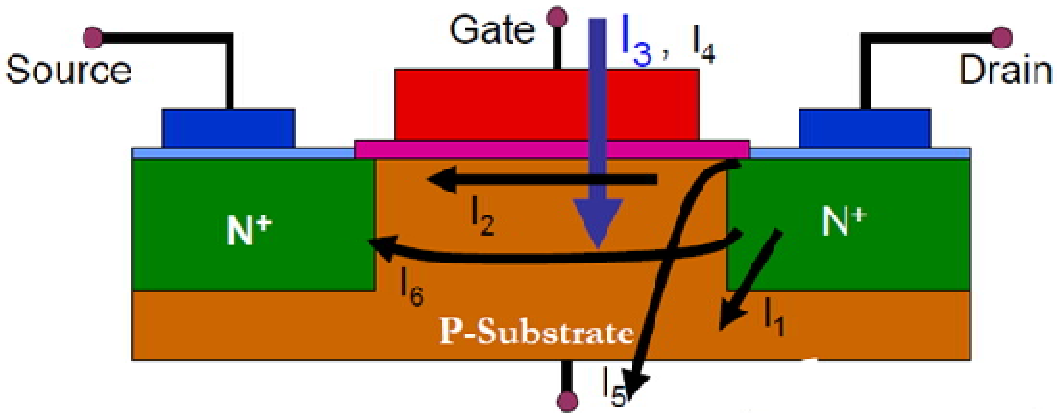

Fig. 2. Leakages in Nanoscale CMOS (Source: Roy proceedings of IEEE, 2007)

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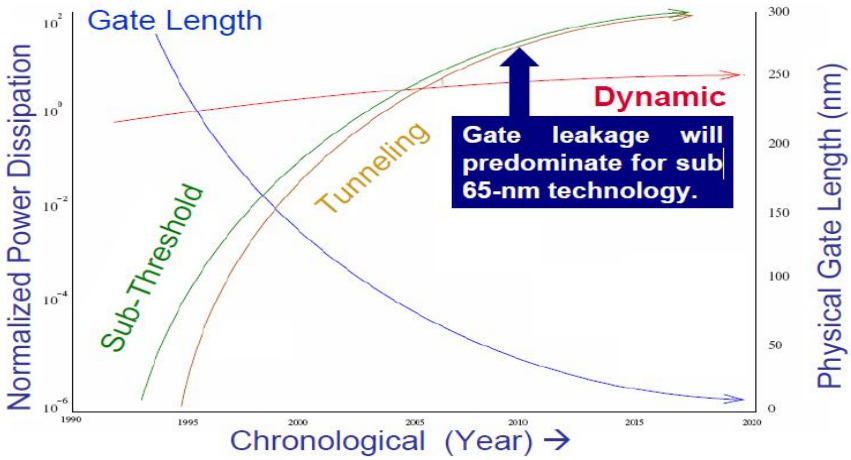

Fig. 3. Power redistribution graph (Source: Hansen 2004)

Among the 6 leakage components, sub-threshold leakage and gate leakage are dominant.

1) Sub threshold leakage current:

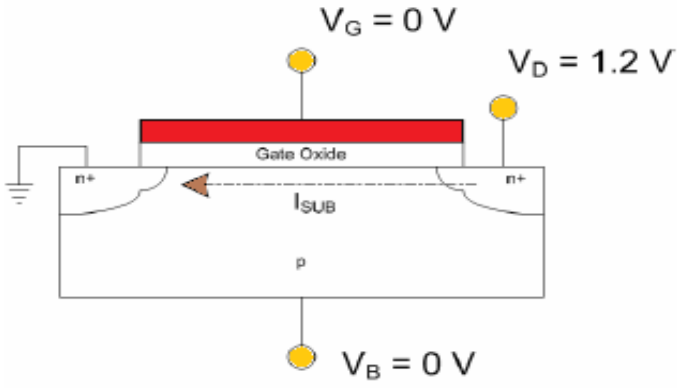

Fig. 4. Sub threshold current

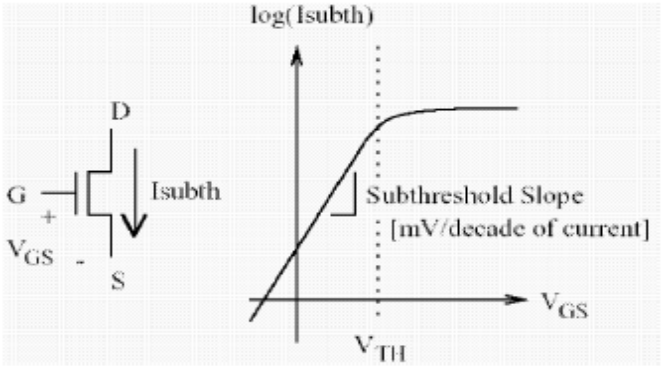

Fig. 5. Sub threshold leakage in a negative channel metal–oxide–semiconductor (NMOS) transistor.

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The sub-threshold leakage current mathematically could be given as:

$$I_{subthreshold} = I_0 \exp[(Vgs - Vt)/ (nVT)] [1 - \exp(- Vds/VT)]$$

$$I_0 = \mu eff\ Cox(W/L)VT2$$

μeff = electron/hole mobility,
Cox = gate capacitance per unit area,
W and L are width and length of the channel respectively,
Vt = threshold voltage,
n = sub-threshold swing co-efficient,
VT = thermal voltage,
Vgs = transistor gate to source voltage
Vds = drain to source voltage

2) Gate leakage components:

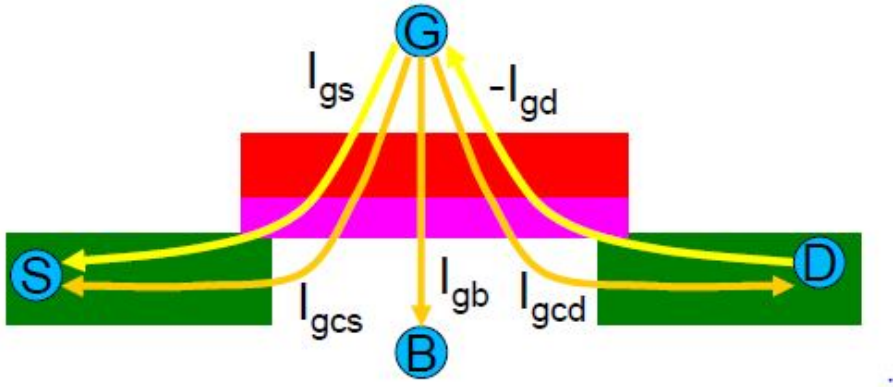

Fig. 6. Gate leakage components

Gate oxide tunneling current components in BSIM4.4.0 model.
Igs, Igd: Components due to the overlap of gate and diffusions
Igcs, Igcd: Components due to tunneling from the gate to the diffusions via the channel and
Igb: Component due to tunneling from the gate to the bulk via the channel. GBSDIgs-IgdIgcsIgcdIgb
Note: all the currents are with respect to gate.

This has become serious concern as gate oxide prevails in advanced CMOS processes. These oxides could degrade circuit performance by conducting leakage current through various direct-tunneling mechanisms. Recently, analytical gate leakage model with physical source/drain partition for MOSFET is developed.

III. LEAKAGE REDUCTION TECHNIQUES

Transistor stacking and self-adjustable voltage level circuit are the two leakage reduction techniques. These two techniques will be discussed in this section.

Transistor stacking:

Multi-Threshold Super Cut-off Stack (MTSCStack) technique is a new approach which uses high threshold and low threshold voltage transistors which is an effective technique to reduce leakage power in VLSI circuits.

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Techniques for leakage power reduction can be divided into following two categories: 1) state-saving techniques where circuit state (present value) is retained and 2) state-destructive techniques where the current Boolean output value of the circuit might be lost.

State-destructive techniques cut off transistor networks from supply voltage or ground using sleep transistors. Multithreshold CMOS (MTCMOS) technology uses high-Vth sleep transistors between pull-up networks and Vdd and between pull-down networks and ground while logic circuits use low-Vth transistors in order to maintain fast logic switching speeds. The sleep transistors are controlled by a sleep signal used for active or standby mode.

In active mode the sleep signal is high and the sleep transistors are turned on. Then the low VTH logic gates operate normally at high speed. During standby mode, sleep signal is low and sleep transistors are turned off. In this stage the leakage current reduces by using high VTH transistors. This stage will isolate the logic core with VDD and GND. This technique will lead to the destruction of state plus floating output voltage because of circuit state floating after sleep mode.

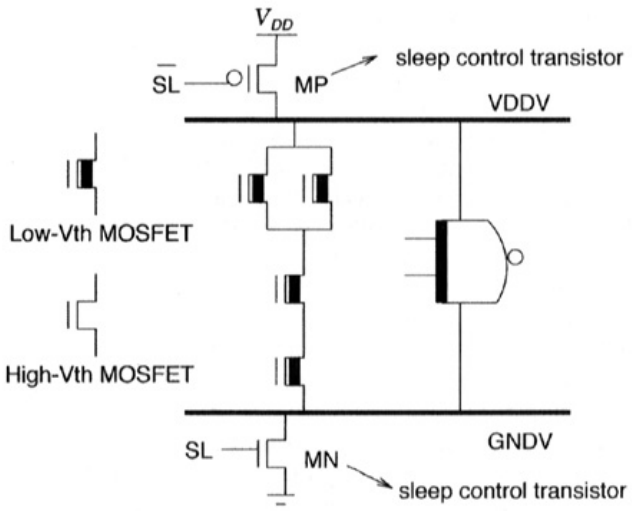

Fig. 7. Schematic Diagram of MTCMOS (Source: file.scirp.org)

An alternative technique which is similar to MTCMOS technique is Super Cut off CMOS (SCCMOS) technique. The sub-threshold leakage is dependent on the gate to source voltage of a MOSFET, depending on this by using slight negative gate voltage, the sub- threshold current reduced here.

SCCMOS differs from MTCMOS by using the sleep transistors have the same low threshold voltage as that of logic core. Here the usage of low VTH sleep transistors reduces the additional delay caused by high VTH sleep transistors during active mode. As SCCMOS technique also reduces the leakage and increases the performance it can't save the circuit logic state during standby mode. So the technique results in destruction of circuit logic state.

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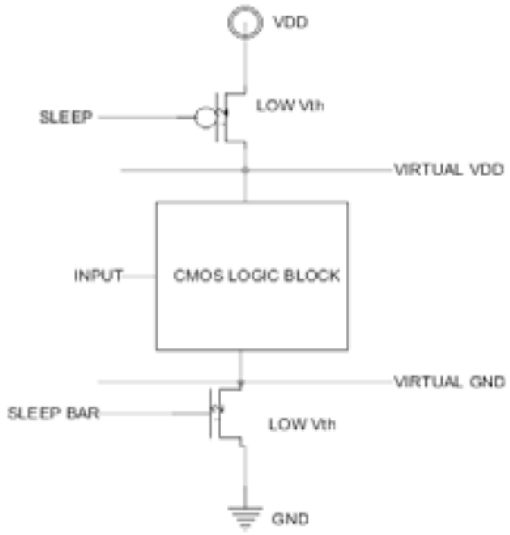

Fig. 8. SCCMOS

The other technique which is used for leakage power reduction in active mode is the stack technique. The stack effect results in substantial sub threshold leakage current reduction when two or more stacked transistors are turned off together

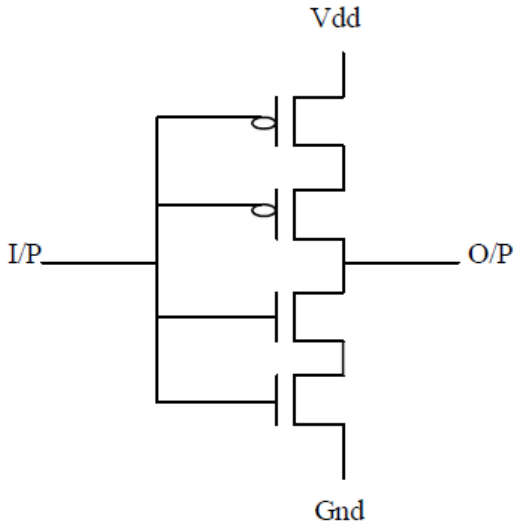

Fig. 9. Schematic diagram of Forced stack technique

Forced stack technique exploits the stack effect of transistors and reduces the leakage. This happens due to the reduction of gate to source voltage and reduction of DIBL coefficient due to lower drain to source potential thereby further reducing leakage. Forced stack technique fails in saving power consumption in standby mode. [7].

Finally, MTSCStack technique is a combination of MTCMOS, SCCMOS and Forced Stack techniques. In MTSCStack technique power consumption is reduced in active mode and retains the exact logic state in sleep mode.

Operation of MTSCStack technique is similar to the MTCMOS technique where the sleep transistors are turned on during active mode and turned off during sleep mode.

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In active mode when sleep transistors are turned on, the low VTH transistor work normally with high speed and reduces leakage power.

In standby mode when sleep transistors are turned off there is no connection between low VTH transistors and source as well as ground. Here the high VTH transistors will reduce the leakage power. NMOS transistors in parallel to the PMOS sleep transistors is the only source of VDD to the pull up network and PMOS transistors in parallel to the NMOS sleep transistors is the only source of GND to the pull down network .

Self-adjustable voltage level circuit (SAL):

In the below figure 9, the general self-adjustable voltage level circuit is shown, V_L is the output voltage and V_{dd} is the supply voltage applied to the load. When SL is low i.e., active mode, supply voltage is maximum. So, the transistor P1(PMOS) will be switched ON and the circuit operates more quickly.

On the other hand, when SL is high i.e., stand-by mode, the supply voltage will be slightly lowbecause V_{DD} passes through multiple N-MOS transistors.

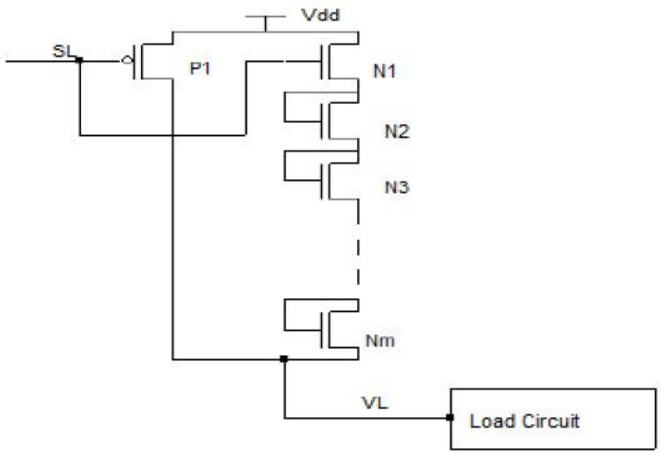

Fig. 10. Self-adjustable voltage level circuit

$$V_L = V_{dd} - Vn$$

Where Vn is the voltage drop of m weakly ON NMOS transistors. The drain to source voltage Vdsnof the OFF NMOS in the standby mode is expressed as

$$Vdsn = VL - Vss = VL$$

Vdsn can be decreased by increasing Vn that is increasing m, the number of NMOS transistors.When Vdsn is decreased, the drain- induced – barrier-lowering (DIBL) effect is decreased and thisin turn increases the threshold voltage Vtn of NMOS transistors. Consequently the sub thresholdleakage current of the OFF MOSFETs decreases, so leakage power is minimized, while data areretained.

IV. SIMULATION AND RESULTS

In this work, different designs of D-flipflops are implemented in CMOS process with 90nm technology. The leakage power dissipation are compared with and without the power reduction techniques. The net lists are extracted and simulated with B-SIM4 models of MOSFET[25]. The simulations are performed in HSPICE with a supply voltage of 1V at a temperature of 27 degrees centigrade and at a load capacitance of fF.

The simulation results of D-flipflop with and without transistor stacking technique are given in Table.1.
Table.2. shows the leakage power reduction using SAL technique .

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DFF Design using	Pleak (nW)		Percentage reduction in Pleak
	Without stack	With Stack	
Pass transistor	11.59	10.60	8.54
Transmission gates	21.58	18.93	12.27
GDI gates	17.66	15.77	10.70

Table.1. Simlation results of D-flipflop with and without transistor stacking technique

DFF Design using	Pleak (nW)		Percentage reduction in Pleak
	Without SAL	With SAL	
Pass transistor	11.59	9.13	21.23
Transmission gates	21.58	13.61	36.93
GDI gates	17.66	14.19	19.65

Table.2. Leakage power reduction with and without SAL technique

Hence according to above tables, reduction in Pleakis highest in DFF design using Transmission gates.

V. CONCLUSION

Previously, the dynamic power dissipation is quite high compared to leakage power, but because of scaling, the leakage power is now on-par with the dynamic power loss. Hence, the need for reducing leakage power is as important as the need for reduction in dynamic power. And so, the above delineated two techniques, Transistor stacking and self-adjustable voltage level circuit could alleviate the leakage power reduction. In future, more leakage power could be saved if new techniques better than the existing ones at gate level and block level are discovered.

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