



Power Estimation in FPGA

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ABSTRACT: The continuous decrease in feature size and the corresponding increase in chip density have made power consumption a major concern in VLSI design. The SIA has considered this as a major issue. Excessive power dissipation causes overheating which may lead to damage of chip or decrease in lifetime of the chip. Hence estimation of power dissipated at the design phase would enable easy redesign if necessary and also eliminate unnecessary cost of manufacturing. Also there is limited published work on FPGA Power modeling. The estimation of power at the design phase is complex since inputs are unknown, whereas estimation requires knowledge of inputs. Hence there is a need for an accurate power estimation model. In this paper we aim to estimate total power in an FPGA with increased fidelity.

KEYWORDS: FPGA Power modeling, SIA.

I. INTRODUCTION

In the recent years, a number of techniques have been proposed for estimation of power. Existing estimation techniques assume spatial independence i.e. that the inputs and internal signals are independent of each other. But practically most signals both primary as well as internal are correlated. Hence this assumption makes computation easy but does not give the accurate power. There is a need for a more efficient model in the aspect of improved computation time and accuracy. The pros and cons of the existing estimation techniques have been analysed [6]. Increased fidelity can be achieved by estimating power, assuming spatial correlation. Spatial correlation is the interdependence of the signals [4]. The goal is to compare the powers estimated using Hspice, simulation tool and the proposed model and tabulate the relative error to show the accuracy.

Moreover it has been found that FPGA vendors report power consumption as one of priority concerns among customers. Field-Programmable Gate Array (FPGA) devices are used for implementing digital applications. Unlike Application Specific Integrated Circuits (ASIC) they can implement various types of circuits without need for fabrication every time thus reducing the cost. They are rectangular arrays of logic cells (LC) connected by a programmable routing network. Each logic cell is responsible for implementing a logic function and/or a flip-flop. Compared to ASICs and other custom chips FPGA have long routing channels with significant parasitic capacitance. During high speed operations, switching activity on these long routing tracks cause significant power dissipation [3].

II. BACKGROUND

There are three power sources in FPGAs, namely, switching power, short-circuit power and static power. Total power for any design includes dynamic, static and glitch power. The first two types of power together are called dynamic power, and they can only occur when a signal transition happens. There are two types of signal transitions, namely functional transition and spurious transition. Functional transition is the necessary signal transition to perform the required logic functions between two consecutive clock ticks while spurious transition or glitch is the unnecessary signal transition due to the unbalanced path delays to the inputs of a gate [1]. Glitch power can be a significant portion of the dynamic power.

Switching power is the power consumed when necessary signal transition occurs to perform a particular logical function. Short-circuit power is the power consumed when a signal transition occurs at a gate output, when both the pull-up and pull-down transistors are conducting simultaneously for a short period of time [1][3].

Static power is also called as the leakage power. It is the power consumed when there is no signal transition for a gate or a circuit module. The leakage power in a nano-scale CMOS device includes reverse-biased leakage, sub-threshold leakage power, drain induced barrier lowering leakage, gate tunnelling leakage, gate induced drain leakage, etc [3].



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 10, October 2013

III. BRIEF OVERVIEW

The term power estimation generally means estimating the average power dissipation of a digital circuit. It can be done using two methods namely, Simulation approach and Probabilistic approach.

A. SIMULATION APPROACH

Most simple and direct approach of power estimation would be by simulation. That is to perform a circuit simulation of the design and monitor the power supply current waveform. The advantages of this technique are mainly its accuracy and generality. It can be used to estimate the power of any circuit, regardless of technology, design style, functionality, architecture, etc. The simulation results are directly related to the specific input signals used to drive the simulator [6].

But the disadvantages are that complete and specific information about the input signals is required, in the form of voltage waveforms. Hence these simulation-based techniques are strongly pattern-dependent. The power of a functional block needs to be estimated when the rest of the chip has not yet been designed, or even completely specified. In such a case, very little may be known about the inputs to this functional block, and complete and specific information about its inputs would be impossible to obtain.

B. PROBABILISTIC APPROACH

There are many ways of defining probability measures associated with the transitions made by a logic signal. There are mainly two kinds namely, signal probability, probability defined as the average fraction of clock cycles in which the steady state value of z is a logic high and transition probability defined as the average fraction of clock cycles in which the steady state value of x is different from its initial value. If a zero-delay model is assumed and the transition probabilities are computed, then the power can be computed as [6]:

$$P_{av} = 1/2T_c V_{dd}^2 \sum_{i=1}^n C_i P_t(x_i) \quad (1)$$

where T_c is the clock period, C_i is the total capacitance at node zz , and n is the total number of circuit nodes that are outputs of logic gates or cells. Since this assumes at most a single transition per clock cycle, then this is actually a lower bound on the true average power. In practice, signals may be correlated so that, for instance, two of them may never be simultaneously high. It is computationally too expensive to compute these correlations, so that the circuit input and internal nodes are usually assumed to be independent. We refer to this as a spatial independence assumption. Another independence issue is whether the values of the same signal in two consecutive clock cycles are independent or not. If assumed independent, then the transition probability can be easily obtained from the signal probability according to:

$$P_t(x) = 2P_s(x)P_s(x) = 2P_s(x)[1-P_s(x)] \quad (2)$$

A zero-delay model was assumed and a temporal independence assumption was made so that the transition probabilities could be estimated using signal probabilities. Signal probabilities supplied by the user at the primary inputs are propagated into the circuit assuming spatial independence and the power was computed [6].

We refer to the above approaches as probabilistic because probabilistic information is directly propagated into the circuit. To perform this, special models for circuit blocks (gates) must be developed and stored in the cell library.

IV. EXISTING TECHNIQUES

A. USING SIGNAL PROBABILITY

When a zero-delay model is assumed temporal as well as spatial independence is assumed. The user is expected to provide signal probabilities at the primary inputs. These are then propagated into the circuit to provide the probabilities at every node. The propagation of probabilities is performed at the switch-level, but this is not essential to the approach. The simplest way to propagate probabilities is to work with a gate-level description of the circuit. Thus if $y = \text{AND}(x_1, x_2)$, then it follows from basic probability theory [6],



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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$$P_s(y) = P_s(x_1) P_s(x_2) \quad (3)$$

provided x_1 and x_2 are (spatially) independent. Similarly, other simple expressions can be derived for other gate types. Once the signal probabilities are computed at every node in the circuit, the power is computed based on the temporal independence assumption.

B. PROBABILISTIC SIMULATION

This approach requires the user to specify typical signal behaviour at the circuit inputs using probability waveforms. A probability waveform is a sequence of values indicating the probability that the signal is high for certain time intervals, and the probability that it makes low-to-high transitions at specific time points. The transition times themselves are not random. This allows the computation of the average, as well as the variance, of the current waveforms drawn by the individual gates in the design in one simulation run. The average current waveforms can then be used to compute the average power dissipated in each gate and the total average power of the circuit.

The events are propagated one at a time, using an event queue based mechanism. Whenever an event occurs at the input to a gate, the gate makes a contribution to the overall average current that is being estimated, and generates an output event that is scheduled after some time delay [6][4].

C. USING TRANSITION DENSITY

The average number of transitions per second at a node in the circuit has been called the transition density, where an efficient algorithm is presented to propagate the density values from the inputs throughout the circuit. The average number of transitions per second at a node in the circuit has been called the transition density, where an efficient algorithm is presented to propagate the density values from the inputs throughout the circuit. If y is a Boolean function that depends on x , then the Boolean difference of y with respect to x is defined as [6]:

$$\frac{\partial y}{\partial x} = y \Big|_{x=1} \oplus y \Big|_{x=0} \quad (4)$$

If the inputs x_i to a Boolean module are (spatially) independent, then the density of its output y is given by:

$$D(y) = \sum_{i=1}^n P\left(\frac{\partial y}{\partial x_i}\right) D(x_i) \quad (5)$$

Given the probability and density values at the primary inputs of a logic circuit, gives the density at every node.

D. BDD APPROACH

The technique proposed attempts to handle both spatial and temporal correlations by using a BDD to represent the successive Boolean functions at every node in terms of the primary inputs. The intermediate values that the node takes before reaching steady state are not represented by this function. One disadvantage of this technique is that it is computationally expensive. Since the BDD is built for the whole circuit, there will be cases where the technique breaks down because the required BDD may be too big. As a result, this approach is limited to moderate sized circuits. The situation is actually potentially worse than this, because a BDD function must be built for every intermediate state and for their pair wise XOR functions. In cases where many intermediate transitions occur, even moderate sized circuits may be too big to handle [6].

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 2, Issue 10, October 2013

TABLE 1 COMPARISON OF EXISTING TECHNIQUES

APPROACH	TOGGLE POWER	SPATIAL CORRELATION	SPEED
SIGNAL PROBABILITY	NO	NO	FAST
PROBABILISTIC SIMULATION	YES	NO	FAST
TRANSITION DENSITY	YES	NO	FAST
BDD	YES	YES	SLOW

V. PROPOSED MODEL

Our work describes a novel approach for total power estimation in FPGAs while considering spatial correlation among the different signals in the design including glitch. The signal probabilities under spatial correlations are used to properly model the dynamic power dissipation. The model has been simplified into modules and integrated. The modules are:

- Creating a linked list for the various bench mark circuits in ISCAS85 format to parse the circuit.
- Creating an input file to feed probability information assuming spatial correlation and obtain static and transition probability at each of the nodes in the circuit.
- Implement an algorithm that takes the correlation co-efficient into account using nodal information to compute average power.
- Compute power for the a set of benchmarks using the above proposed method
- Compute power using a simulation tool - Quartus II for the same set of benchmark circuits.
- Assuming an k-input LUT FPGA architecture estimate power in Hspice for the same set of benchmark circuits.
- Compare the powers estimated using simulation tool, proposed model and Hspice and tabulate the relative error.

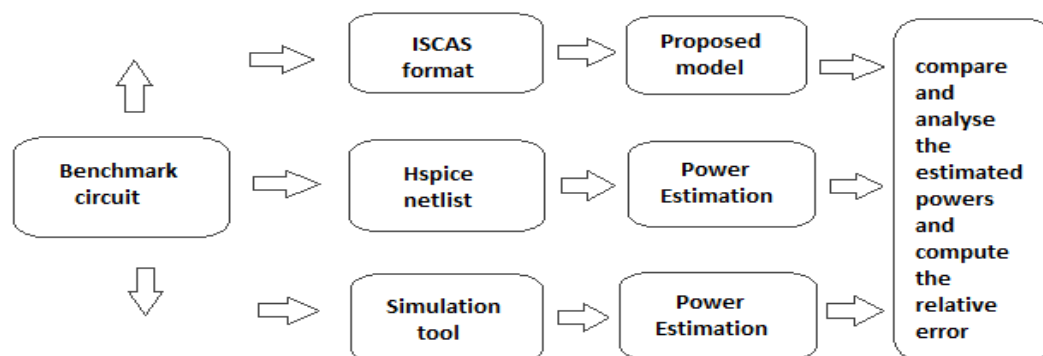


Fig 1 Block diagram of the work

VI. FUTURE WORK

An algorithm for glitch power estimation can be incorporated to the model to increase the fidelity. Firstly glitch probability must be calculated. The algorithm consists of three phases: glitch generation, glitch propagation, and glitch termination. Starting with the logic cells connected to the primary inputs, and parsing the circuit in a depth-first



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 2, Issue 10, October 2013

strategy, glitches are generated at the output of the logic cell such that the differences in the arrival times is larger than the intrinsic delay of the logic implemented .

When a glitch from the output of one cell is fed to the input of the next cell, that glitch propagates only if the logic function of the second cell allows the glitch to. The probability that certain glitch will propagate is equal to the probability of the glitch multiplied by the conditional probabilities of the inputs needed to propagate the glitch. The proposed glitch propagation algorithm keeps on parsing the circuit by the depth first search until the probability of glitch propagation is less than 0.01, at which point the glitch is dropped i.e. glitch termination. Using this probability information glitch power can be calculated in an approach similar to earlier case.

VII.RESULTS

Firstly, a simulation tool such as Quartus II is used to estimate the total power using the PowerPlay Power Analyser tool available in the software for a set benchmark circuits of ISCAS85 format. The results have been tabulated as in TABLE 2. Moreover, the algorithm for obtaining signal probabilities and the linked list for parsing the various benchmark circuits and obtain nodal information has been successfully completed. Apart from the above mentioned work other modules are being currently pursued.

TABLE 2 QUARTUS II – POWER ESTIMATION

BENCKMARK CIRCUITS	TOTAL POWER(in mW)
C17	323.74
C432	324.98
C499	326.10
C6288	325.78
C5315	334.44

VIII.CONCLUSION

It is believed that after a complete analysis of the pros and cons of existing techniques the proposed algorithm manages to estimate power with greater accuracy though there is a tradeoff with the computation time. On the other hand, comparison is done between the power estimated with glitches considered and glitches ignored to observe the percentage error.

The presented techniques are weakly pattern dependent since the user is expected to supply some information on the typical behavior at the circuit inputs. But the method is fast which is very important since VLSI designers are interested in power estimation of large circuits.

Our model could effectively find its place in FPGA based industries that are looking forward for an efficient model for estimation of power.

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ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 10, October 2013

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