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# Comparative Analysis of CMOS and Fin FET based Ripple Carry and Carry Save Adders

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**ABSTRACT:** Adders are basic digital circuit that performs addition. There are many adders like ripple carry and carry save adders used for multiple bit addition in ALU's. These adders based on CMOS technology requires more power. FinFET technology is used to reduce power consumption and propagation delay in ripple carry & carry save adders since CMOS technology consumes more power and results in longer propagation delays. Both circuits are designed with LT Spice tool with 45nm FinFET technology. The proposed Ripple carry adder and Carry save adder is compared with some CMOS technology nodes based on power consumption, delay, and power delay product. The proposed Ripple carry adder achieves 52.32% improvement in speed than the CMOS Ripple carry adder and for Carry save adder achieves 59.31% improvement in speed than the CMOS Carry save adder when simulated with 45-nm technology and 1V. When compared between the proposed Carry save adder is 18.62% faster than the other adder. It also found that the proposed adder cell exhibits excellent driving capability when operated at low voltages.

**KEYWORDS:** Carry Save Adder, FinFET, Ripple Carry Adder

## I. INTRODUCTION

The adders play an important role in complex arithmetic and computational circuits such as multiplier, comparator, and parity checkers. In recent years, many approaches have been proposed to implement a low power full adder. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems. The XOR-XNOR circuits are basic building blocks in various circuits especially arithmetic circuits (adders & multipliers), comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector. Adder is the basic building block of complex arithmetic circuits like addition, multiplication, division, exponentiation and so forth. The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes (ie., channel widths) and the intra cell wiring capacitances. Circuit size depends upon the number of transistors, their sizes and complexity. Some use one logic design for the whole full adder while the other uses more than one logic design for their implementation. Power is one of the vital resources, hence the designers try to reduce the power while designing a system. Power dissipation depends upon the switching activity, node capacitances (made up of gate, diffusion, and wire capacitances), and control circuit size. By selecting proper W/L ratio can be minimize the power dissipation without decreasing the supply voltage. The proposed full adder designed with FinFET transistors which can eliminates scaling problem. The proposed circuit consumes less power and operates at low supply voltages. Comparing with existing adders CMOS adders the characteristic of the proposed full adder shows that the design has the best delay, PDP, total power dissipation and area. Due to the minimum delay, the adder core greatly improves the overall performance for a large scale of a multi- 3 bit adder.

Several logic styles have been used in the past to implement the full adder cell. Each logic style has its own advantages and disadvantages. Standard static CMOS full adder (C-CMOS) is based on regular CMOS structure with pull up and pull-down transistors. This adder provides full output voltage swing against voltage and transistor sizing. The limitations of this design are its larger area and slower speed due to the availability of PMOS devices and larger input capacitance of the static CMOS logic gates. On the other hand, complementary pass transistor logic (CPL) is fast and also provides full voltage swing output. CPL adder is based on dual rail structure and requires 32 transistors. But it has larger power consumption because of the presence of static inverter and lot of internal nodes. The other adders are designed using hybrid logic styles and are called hybrid adder. These adders are designed with a combination of more than one logic style to enhance the overall performance of the system. The main focus of hybrid. logic style is to reduce the number of transistors and power dissipating nodes of the adder cell. Hybrid pass logic with static CMOS (HPSC) is an example of hybrid adder. HPSC provides full output voltage swing and has good output drive capability. The

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limitation of this adder 2 is its higher propagation delay. On the other hand, hybrid adder is a good choice in terms of power consumption and speed than HPSC but at the cost of increased number of transistors in the design. However, hybrid CMOS full adder is faster than HPSC at all supply voltages. But its delay is increased with varying the load. Full adder proposed in reference 1 is designed with CMOS transistors and consumes more power. In this adder, signals have high ripples at the output, and it makes the design inefficient at the scaled technology.

The conventional CMOS technology-based adders consume more power, and it has lower switching speed. Due to this it has low performance and more propagation delay. As nano-meter process technology advances, CMOS technology is rapidly reaching its limits. The proposed Ripple Carry adder & Carry Save adder using FinFET transistors. Due to fast switching speed, it's propagation delay is reduced. Power consumption is reduced by the low leakage current. By using FinFET, power supply is reduced, and performance can be increased. Speed is increased and delay is reduced.

**Adders**

This section presents theoretical review on Ripple carry adder circuit, as well as the description of the traditional approach to design various types of adders, which includes the summary of Ripple carry adder circuit and an overview of existing adders. We also explore some of the existing designs in reference [1] with CMOS technology currently used in the Ripple carry adder design together with the experimental results obtained when simulated, e.g., the average power consumption of 11.325µW, and was found to be used 45nm CMOS technology. In reference [3] we explore some of the existing designs with CMOS technology currently used in the full adder design together with the experimental results obtained when simulated, e.g., the average power consumption of 1.1055µW, and was found to be extremely low for 0.8-V supply for CMOS technology. In conclusion, there are only limited full adder designs consumes lower power and delay. We consider low power and lower propagation delay, which has must be explored in future.

**14T Conventional CMOS Full Adder**

This CMOS full adder consists of both PMOS and NMOS in the form of pull-up and pull- down network. Figure 1 shows the schematic diagram of 14T conventional CMOS full adder cell. It was observed that the output waveforms are inappropriate. It also observed that the full adder with CMOS technology has voltage swings at the output.

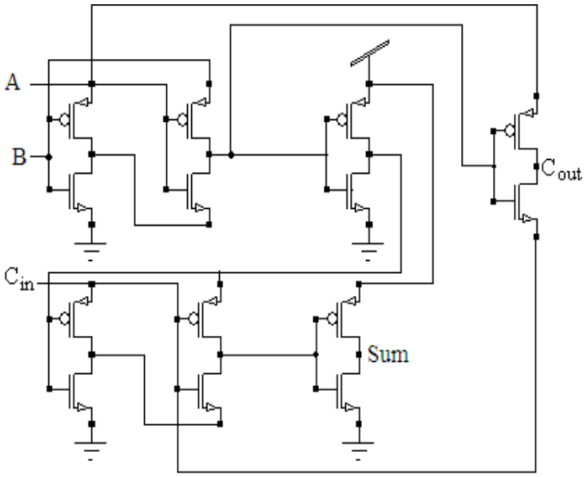


Figure 1: 14T conventional CMOS full adder

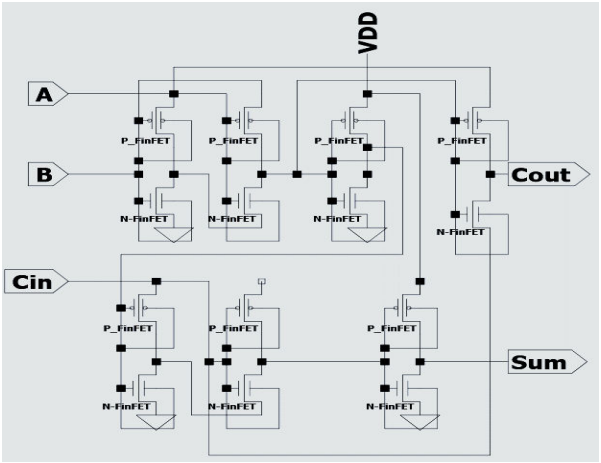


Figure 2: Schematic of 14T FinFET full adder.

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**14T FinFET Full Adder**

To overcome the scaling issue faced by MOSFET, full adder cell is designed using FinFET. FinFET allows further scaling to nano-meter technology. This full adder cell consists of both nFET and pFET to replace the complementary MOS logic. The Figure 3.4 gives the schematic diagram of 14T FinFET full adder cell. The circuit consists of A, B, Cin as inputs and Sum, Cout as outputs. The total power consumption is responsible of inverters and XNOR which causes output sum and carry. In the proposed full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extent with avoiding the voltage degradation possibility. the XNOR uses four transistors to get better logic swing compared with previous XNOR circuits.

**Ripple Carry Adder**

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurance of the corresponding output. Consider a NOT gate, When the input is “0” the output will be “1” and vice versa. The time taken for the NOT gate’s output to become “0” after the application of logic “1” to the NOT gate’s input is the propagation delay here. Similarly, the carry propagation delay is the time elapsed between the application of the carry in signal and the occurance of the carry out (Cout) signal. Figure 3 shows Ripple Carry Adder. A Ripple Carry adder (RCA) consists of n full adders connected in a chain. The inputs are two n-bit numbers, A and B, and a carry-in bit, Cin. The outputs are an n-bit sum, S, and a carry-out bit, Cout. Each full adder takes three inputs: a bit from A, a bit from B, and the carry-in bit. It produces two outputs: a sum bit and a carry-out bit. The sum bit is passed on to the next full adder in the chain, while the carry-out bit is used as the carry-in bit for the next full adder.

The final full adder in the chain produces the least significant bit of the sum, as well as the carry-out bit. This carry-out bit can be used as the carry-in bit for another RCA, allowing for fast and efficient addition operations on large, multi-bit numbers.

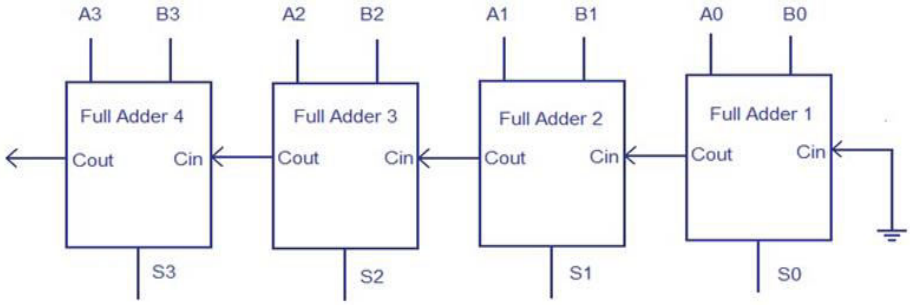


Figure 3: 4-bit Ripple Carry Adder

**Carry Save Adder**

Carry Save adder (CSA) is a type of adder used in digital circuits for adding multiple binary numbers. Unlike ripple carry adders, which can be slow for large, high-speed computations due to the delay caused by the carry bit having to ripple through the adder, Carry Save adders provide a fast and efficient way to add multiple numbers in parallel.

Carry save adder consists of 5-Full adders and 3-Half adders shown in figure 4 Since it uses half adders, it reduces consumption of power and improves speed and also reduces area by using half adders which requires less number of transistors. Since it uses half adders, it reduces consumption of power and improves speed and also reduces area by using half adders which requires less number of transistors. Carry save adder is consists of three or more n-bit binary numbers. Carry save adder is similar as full adder. Here we are computing sum of 3-bit binary numbers, so we take 3 full adders at first stage. Carry save unit consists of 6 full adders, each of which computes single sum and carry bit based only on the corresponding bits of the two input numbers. One of the main advantages of Carry Save adders is their speed and efficiency in performing arithmetic operations on large, multi-bit numbers. They are particularly useful

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for multiplication and division operations, where the carry-out bits can be used as the carry-in bits for another CSA, allowing for fast and efficient computation.
However, one of the main disadvantages of CSAs is their complexity and cost compared to other types of adders. They require more circuitry.

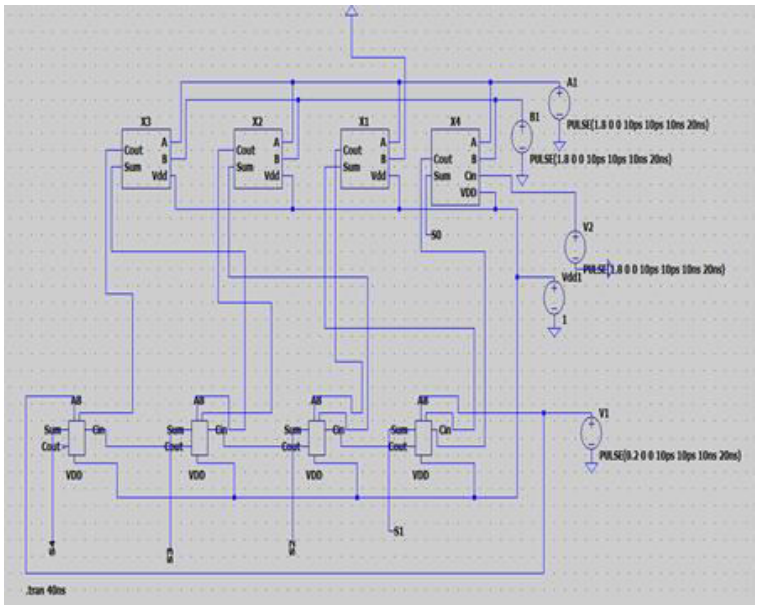


Figure 4: Schematic of 4-bit Carry save adder.

## II. SIMULATION RESULTS AND COMPARISON

The simulation of the circuits CMOS and FinFET based Ripple carry and Carry save adders are carried out 45-nm technology using spice tool. Both the adders are simulated using the common simulator. The simulations are performed on supply voltage 0.8 V and 1V. The proposed adders designed with FinFET technology is compared in terms of power consumption, propagation delay and Power Delay Product (PDP) with the existing CMOS adders at 45-nm technology Table 1 and 2 respectively. Adders are analyzed under no-load condition. The proposed Ripple carry adder achieves 52.32% improvement in speed than the CMOS Ripple carry adder and for Carry save adder achieves 59.31% improvement in speed than the CMOS Carry save adder when simulated with 45-nm technology and 1V. When compared between the proposed Carry save adder is 18.62% faster than the other adder. This makes the proposed designs are better consideration for low power and high-speed VLSI applications. Figure 5 & 6 shows that the simulated output waveforms of prproposed proposed 4-bit Ripple carry adder and Carry save adder respectively, their output Sum = 1101, Cout = 1. It is proposed that this adder eliminates ripples at the output and exhibits exact values compared with the input combinations of the adder. The simulation part which is performed of existing and proposed adder circuits at the same design parameters as shown in Table 1 & 2, it shows the calculation of average power, delay, power delay product of the proposed adders along with the existing adders. These results are calculated by using SPICE tool at 45nm MOSFET technology and it is clearly seen that the power consumption and propagation delay of proposed circuit is better than the existing CMOS based adders. It was the proposed adder circuits eliminates ripples at the output and exhibits exact values compared with the input combinations of the adder.

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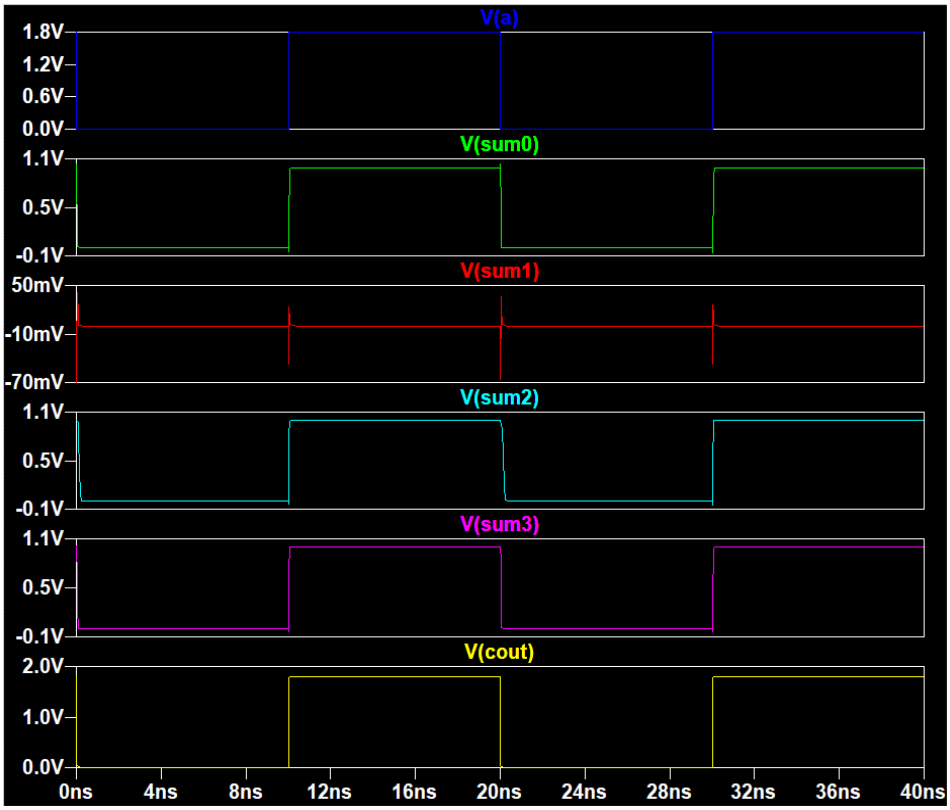


Figure 5: Output waveforms of 4-bit FinFET Ripple carry adder circuit

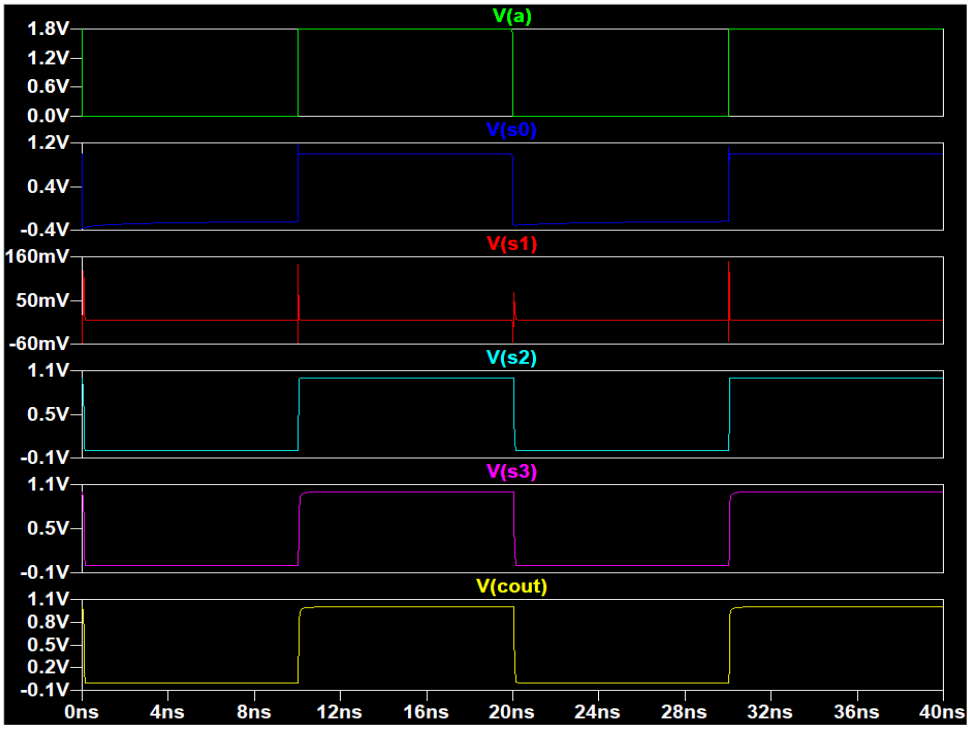


Figure 6: Output waveforms of 4-bit FinFET Carry save adder circuit

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Table 1: Power, Delay and power and delay product comparison of RCA & CSA using CMOS Technology

| Adder Type | Power (µW) | Delay (ps) | Power Delay Product (fJ) |
|---|---|---|---|
| RCA 4-bit | 46.8 | 168 | 7.86 |
| RCA 8-bit | 93.6 | 180.4 | 16.8 |
| CSA 4-bit | 110.2 | 152.3 | 16.78 |
| CSA 8-bit | 168.4 | 172 | 28.96 |

Table 2: Power, Delay and power and delay product comparison of RCA & CSA using FinFET Technology

| Adder Type | Power (µW) | Delay (ps) | Power Delay Product (fJ) |
|---|---|---|---|
| RCA 4-bit | 2.5 | 84 | 0.21 |
| RCA 8-bit | 3.44 | 86 | 0.3 |
| CSA 4-bit | 8.2 | 62 | 0.5 |
| CSA8-bit | 36.7 | 70 | 2.5 |

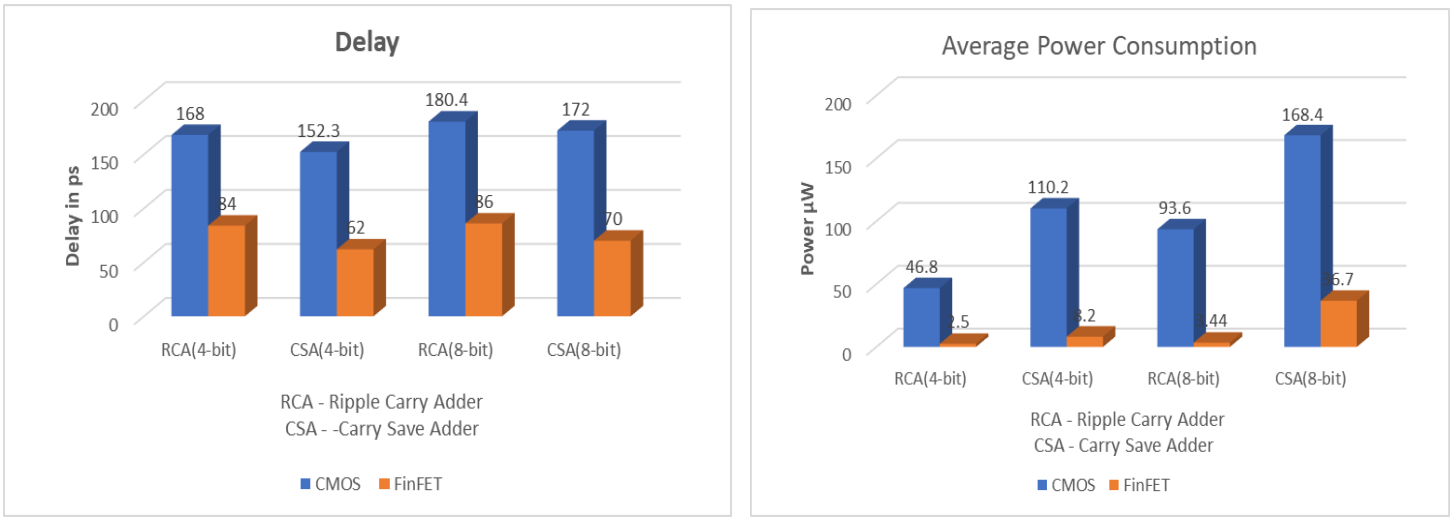


Figure 7: Comparison of delay and power consumption for CMOS and FinFET based RCA & CSA

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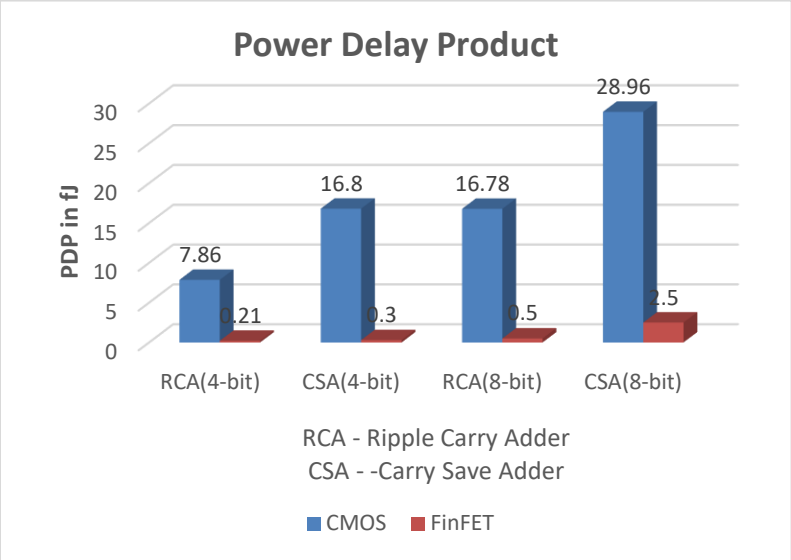


Figure 8: Comparison of power and delay product for CMOS and FinFET based RCA & CSA

## III. CONCLUSION

In this project, design and analysis of ripple carry and Carry save adders based on CMOS & FinFET technology have been presented. Simulations are carried out on spice tool using 45-nm technologies to evaluate the new design and existing designs. Results show that the proposed design has high performance and best PDP in comparison with many existing full adder cells. Consequently, this new design is found appropriate at low voltages and has good output levels. This shows that proposed design can be a good choice in the future at scaled technology by using FinFET. It is also verified through simulation results that the proposed design performs well under the projected lower threshold voltage and temperature.

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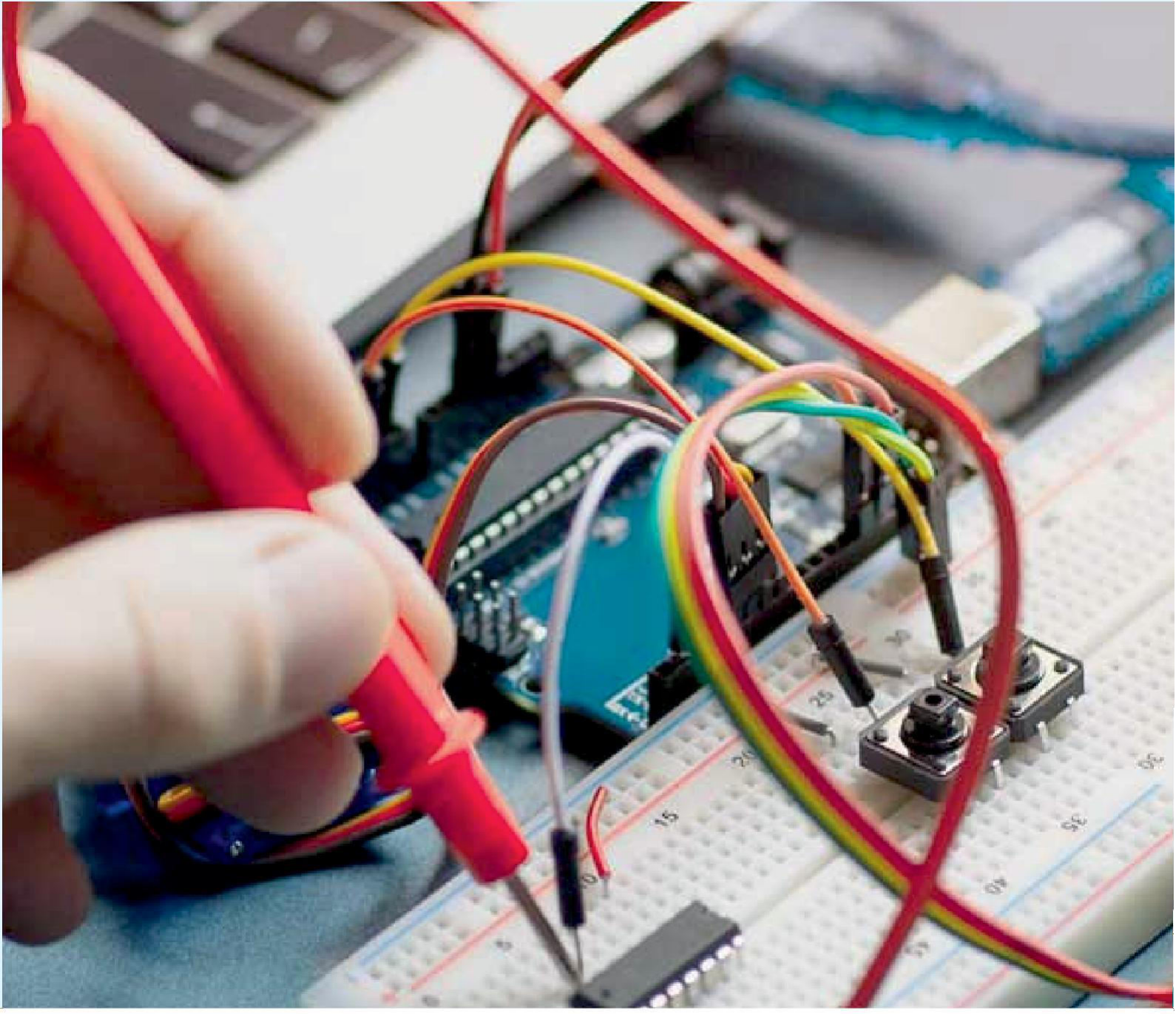

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