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Efficiency of DC-DC Switching Power Converter in CCM and SDCM of Operation

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ABSTRACT: This paper presents an efficiency comparison of DC-DC switching power converter in continuous current mode (CCM) and in synchronous discontinuous current mode (SDCM) of operation. Non-isolated bidirectional synchronous DC-DC switching power converter is considered for this study. The circuit is made to operate in CCM and SDCM of operation, which depends on inductor value of the converter. SDCM of operation occurs when the circuit inductor value is smaller than critical inductor value and CCM of operation occurs when the circuit inductor value is larger than critical inductor value. CCM of operation has the advantage of less inductor current ripple. But it increases the inductor size, cost, weight and converter size. SDCM of operation have many advantages like the inductor size, cost, weight and converter size can be minimized, minimum turn-on loss, low diode reverse recovery loss, minimum inductor current parasitic ringing effect, and high power density. But it has large turn-off loss and increases inductor current ripple. A series of MATLAB scripts are executed to find inductor value for SDCM and CCM of operation and to select snubber capacitor for maximum efficiency.

KEYWORDS: CCM, SDCM, buck, boost, bidirectional, non-isolated, MATLAB script.

I. INTRODUCTION

DC-DC switching power converters are power electronic circuits which transfer one level of electrical voltage into another level by switching action. These converters are implemented in numerous fields like Uninterrupted Power Supplies (UPS), telecommunication purpose, DC machine drives, aerodynamics, hybrid electric and fuel cell vehicles [1][2], renewable energy system etc. The function of a DC-DC converter is to give a constant DC output voltage from a given input voltage. The converter is typically required to control the DC output voltage given a range of load currents drawn and/or range of input voltage applied. Ideally the DC output is to be clean, that is with ripple current or voltage held below a specified level. Furthermore, the load power is to be delivered from the source with some specified level of efficiency. Power inductor selection is an important step to achieving these goals. Inductance is calculated to provide a certain minimum amount of energy storage and to reduce output current ripple. Using less than the calculated inductance causes increased AC ripple on the DC output. Using much greater or much less inductance may force the converter to change between continuous and discontinuous modes of operation. A smaller inductor value enables a faster transient response; it also results in larger current ripple, which causes higher conduction losses in the switches, inductor, and parasitic resistances. The smaller inductor also requires a larger filter capacitor to decrease the output voltage ripple [3]. The turn off loss of the switch induced by SDCM of operation is minimized by connecting snubber capacitor across the transistor switch. A snubber is an energy-absorbing circuit used to eliminate voltage spikes caused by circuit parasitic inductance when a switch opens. Design process of snubber circuit for DC-DC converter and six topologies of snubber circuits were investigated in simulation tests [4]. Before the switch is turned ON, snubber capacitor requires certain amount of energy must be stored in the inductor to discharge the capacitor energy [5]. Complementary gate control signals are used to control the ON and OFF of main and auxiliary switch. SDCM of operation due to complementary control gate signal scheme, minimum turn on loss of the transistor switch and low diode reverse recovery loss are achieved. Thus the Zero Voltage Resonant Transition (ZVRT) of transistor switch is realized, both turn on and turn off loss is minimized and also removes the parasitic ringing in inductor current. This paper proposes an inductor selection for CCM and SDCM of operation, and for snubber capacitor optimization, for this a serial of MATLAB scripts are executed. Finally efficiency comparison between CCM and SDCM of operation is performed.

II. CIRCUIT TOPOLOGY

A non-isolated synchronous bidirectional switching DC-DC power converter technology is to combine a buck, boost and bidirectional mode of operation. Complementary gate signal control scheme is used to control the ON and OFF of



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transistor switches. The converter is operated in CCM and SDCM of operation. SDCM of operation decreases the inductor size, cost and weight of the converter. The SDCM of operation introduces more turn-off loss due to the main switch turn off during twice or higher load current [6]. This is one of the drawback of the inductor size reduction. The inductor current parasitic ringing will be caused by the oscillation of inductor with device output capacitance during turn off period of switch [7]. This issue due to SDCM of operation will affect the efficiency. The snubber capacitor added across the transistor switch is to reduce turn off loss. For zero turn-on loss the energy stored in the capacitor need to be discharged before the switch is turned ON, thus the Snubber capacitor requires certain amount of energy must be stored in the inductor to discharge the capacitor energy before the device is turned ON. Thus the Zero Voltage Resonant Transition (ZVRT) of transistor switch is realized. The main advantage of the SDCM of operation is minimum turn-on loss, thus low diode reverse recovery loss is achieved and also removes the parasitic ringing in inductor current. Thus both turn-on and -off losses are minimized. The advantage of CCM of operation is less inductor current ripple, but it increases the inductor size, cost and converter weight.

Fig.1 shows the circuit topology. When $V_H = DC$ source voltage and $V_L = 0$ voltage, the circuit will act as buck mode with R_2 act as load and R_1 is the internal resistance of V_H . When V_H =0 V and V_L =DC source voltage, the circuit is in boost mode with R1 as a load and R2 is the internal resistance of VL. In buck mode the inductor average current is positive and in boost mode it is negative. In bidirectional mode of operation, $V_{\rm H}$ and $V_{\rm L}$ are the source voltage at high side (V_1) and at low side (V_2) voltage respectively, R_1 is the internal resistance of V_H , R_2 is the load resistance at low voltage side. C_H and C_L are the input and output capacitors to smooth the load current and load voltage, its value is 150 μ F. Q_1 and Q_2 are MOSFETs with 35 m Ω turn-on resistances, acts as switches with body diode D_1 and D_2 respectively. C_1 and C_2 are snubber capacitors. L is the inductor with effective series resistance R_{LP} of 36 m Ω .

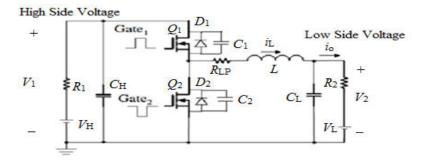


Fig.1 Circuit topology

III. INDUCTOR SELECTION

The critical inductor (L_{cr}) value, given in equation (1) [8] allows the converter operating under the boundary condition between SDCM and CCM of operation.

$$L_{cr} = \frac{1}{2} \cdot \frac{V_{in} - V_{out}}{P_o} \cdot \frac{V_{out}^2}{V_{in}} \cdot T_s$$
 (1)

Where V_{in} is the input voltage, V_{out} is the output voltage, P_o is output power and T_s is the switching frequency.

The inductor ripple current (ΔI_L) [9] and the inductor conduction loss (P_L) [10] are given in equation (2) and (3) respectively.

$$\Delta I_{L} = \frac{1}{2} \cdot \frac{V_{in} - V_{out}}{L} \cdot \frac{V_{out}}{V_{in}} \cdot T_{s}$$
 (2)

$$P_{L} = I_{RMS_L}^{2}.R_{LP}$$
 (3)

Where R_{LP} is the effective series resistance (ESR) of the inductor L and I_{RMS L} is the rms inductor current given in equation (4)

$$I_{RMS_L}^2 = I_L^2 + \frac{\Delta I_L^2}{12} \tag{4}$$

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Where I_L is the inductor average current.

The different test cases of buck, boost and bidirectional mode of operation is given in Table 1. A series of MATLAB script are executed, to find minimum inductor value for CCM and SDCM of operation. The results are tabulated in Table 2. The switching time considered is 0.02 ms. From the Table 2, it is observed that, the minimum and maximum inductor value at boundary condition is 12.65 µH and 44.42 µH and their corresponding power loss are 5.6 Watt and 8.77 Watt respectively. Therefore the required minimum inductor value to make the converter to operate in SDCM of operation for different test cases in different modes of operation must be less than 12.65 µH. Hence 10 µH is considered in circuit topology module which ensures SDCM of operation in all the three modes of operation in different test cases. This inductor conduction loss lies in the range of 5.85 Watt to 43.76 Watt for different test cases in SDCM of operation. For CCM of operation the required inductor value must be greater than 44.42 µH. Hence 50 µH is considered which ensures CCM of operation in all the three modes of operation in different test cases. This inductor conduction loss lies in the range of 5.21 Watt to 32.85 Watt for different test cases in CCM of operation.

Table 1 Test cases for buck, boost and bidirectional mode of operation

Mode of	Case	V_{H}	$V_{\rm L}$	R_1	R_2	I*	f_{sw}
Operation		(V)	(V)	(Ω)	(Ω)	(A)	(KHz)
	1	250	0	10m	10	15	50
Buck	2	250	0	10m	10	20	50
	3	250	0	10m	5	20	50
	4	270	0	10m	10	15	50
	1	0	50	18	10m	-12	50
	2	0	60	18	10m	-12	50
Boost	3	0	60	18	10m	-16	50
	4	0	60	9	10m	-12	50
		250	110	10m	2	30	50
	1	250	110	10m	2	-20	50
Bidirectional		250	110	10m	1	30	50
	2	250	110	10m	1	-20	50
		260	110	10m	2	30	50
	3	260	110	10m	2	-20	50

Table 2 Inductor Selection

Case	L_{cr}	Bour	ndary	SDCM of operation		CCM of operation	
*	(μH)	Conc	lition				
		ΔI_{Lcr}	P_{Lcr}	$\Delta I_{L\text{-}10\mu H}$	$P_{L-10\mu H}$	$\Delta I_{L-50\mu H}$	$P_{L-50\mu H}$
		(A)	(W)	(A)	(W)	(A)	(W)
1	39.97	15	8.77	59.96	18.88	11.99	8.53
2	19.94	20	15.60	39.89	19.17	7.97	14.59
3	29.99	20	15.60	59.98	25.19	11.99	14.83
4	44.42	15	8.77	66.64	21.42	13.32	8.63
1	21.79	11.79	5.60	25.70	7.16	5.14	5.26
2	23.77	11.82	5.60	28.12	7.55	5.62	5.27
3	20.57	15.69	9.95	32.30	12.34	6.46	9.34
4	12.65	11.82	5.60	14.97	5.85	2.99	5.21
	18.10	30	35.10	54.30	41.24	10.86	32.75
1	25.20	20	15.60	50.40	22.02	10.08	14.70
	20.51	30	35.10	61.54	43.76	12.30	32.85
2	28.80	20	15.60	57.60	24.35	11.52	14.79
	* 1 2 3 4 1 2 3 4 1 1	* (µH) 1 39.97 2 19.94 3 29.99 4 44.42 1 21.79 2 23.77 3 20.57 4 12.65 18.10 1 25.20 20.51	* (μH) Conc ΔI_{Lcr} (A) 1 39.97 15 2 19.94 20 3 29.99 20 4 44.42 15 1 21.79 11.79 2 23.77 11.82 3 20.57 15.69 4 12.65 11.82 18.10 30 1 25.20 20 20.51 30	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	* (μH) Condition AI _{Lcr} P _{Lcr} AI _{L-10μH (A) (W) (A) 1 39.97 15 8.77 59.96 2 19.94 20 15.60 39.89 3 29.99 20 15.60 59.98 4 44.42 15 8.77 66.64 1 21.79 11.79 5.60 25.70 2 23.77 11.82 5.60 28.12 3 20.57 15.69 9.95 32.30 4 12.65 11.82 5.60 14.97 1 8.10 30 35.10 54.30 1 25.20 20 15.60 50.40 20.51 30 35.10 61.54}	* (μH) Condition AI_{Lcr} P_{Lcr} $AI_{L-10\mu H}$ $P_{L-10\mu H}$	* (μH) Condition AI_{Lcr} P_{Lcr} $AI_{L-10\mu H}$ $AI_{L-50\mu H}$ AI_{L-50



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	19.58	30	35.10	58.76	42.75	11.75	32.81
3							
	25.57	20	15.60	51.15	22.25	10.23	14.71

^{*} Test cases as in Table 1, for different values of V_H, V_L, R₁, R₂, and I*

IV. SNUBBER CAPACITOR SELECTION

To minimize the turn-off loss in larger extent, larger value of snubber capacitor is required which minimizes drain current during turn-off period, but it may lead to more turn-on loss, because it will not discharge fully during turn-on period. The snubber capacitor is selected in such a way that it must minimize total turn-on, turn-off and snubber capacitor loss. During switch turn ON time, capacitor voltage fully discharges when the inductor stored energy is greater than the capacitor energy storage ability. This leads to minimum turn ON loss. The charge balance of CV^2 and $\frac{1}{2}LI_L^2$ is used for snubber capacitor design as given in equation (5) for minimum turn ON loss

$$C.V^2 \le \frac{1}{2}.L.I_L^2$$
 (5)

The above equation is modified for snubber capacitor value as given in equation (6) to minimize switching turn on loss as well as snubber capacitor loss.

$$C \le 0.5. L. \left(\frac{I_L}{V}\right)^2 \tag{6}$$

Where C= snubber capacitor, V= capacitor voltage, L= Inductor and I_L = inductor average current.

The power loss in snubber capacitor is given in equation (7) [11]

$$P_{-}C_{SNU} = \frac{1}{2} \cdot C_{s} \cdot V_{DS}^{2} \cdot f_{sw}$$
 (7)

Where C_s is the snubber capacitor, V_{DS} is the maximum voltage across the switch and f_{sw} is the switching frequency

The snubber capacitor is optimized for minimum power loss across it and for minimum switching turn on loss to improve the efficiency. For this, series of MATLAB script are executed and results are tabulated in Table 3.

Table 3 Snubber capacitor selection in SDCM of operation

Mode of		$V_1=V_{DS}$	C_{SNU}	E_C _{SNU}	E_15nf	Ε_10μΗ	P_C _{SNU}	P_15nf
operation	Case*	(V)	(nF)	$[C_S.V_1^2]$	(Joule)	$[\frac{1}{2}.L.I_{L}^{2}]$	(W)	(W)
				(Joule)		(Joule)		
	1	249.90	18.01	0.0011	9.36e-4	0.0011	56.25	46.84
	2	249.83	32.04	0.002	9.36e-4	0.002	100	46.81
Buck	3	249.91	32.02	0.002	9.36e-4	0.002	100	46.84
	4	269.91	15.44	0.0011	0.0011	0.0011	56.25	54.64
	1	102.90	67.98	7.2e-4	1.58e-4	7.2e-4	36	7.94
	2	112.91	56.47	7.2e-4	1.91e-4	7.2e-4	36	9.56
Boost	3	130.02	75.70	0.0013	2.53e-4	0.0013	64	12.68
	4	79.84	112.94	7.20e-4	9.56e-5	7.2e-4	36	4.78
		249.79	72.11	0.0045	9.35e-4	0.0045	225	46.79
Bidirectio	1	250.05	31.98	0.0020	9.37e-4	0.0020	100	46.89
nal		249.82	72.09	0.0045	9.36e-4	0.0045	225	46.81
	2	250.07	31.98	0.0020	9.38e-4	0.0020	100	46.90
		259.80	66.67	0.0045	0.0010	0.0045	225	50.62
	3	260.05	29.57	0.0020	0.0010	0.0020	100	50.72

^{*} Test cases as in Table 1, for different values of V_H, V_L, R₁, R₂, and I*



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From equation (7) the power loss in snubber capacitor is directly proportional to snubber capacitor value, drain to source voltage of MOSFET and switching frequency, so it is better to select minimum value of snubber capacitor for maximum efficiency. From the Table 3 for SDCM of operation, it is observed that, the minimum snubber capacitor value for maximum capacitor voltage is 15.44 nF and the corresponding power loss across it is 56.25 Watts. To satisfy equation (5), for all different test cases in different modes of operation, a snubber capacitor of 15nF is considered in circuit topology module which ensures, the capacitor fully discharge before the switch is turn on, which minimizes the switch turn-on loss.

Mode of		$V_1=V_{DS}$	C_{SNU}	E_C _{SNU}	E_75nf	Ε_50μΗ	P_C _{SNU}	P 75nf
operation	Case*	(V)	(nF)	$[C_{S}.V_{1}^{2}]$	(Joule)	$[\frac{1}{2}. L. I_L^2]$	(W)	(W)
				(Joule)		(Joule)		` ′
	1	249.90	90.06	0.0056	0.0047	0.0056	281.25	234.20
	2	249.83	160.21	0.010	0.0047	0.01	500	234.07
Buck	3	249.91	160.10	0.010	0.0047	0.01	500	234.22
	4	269.91	77.20	0.0056	0.0055	0.0056	281.25	273.20
	1	102.90	339.94	0.0036	7.94e-4	0.0036	180	39.71
	2	112.91	282.35	0.0036	9.56e-4	0.0036	180	47.81
Boost	3	130.02	378.55	0.0064	0.0013	0.0064	320	63.40
	4	79.84	564.70	0.0036	4.78e-4	0.0036	180	23.90
D' 1'	1	249.79	360.6	0.0225	0.0047	0.0225	1.125e3	233.98
Bidirectio	1	250.05	159.93	0.010	0.0047	0.010	500	234.47
nal		249.82	360.49	0.0225	0.0047	0.0225	1.125e3	234.05
	2	250.07	159.91	0.010	0.0047	0.010	500	234.50
		259.80	333.35	0.0225	0.0051	0.0225	1125	253.11
	3	260.05	147.87	0.010	0.0051	0.010	500	253.60

Table 4 Snubber Capacitor selection in CCM of operation

From the Table 4 for CCM of operation, it is observed that, the minimum snubber capacitor value for maximum capacitor voltage is 77.20 nF and the corresponding power loss through it is 281.25 Watts. To satisfy equation (5), for all different test cases in different modes of operation, a snubber capacitor of 75nF is considered in circuit topology module which ensures, the capacitor fully discharge before the switch is turn on, which minimizes the switch turn-on loss.

V. EFFICIENCY CALCULATION

Majority of losses in DC-DC switching power converter is from device conduction (MOSFET and diode), switching (MOSFET), inductor and from snubber capacitor. The switch conduction loss and diode conduction loss are given in equations (8) and (9) respectively [6]

$$P_{sw_con} = I_{sw} (0.75 + 0.003I_{sw})$$
 (8)

$$P_{d_con} = I_d (1 + 0.0016I_d)$$
(9)

Where I_{sw} and I_d are total switch rms current and total diode rms current respectively.

Switching loss in converters occurs during switching transitions and is due to the nonzero product of the switch drain-to-source current and drain-to-source voltage and it is given in equation (10)[12]. There is another switching loss due to discharging of drain to source capacitor of the MOSFET during turn on; this is given in equation (11) [12].

$$P_{sw1} = \frac{1}{2} \cdot V_{off} \cdot I_{on} \cdot f_{sw} (T_{on} + T_{off})$$
 (10)

Where V_{off} is the drain to source voltage when the MOSFET is off, I_{on} is the drain current when the MOSFET is on and f_{sw} is the switching frequency. The MOSFET on and off times, T_{on} and T_{off} are obtained from data sheets.

$$P_{sw2} = \frac{1}{2} \cdot C_{ds} \cdot V_{off}^2 \cdot f_{sw}$$
 (11)

^{*} Test cases as in Table 1, for different values of V_H, V_L, R₁, R₂, and I*



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Where C_{ds} is the drain to source capacitor of the MOSFET, its value is obtained from datasheet.

The efficiency is calculated by equation (12)

$$\eta = \left[\frac{P_0}{P_0 + P_{sw_con} + P_{d_con} + P_{sw1} + P_{sw2} + P_L + P_C C_{SNU}} \right] X100\%$$
 (12)

Where $P_o = I_o.V_o$, is the output power. I_o and V_o are the output current and output voltage respectively. P_L and P_C_{SNU} are inductor and snubber capacitor loss given in equation (3) and (7) respectively.

VI. EFFICIENCY COMPARISON IN SDCM AND CCM OF OPERATION

Table 5 Efficiency in SDCM and CCM of operation in buck, boost and bidirectional mode.

Mode of	Case		SDCM, L	=10 μΗ			CCM, L	=50 μΗ		$oldsymbol{\eta}_{ ext{diff}}$
operation	*	I_{Peak}	I_{min}	ΔI_{L}	η	I_{Peak}	I_{min}	$\Delta ext{I}_{ ext{L}}$	η	(%)
		(A)	(A)	(A)	(%)	(A)	(A)	(A)	(%)	
	1	74.96	-44.96	59.96	95.08	26.99	3.00	11.99	89.16	5.92
Buck	2	59.89	-19.89	39.89	96.86	27.97	12.02	7.97	93.28	3.58
	3	79.98	-39.98	59.98	94.64	31.99	8.00	11.99	87.52	7.12
	4	81.64	-51.64	66.64	94.68	28.32	1.67	13.32	87.79	6.89
	1	13.70	-37.70	25.70	94.38	-6.85	-17.14	5.14	90.45	3.93
Boost	2	16.12	-40.12	28.12	95.21	-6.37	-17.62	5.62	91.03	4.18
	3	16.30	-48.30	32.30	94.64	-9.53	-22.46	6.46	90.76	3.88
	4	2.97	-26.97	14.97	96.93	-9.00	-14.99	2.99	94.11	2.82
Bidirectional	1	84.30	-24.30	54.30	96.75	40.86	19.13	10.86	97.36	0.61
Buck	2	91.54	-31.54	61.54	96.19	42.30	17.69	12.30	92.82	3.37
	3	88.76	-28.76	58.76	96.63	41.75	18.24	11.75	93.66	2.97
Bidirectional	1	30.40	-70.40	50.40	91.85	-9.91	-30.08	10.08	83.36	8.49
Boost	2	37.60	-77.60	57.60	93.57	-8.47	-31.52	11.52	86.56	7.01
	3	31.15	-71.15	51.15	91.51	-9.76	-30.23	10.23	82.42	9.09

^{*} Test cases as in Table 1, for different values of V_H, V_L, R₁, R₂, and I*

Table 5 shows the efficiency comparison among SDCM and CCM of operation for different test cases given in Table 1. From the obtained results, it is noticed that, efficiency in SDCM is more than in CCM of operation except in case 1 of bidirectional buck mode of operation. But inductor ripple current is more in SDCM of operation than in CCM of operation. Comparison of efficiency and inductor ripple current among SDCM and CCM of operation for buck, boost and bidirectional mode of operation is shown in Figures 2, 3 and 4 respectively.



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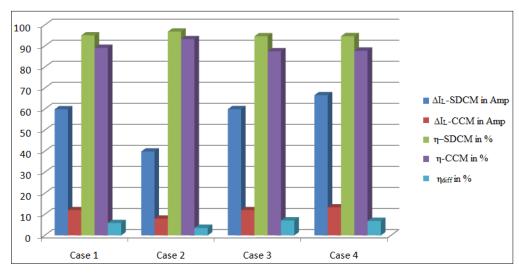


Fig. 2 Variation of inductor ripple current and efficiency in buck mode of operation

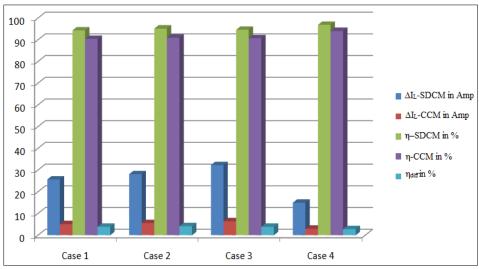
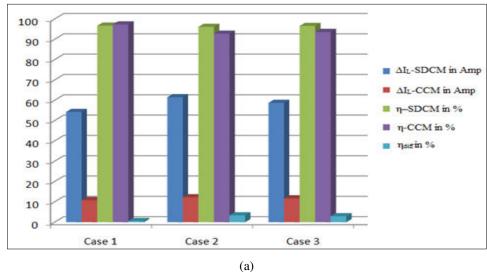


Fig. 3 Variation of inductor ripple current and efficiency in boost mode of operation





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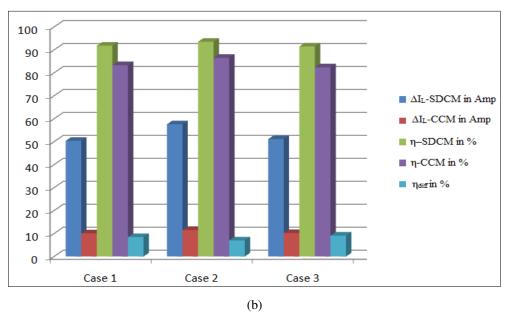


Fig.4 Variation of inductor ripple current and efficiency in bidirectional mode of operation

(a) Buck mode of operation (b) Boost mode of operation

VII. CONCLUSION

The paper presents a high-efficiency non-isolated bidirectional synchronous DC-DC switching power converter. The converter is made to operate in Synchronous Discontinuous Current Mode (SDCM) and Continuous Current Mode (CCM) of operation. A serial of MATLAB script are executed to find the snubber capacitor and inductor value for SDCM and CCM of operation. A complementary gate signal control scheme is used to turn on and off the transistor switch. Anti-paralleled diode of the transistor switch helps to discharge the capacitor. Efficiency in SDCM and CCM of operations for different test cases of buck, boost and bidirectional mode of operation is carried out. From the obtained result, it is observed that, the efficiency is more in SDCM of operation than in CCM of operation except in case one of bidirectional buck mode of operation. So, SDCM of operation is the best choice for maximum efficiency and to minimize the size, cost and weight of the converter.

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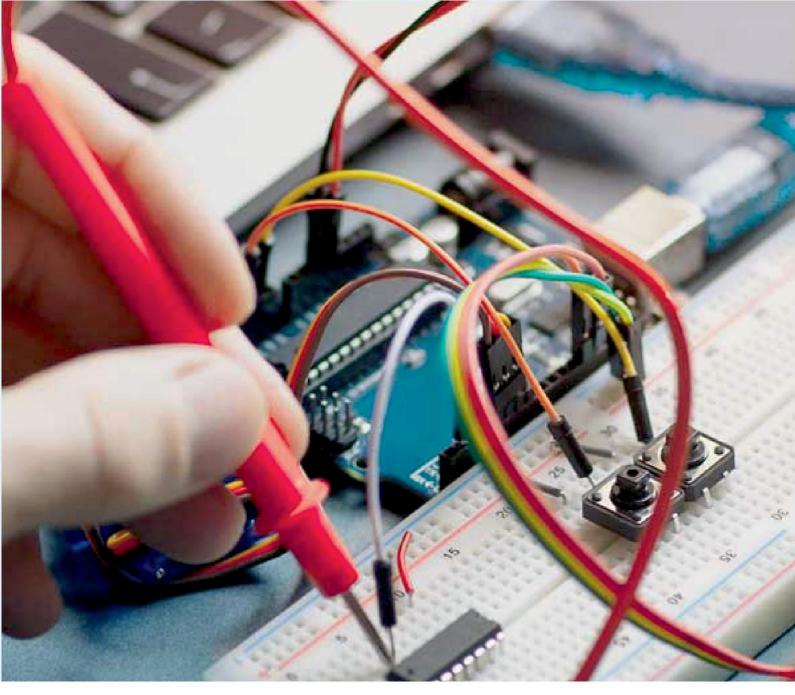
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