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Wallace Tree Multiplier with Koggestone Adder using 15-4 Compressor

B. Mani Harika[1], K.V. Durga Bhavani[2], K. Durga Tejaswini[3], R. B.V.N. L Vydehi[4], G.Vinutna Ujwala [5].

Student, Department of ECE, Pragati Engineering College, Suramplaem, East Godavari (Dt.), India[1234]

Assistant Professor, Department of ECE, Pragati Engineering College, Suramplaem, East Godavari (Dt.), India [5]

ABSTRACT: In the electronics world, multiplier plays a key role. Multipliers are necessary in many applications like basic fundamental blocks of digital systems, FIR filters, DSP, Image processing, Arithmetic operations. But, multipliers are the main reason for power dissipation and propagation delay. They occupy more space in chip designing. These drawbacks affect the performance of the multiplier. This paper focuses on a multiplier which yields highperformance of the circuit A 16-bit Wallace tree multiplier with koggestone adder using 15-4 compressor is designed to reduce propagation delay, power dissipation and area. This proposed multiplier is synthesized& simulated using Xilinx 14.7 ISE Design suite. Here, the performance of the proposed multiplier is compared with that using a ripple carry adder. The multiplier occupies about 6% of available LUT's. The dissipated power and delay are 0.005µw, 25.893 ns respectively.

KEYWORDS: Wallace tree multiplier, Koggestone adder, Compressor, Power dissipation, propagation delay.

I. INTRODUCTION

The important considerations in chip designing are power consumption, propagation delay and area. This proposed Wallace tree multiplier with koggestone adder using 15-4 compressor meets all the considerations in chip designing.Wallace tree multiplier comprises of 3 stages partial product generation, reduction and addition in final stage. The partial products reduction phase involves in more power consumption and area. To achieve these concerns, a 15-4 compressor technique is used in reduction stage. This 15-4 compressor internally consists of 5 full adders and two 5-3 compressors. Compressors are used to reduce and assemble large number inputs to smaller number of inputs laterally.

In the final stage of addition, the existing ripple carry adders involve propagation delay. To reduce propagation Delay koggestone adder is implemented. The comparision table, simulation results and brief descriptions of Wallace tree multiplier, 15-4 compressor and koggestone adder is done in further sections.

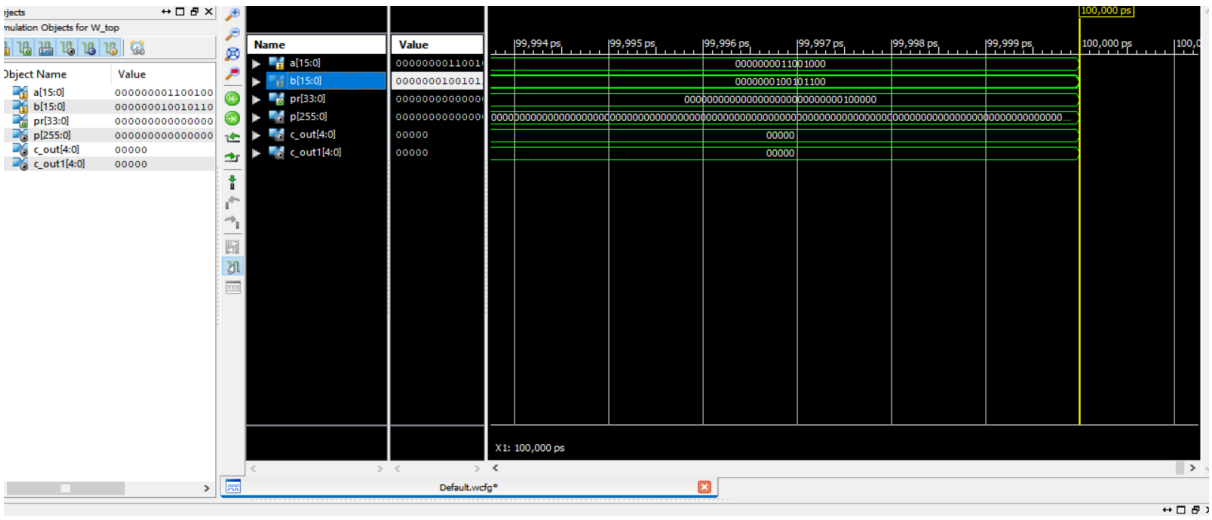

Fig. 1. Output of a 16 bitWallace tree multiplier with koggestone adder using 15-4 compressor Design.

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II. WALLACE TREE MULTIPLIER

A Wallace tree multiplier is a hardware implementation of digital circuit used to multiply two binary numbers. To multiply 16-bit and 32-bit numbers using conventional multipliers, the implementation becomes more complex than that in case of 4-bit and 8-bit numbers. To prevail over this complexity Wallace tree multiplier is used. It is well known for its reduction technique. Here, it involves 3 stages:

a. Partial Products generation.
b. Partial Products reduction.
c. Addition at the final stage.

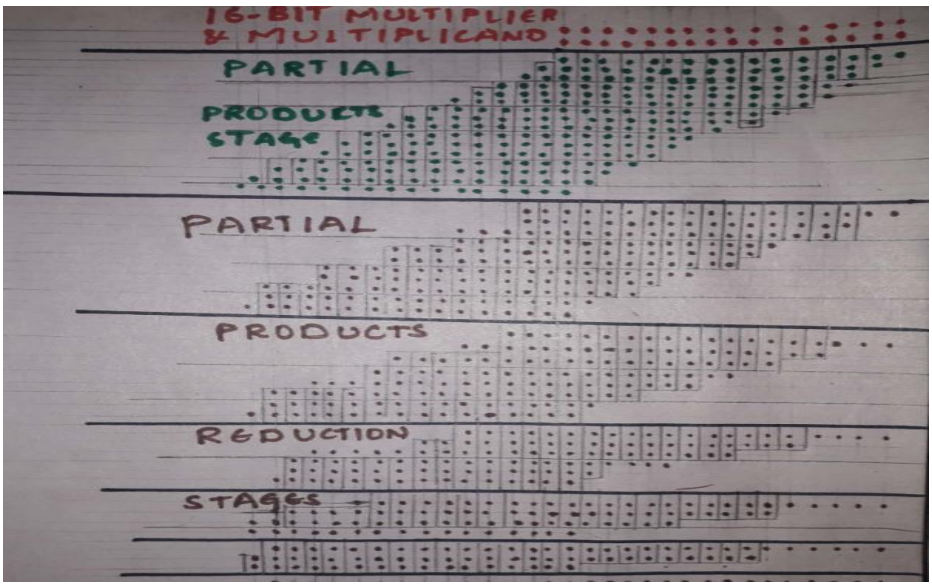

Fig. 1. Wallace tree multiplier.

Partial products are generated by multiplying 16-bit multiplicand and 16-bit multiplier. In the figure each symbol implies a partial product. The reduction technique contains 15-4 compressor, 5-3 compressor, half adders and full adders. Zero padding is done for 13^{th} and 14^{th} and column. For a particular column, depending on number of bits in that column appropriate adder is chosen. In case, of a single bit it is moved to the further levels. The reduction technique is cumulatively done until two rows remain. Finally, the addition of two rows is accomplished by 4-bit koggestone adder.

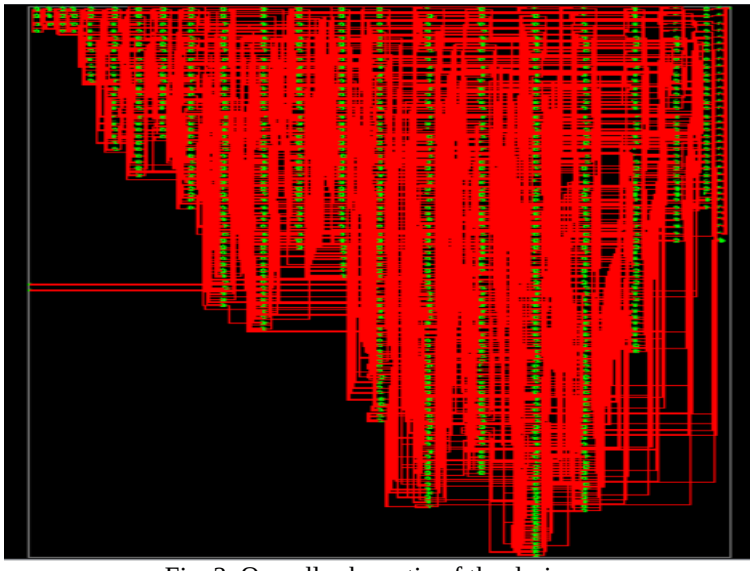

Fig. 2. Overall schematic of the design.

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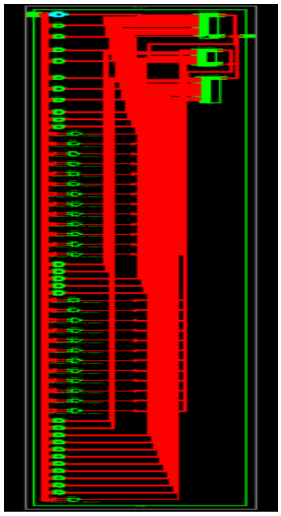

Fig.3. RTL schematic of the design.

III. COMPRESSOR

Here, the 15-4 compressor is accomplished to reduce the number of bits in partial products reduction stage and to reduce the operands in addition of partial products. It speeds the performance of the Wallace tree multiplier. Many DSP's, image processing techniques for their arithmetic operations utilize these compressors. Internally, it reduces the number of gates involved in the circuit. The internal structure of 15-4 compressor comprises of 5 full adders, two 5-3 compressors and a 4-bit koggestone adder.

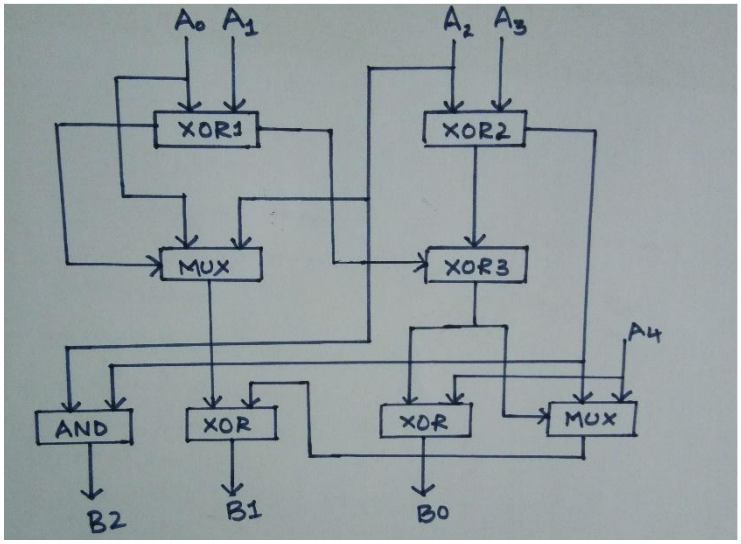

Fig. 4. 5-3 Compressor.

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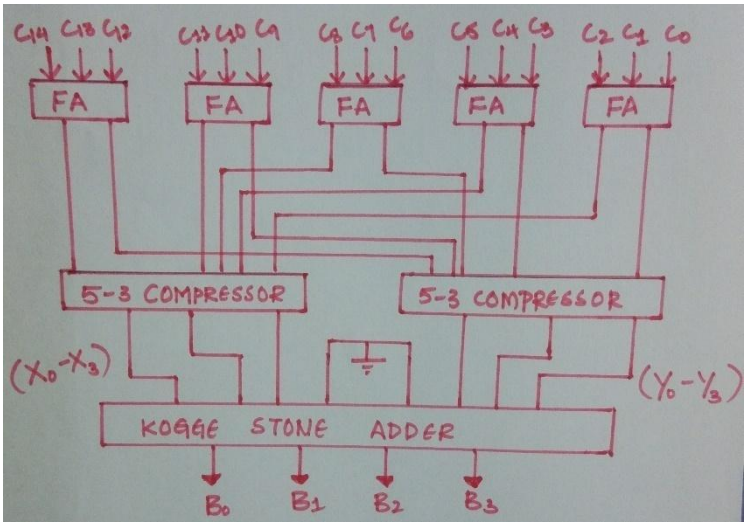

Fig. 5. 15-4 Compressor.

5-3 compressor is the fundamental unit of 15-4 compressor. By the name itself, the 5-3 compressor compresses.The 5-bit input to a 3-bit output. It is composed of XOR gates, AND gates, MUX's and employs counter property i.e., measures the active inputs (presence of logic '1').

IV. KOGGESTONE ADDER

In the conventional multipliers, the ripple carry adder propagates delay for the carry bit at each stage. The koggestone adder is implemented to boost up the performance of the Wallace tree multiplier by reducing propagation delay in addition stage. Koggestone is a parallel prefix form of carry look-a-head adder. Each vertical stage in koggestone adder produces 'Generate' and 'Propagate' signals. The computation is done in 3 stages:

I. Pre- processing.
II. Prefix.
III. Final computation.

Pre-Processing:

It produces, propagate (P_i) and generate (G_i) bits.

$P_i = A_i$ XOR B_i.
$G_i = A_i$ AND B_i.

Prefix:

- Black Cell: It takes two pairs of generate and propagate signals and produces a pair of generate and propagate signals as output.
  $G = G_i$ OR (P_i AND P_j).
  $P = P_i$ AND P_j.
- Grey Cell: It takes pair of propagate and generate signals and produces only generate signal.
  $G = G_i$ OR (P_i AND P_j).

Final Computation:

The sum and carry bits are generated as

$C_i = G_i$.
$S_i = P_i$ XOR C_{i-1}.

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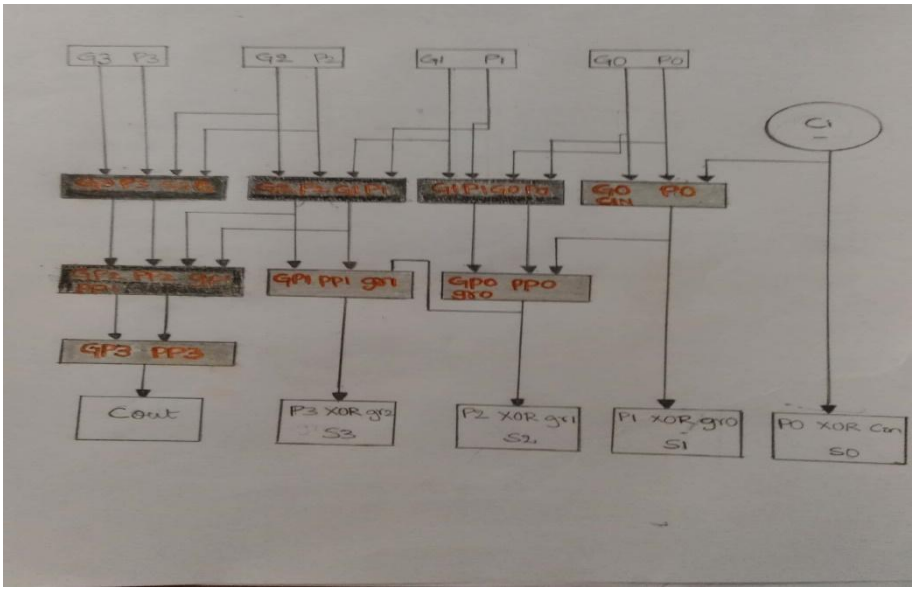

Fig. 6. Koggestone adder.

V. SIMULATION RESULT

Simulations of 16-bit Wallace tree multiplier with koggestone adder using 15-4 compressor is done in Verilog, using Xilinx 14.7 ISE. The power consumption, delay and area of the conventional and proposed designs are tabulated in table1. The simulation results and overall architecture of 16-bit Wallace tree multiplier with koggestone adder using 15-4 compressor are as follows.

A. Power analysis of 16-bit Wallace tree multiplier with koggestone adder using 15-4 compressor.

Fig. 7. Power report

B. Delay analysis of 16-bit Wallace tree multiplier with koggestone adder using 15-4 compressor.

```
MUXF5:S->O             1   0.401   0.388  w2/rr1/f4/carry46_SW0_f5 (N98)
LUT3:I2->O             1   0.147   0.514  w2/rr1/f4/carry46 (w2/rr1/c4)
LUT4:I1->O             1   0.147   0.388  w2/rr1/ff6/carry40 (w2/rr1/ff6/carry40)
LUT2:I1->O             2   0.147   0.567  w2/rr1/ff6/carry45 (w2/cq)
LUT4:I0->O             4   0.147   0.398  w2/hh1/x2/w1_and00001 (c_out1<4>)
LUT3:I2->O             3   0.147   0.565  w3/compe1/m2/y_and00001 (w3/compe1/m2/y_and00
LUT4:I0->O             4   0.147   0.564  w3/compe1/x5/y1 (w3/cq1)
LUT4:I0->O             1   0.147   0.000  w3/compk1/x3/y_and000012 (w3/compk1/x3/y_and0
MUXF5:I0->O            3   0.291   0.525  w3/compk1/x3/y_and00001_f5 (w3/compk1/x3/y_an
LUT4:I1->O             3   0.147   0.565  w3/compk1/x5/y1 (w3/t41)
LUT4:I0->O             3   0.147   0.525  w3/comp256/carry (w3/tc)
LUT3:I0->O             1   0.147   0.554  w3/rr5/f4/carry5 (w3/rr5/f4/carry5)
LUT4:I0->O             1   0.147   0.554  w3/rr5/f4/carry107_SW0 (N114)
LUT4:I0->O             2   0.147   0.527  w3/rr5/f4/carry107 (w3/rr5/c4)
LUT4:I1->O             1   0.147   0.266  w3/h2h7/x1/y1 (pr_29_OBUF)
OBUF:I->O                  3.255          pr_29_OBUF (pr<29>)
----------------------------------------
Total                     25.983ns (10.405ns logic, 15.578ns route)
                                   (40.0% logic, 60.0% route)

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Fig. 8. Time report

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C. Area analysis of 16-bit Wallace tree multiplier with koggestone adder using 15-4 compressor.

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Device utilization summary:
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Selected Device : 4vfx12sf363-12

 Number of Slices:                      415  out of   5472     7%
 Number of 4 input LUTs:                739  out of  10944     6%
 Number of IOs:                          66
 Number of bonded IOBs:                  66  out of    240    27%

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Partition Resource Summary:
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Fig. 9. Area report

Table 1Comparision Table

Parameters	Using parallel adder	Using Koggestone adder
Area	7% of available LUT's	6% of available LUT's
Delay	26.803 ns	25.983 ns
Power	0.218w	0.166w

Table 1 compares the proposed Wallace tree multiplier with koggestone adder using 15-4 compressor with that of a multiplier using Ripple carry adder.

VI. CONCLUSION

The improved version of Wallace tree multiplier with koggestone adder using 15-4 compressor is thus, can be considered faster, efficient than the multiplier with ripple carry adder. The synthesis and simulation reports of this design are achieved by using Virtex4 board in Xilinx ISE 14.7.

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