International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (IJAREEIE)

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

FPGA Implementation of 32 Bit Complex Floating Point Multiplier Using Vedic Real Multipliers with Minimum Path Delay

Vinayak Honnungar[1], Shweta Basarikatti[2], Smital Domble[3], Sonali Iroji[4], Priya Naik[5]

Assistant Professor, Dept. of ECE, S. G. Balekundri Institute of Technology, Belgavi, Karnataka, India[1]

UG Students, Dept. of ECE, S.G.Balekundri Institute of Technology, Belgavi, Karnataka, India[2,3,4,5]

ABSTRACT: "Vedic Mathematics" refers to technique of calculation based on a set of 16 Sutras, or aphorisms, as algorithms and their upa-sutras or corollaries derived from these Sutras. Its enthusiasts advance the claim that any mathematical problem can be solved mentally with these sutras.Based on the Indian Vedic mathematics sutra called URDHVA TIRYAKBHYAM, two architectures for 24 x24 bit Vedic real multiplier are proposed.The four floating point real multipliers solution for the proposed multiplier is coded in Verilog for implementation on FPGA. Finally, the results of the proposed multiplier are compared with that of the Booth and Array multipliers.

KEYWORDS: Vedic Mathematics, Urdhva-triyakbhyam sutra, Vedic real multiplier, complex floating Point multiplier, FPGA.

I.INTRODUCTION

Vedic Mathematics is the name given to the ancient system of Indian Mathematics which was rediscovered from the Vedas between 1911 and 1918 by Sri BharatiKrsnaTirthaji (1884-1960). 'Vertically and Crosswise' is one of these Sutras. These formulae describe the way the mind naturally works and are therefore a great help in directing the student to the appropriate method of solution.Vedic Mathematics can definitely solve mathematical numerical calculations in faster way. Some Vedic Math Scholars mentioned that Using Vedic Maths tricks you can do calculations 10-15 times faster than our usual methods. I agree this to some extent because some methods in Vedic Mathematics are really very fast. But some of this methods are dependent on the specific numbers which are to be calculated. They are called specific methods. As such, complex multipliers in large number are required to implement the hardware modules. A Vedic multiplier (VM) faster than the array multiplier has been designed.Vedic Mathematics is the ancient methodology of Indian mathematics which has a unique technique of calculations based on 16 Sutras (Formulae). two possible architectures are proposed for a Vedic real multiplier based on the UT (Vertically and cross wise) sutra of Indian Vedic mathematics and an expression for path delay of an N×N Vedic real multiplier with minimum path delay architecture is developed. In an array multiplier multiplication of two binary numbers can be obtained with one micro-operation by using a combinational circuit that forms the product bits all at once thus making it a fast way of multiplying two numbers since the only delay is the time for the signals to propagate through the gates that form the multiplication array.

II.OBJECTIVES

1. Main goal of this paper is to reduce the delay and achieve the better area interms of slices.
2. The architecture should be simple as well as time efficient.
3. To enhance the multiplier speed.
4. To implement the project in less cost.

III. METHODOLOGY

The architectures of Vedic real multipliers using Urdhva-Tiryakbhyam sutra. The meaning of this sutra is "Vertically and crosswise" and it is applicable to all the multiplication operations. It is an efficient multiplication technique when the multiplier and multiplicand lengths are small, but for the larger length multiplication this technique is not suitable because a large amount of carry propagation delays are involved in these cases.The 2 x 2 bit vedic multiplier can be implemented using two half adders and four two input AND gates.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

4 x 4 bit Vedic Multiplier: This architecture uses four 2X2 bit VMs and three 4 bit Ripple Carry Adders((RCAs).Thus, by using Urdhva Tiryakbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier

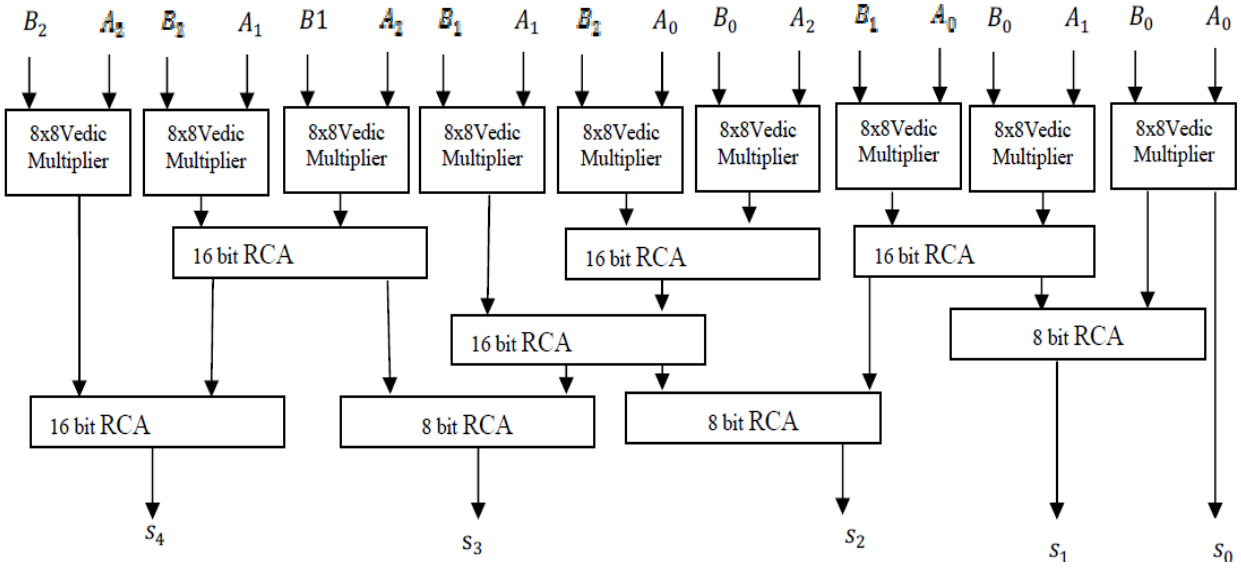


Fig. 1: Architecture of the 24 x 24 bit Vedic Multiplier using 8X8 bit Vedic multipliers.

24X24 BIT VEDIC MULTIPLIER BASED ON 8X8 BIT VEDIC MULTIPLIERS

The 24x24 bit VM architecture is shown in Fig.1.These sutras are used for the multiplication of two numbers in decimal system.The multiplier is based on UrdhavaTriyakbhayam Sutra. In this concept the generation of partial product can be done and then parallel addition of these partial product is done .

Path Delay Analysis :The proposed 24 x24 bit VM (Fig.1) requires nine 8 x 8 bit VMs and five 16 bit and three 8 bit adders. Hence, the 24x24 bit VM path delay can be expressed as

$Pd_{24vm}=pd_{8vm}+3d_{16fa}$ (1)

As one FA requires two HAs and an OR gate, Eq.(1) becomes

$Pd_{24vm}=d_{and}+161d_{ha}+72d_{or}$ (2)

CONVENTIONAL METHOD OF MULTIPLICATION

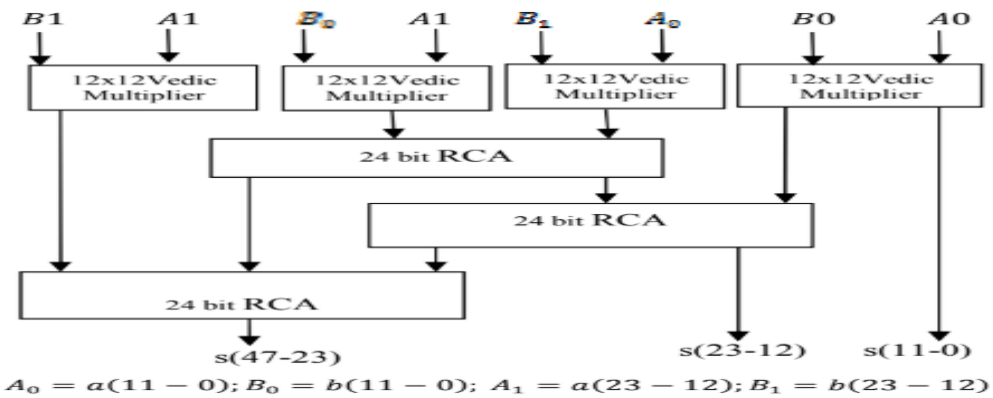


Fig. 2:Architecture of the conventional 24 x 24 bit Vedic Multiplier using 12X12 Vedic multipliers

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

Four 12x12 bit VMs and three 24 bit RCAs are required for the architecture of 24 x 24 bit VM shown in Figure 6. Therefore, the path delay of 24x 24 bit VM is given by,

$pd_{24vm}=pd_{12vm}+3d_{24ha}$ (3)

Since 24 bit adder requires one HA and 23 FAs and using above equation we can rewrite as

$pd_{24vm}=d_{and+}251d_{ha}+120d_{or}$ (4)

It can be observed from Eq.(2) that the delay is more ascompared to the path delay expressed by Eq.(4).Thus, theproposed architecture of vedic multiplication(Fig. 1) isfaster than the architecture given in Fig. 2.

IV. LITERATURE REVIEW

1. FPGA Implementation of Complex Multiplier Using Minimum Delay Vedic Real Multiplier by ArchitectureK.DeerghaRao,Ch. Gangadhar 2016

Proposed two possible architectures of a Vedic real multiplier designed by a Vedic mathematic UrdhvaTiryakbhyam sutra. Based on the path delay analysis of the two architectures, an expression for path delay of an NxN Vedic real multiplier with minimum path delay architecture is developed. Next, we implemented a complex multiplier using three and four real Vedic multipliers solutions. Further, we compared implementation results of the proposed complex Vedic multiplier with that of the four and three real multiplier solutions using the array, and Booth multipliers. The Vedic multiplication is based on an algorithm called Urdhva-Tiryakbhyam(vertical and crosswise) of ancient Indian Vedic mathematics.

2. High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics by PrabirSaha,Arindam Banerjee,Partha Bhattacharyya 14-16 january 2011

In algorithmic and structural levels, a lot of multiplication techniques had been developed to enhance the efficiency of the multiplier; which encounters the reduction of the partial products and/or the methods for their partial products addition, but the principle behind multiplication was same in all cases. Vedic Mathematics is the ancient system of Indian mathematics which has a unique technique of calculations based on 16 Sutras (Formulae). "Urdhva-tiryakbyham" is a Sanskrit word means vertically and crosswise formula is used for smaller number multiplication.

3. Multiplier design based on ancient Indian Vedic Mathematics by Honey DurgaTiwari, GanzorigGankhuyag, Chan Mo Kim, Yong Beom Cho,2008

In an array multiplier multiplication of two binary numbers can be obtained with one micro-operation by using a combinational circuit that forms the product bits all at once thus making it a fast way of multiplying two numbers since the only delay is the time for the signals to propagate through the gates that form the multiplication array. Another improvement in themultiplier is by reducing the numbers of partial products generated. The Booth recording multiplier is one such multiplier; it scans the three bits at a time to reduce the number of partial products. The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sums by examining three bits at a time. The high performance of Booth multiplier comes with the drawback of power consumption. The reason for this is the large number of adder cells (15 cells for 8 rows-120 core cells) that consume power.The conclusion is that the current methodology of multiplication leads to more consumption of power and reduction in efficiency.

4. Efficient FPGA Implementation of Complex Multipliers using the Logarithmic Number System by M.Y.Kong,2008

In many real-time DSP applications, high performance is a prime target. However, achieving this may be done at the expense of area, power dissipation and accuracy. Attempts have been made to use alternative number systems to optimize the realization of arithmetic blocks, maintaining high performance without incurring prohibitive area and power increases. This paper presents the FPGA implementation of complex multipliers based on the logarithmic number system. Synthesis results show that a design with a 10-stage pipeline can achieve a maximum clock rate of 224 MHz and 140 MHz for 16-bit and 32-bit designs, respectively. Both designs use the lowest amount of hardware in terms of gate equivalents as compared to a complex multiplier built with regular FPGA features. The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sumsby examining three bits at a time. The high performance of Booth multiplier comes with the drawback of power consumption.

V. ADVANTAGES

- Increases speed and accuracy.
- Improved academic performance and instant results.
- Sharpens your mind, increases mental agility and intelligence.
- Increase visualization and concentration in children.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

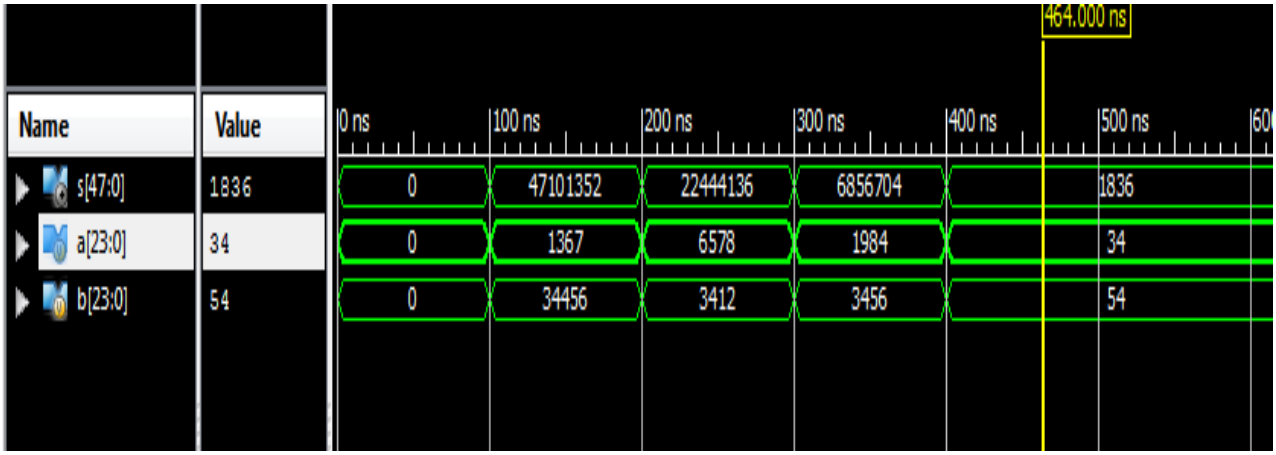
- Become a mental calculator.
- When compared to conventional method, it enables faster calculations. Thus, a lot of time gets saved.
- Acts as a tool for reducing finger counting and written work.

VI. RESULT

The proposed 24x24 bit Vedic multiplier using nine 8x8 Vedic multipliers solution is coded in Verilog and implemented on FPGA

Type of vedic multiplier	24X24 bit vedic multiplier	24X24 bit using conventional
Area consumed	1300 LUTs	1345 LUTs
Delay(ns)	21.77ns	39.916ns

It is inferred from the results that the proposed complex floating point Vedic multiplier is much faster as compared to the array, and Booth complex multipliers with little increase in total power



VII. CONCLUSION AND FUTURESCOPE

Vedic multiplier is faster than array and booth multiplier. Vedic multiplier has the greatest advantage as compared to other multipliers over gate delays and regularity of structures. As the number of bits increased from 8x8 to 24x24 bits the timing delay is greatly reduced for vedic multiplier as compared to other multipliers. The path delay analysis of the new architecture is performed in comparison with the conventional 24 x 24 real Vedic multiplier and has been shown that the new architecture has less path delay than the conventional architecture.

Further, four 32 bit floating point real Vedic multipliers solution for the 32 bit complex floating point Vedic multiplier can be coded in Verilog and execute on a FPGA device.

It is concluded from the results that the proposed Vedic multiplier is much faster(more than twice) as compared to Booth and array multipliers but with little increase in power consumption.

REFERENCES

[1] K.Hwang, Computer Arithmetic: Principles, Architecture and Design. New York: John Wiley & Sons, 1979.
[2] M.Y. Kong., J. P Langlois, and D. Al-Khalili,, "Efficient FPGA implementation of complex multipliers using the logarithmic number system," Proc. IEEE ISCAS, pp. 3154-3157, May, 2008.
[3] H.D.Tiwari, G.Gankhuyag, C.M. Kim,, and Y.B.Cho,"Multiplier design based on ancient Indian Vedic Mathematics,"Proc. IEEE ISOCC'08, Vol.2, pp.65-68, 2008..

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 6, June 2020 ||

[4] P.Saha, A. Banerjee, P.Bhattacharyya, and A.Dandapat, "High speed ASIC design of complex multiplier using vedic mathematics,"Proc. IEEE Students' Technology Symposium (TechSym), pp.237-241, Jan 2011.
[5] K. DeerghaRao, Ch. Gangadhar and P. K. Korrai, "FPGA implementation of complex multiplier using minimum delay Vedic real multiplier architecture," Proc. IEEE UPCON 2016
[6] Jagadguru Swami Sri Bharath, KrsnaTirathji, "Vedic Mathematics or Sixteen Simple Sutras From The Vedas", MotilalBanarsidas, Varanasi (India),1986.
[7] A.P. Nicholas, K.R Williams, J. Pickles, "Application of Urdhava Sutra", Spiritual Study Group, Roorkee (India),1984
[8] Xilinx LogiCore IP Complex Multiplier v3.1.