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Modelling and Simulation of Flying Capacitor Multilevel Inverter with Tapped Reactor

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ABSTRACT: In the last few years, vehicle manufacturers have been faced with the problem of developing a solution to the growing energy crisis and environmental issues.Therefore, electric vehicles, hybrid electric vehicles, and fuel cell vehicles are studied all over the world. Existing vehicle inverters operate at low voltage and are limited to low power. These vehicles operate at higher DC bus voltage and have higher power capacity. If the conventional inverters are used in Electrified vehicles, there is limitation of voltage rating of switches and switching frequency. Multilevel converters offer high power capability, associated with lower output harmonics and lower commutation losses. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. Several topologies for multilevel inverters have been proposed over the years. This work reports a flying capacitor multilevel inverter topology using a tapped reactor. The simplified multi-level inverter requires only eight switches for nine-level output. The studied multi-level inverter topology offers strong advantages such as improved output waveforms, smaller filter size, and lower electromagnetic interference and total harmonic distortion. The results are obtained through MATLAB/Simulink software package.

KEYWORDS: Multilevel Inverter, Tapped Reactor, Total harmonic distortion

I.INTRODUCTION

In the Recent years electric vehicles (EVs), hybrid Electric vehicles (HEVs) are studied all over the world due to several advantages like increased fuel efficiency, lower emissions and better vehicle performance. These vehicles that have large electric drives require advanced power electronic inverters to meet the high-power demands. One of the limitations in these studies when the switching devices are operated at high voltage, switching frequency is restricted. The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonics applications. Multilevel inverters overcome this problem because their individual devices have a much lower voltage per switching and they operate at high efficiencies because they can switch at a much lower frequency than PWM-controlled inverters. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. For this reason, multilevel inverters can easily provide the high power required of a large electric drive. The inverter can be used in hybrid electric vehicles and electric vehicles. Several multilevel inverter topologies have been developed like flying capacitor, neutral point clamped, Cascaded H-bridge (CHB) inverters.Among these topologies, and the cascaded H-bridge inverter has received much attention.

To increase the output voltage levels, the number of H bridges must be connected in cascade hence greater number of power semiconductor switches is required. Each switch requires a related gate drive and protection circuits. This may cause the overall system to be more expensive and complex. This paper suggests a new flying capacitor topology for multilevel inverter with a high number of steps associated with a low number of gate driver and protection circuits for switches. Reduction of rating of the switches is another advantage. The harmonic content is also reduced. A desired high output voltage is synthesized from several levels of dc voltages that can be batteries, capacitors, fuel cells etc.

II.PROPOSED MULTILEVEL INVERTER

The proposed multilevel inverter with tapped reactor is shown in fig1. It consists of an H-bridge configuration made from three-level flying capacitor branches. Essentially, it is a voltage-source inverter (VSI) with capacitive energy storage shared by all three phases. Total of eight switching devices are used in each phase. A tapped reactor is used to connect the two legs of the H-bridge. Typically, the reactor is wound to be centre tapped, making the output line-to-ground voltages (vag for example) the average of the voltages from each side of the H-bridge. Then, the line-to-ground voltages will have five distinct voltage levels. However, with this topology, the tap is set at 1/3. This results in seven distinct output voltages, and therefore, improves the power quality. The switching operation is described next, where seven levels are clearly illustrated.

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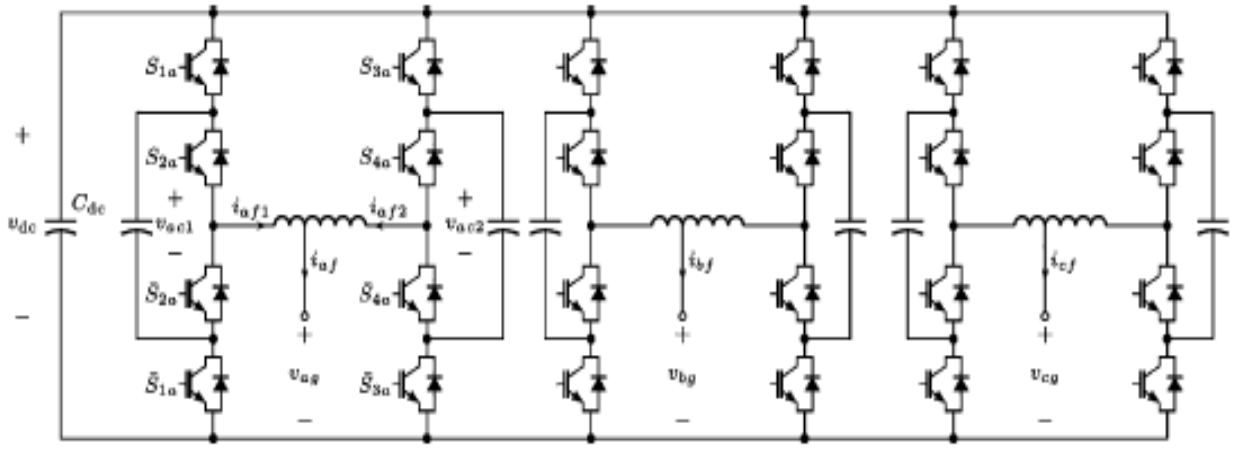

Fig. 1 Flying Capacitor Multilevel inverter with Tapped Reactor

III.TAPPED REACTOR MODEL

Unlike the centre-tapped inter phase reactor, the reactor in the proposed topology has a tap terminal at its one-third position, as shown in fig2. For the convenience of analysis, the reactor can be divided into two parts. In fig 2. part one, denoted as $L1$, consists of the portion from terminal $x1$ to the tap and has a number of turns $N1 = N$; part two, denoted as $L2$ consists of the portion from the tap to terminal $x2$ and has a number of turns $N2 = 2N$. Terminals $x1$ and $x2$ are defined as the input terminals while the tap terminal is defined as the output terminal x. To derive the relationship between the input voltages and the output voltage, an ideal model of the tapped reactor is considered first in which there are no losses and no leakage flux. The following assumptions are made.

1) The core of the reactor is highly permeable such that it requires small magneto motive force to set up the flux.
2) The core does not exhibit any eddy current or hysteresis loss.
3) All the flux is confined in the core, so there is no leakage.
4) The resistance of the reactor is negligible.

Suppose that voltages $vx1$ and $vx2$, with respect to a common ground, are applied to the input terminals $x1$ and $x2$, respectively. For this ideal model, it is straightforward to determine the voltage between the output terminal x and terminal $x2$

$$v_{xx2} = \left(\frac{N_2}{N_1 + N_2}\right)(v_{x1} - v_{x2}) = \frac{2}{3}(v_{x1} - v_{x2}).$$

The voltage at the output terminal with respect to the common ground is therefore

$$v_{xg} = v_{xx2} + v_{x2} = \frac{2}{3}v_{x1} + \frac{1}{3}v_{x2}.$$

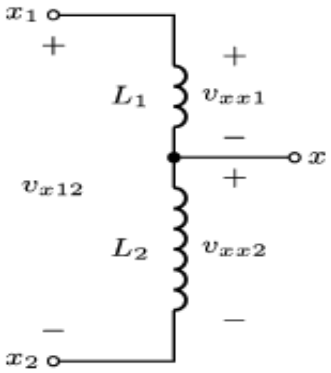

Fig. 2 Tapped Reactor Model

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IV.VOLTAGE LEVELS DETERMINATION

In the general analysis presented earlier, *x* represents a phase, and the phase may be *a*, *b*, or *c*. Each leg of the H-bridge has a voltage-clamping capacitor, and the voltages at the two input terminals of the reactor can be 0, *v*dc/2, or *v*dc, where *v*dc is the nominal voltage of the capacitor *C*dc, as shown in fig3. For each phase, there are nine different switching states, corresponding to nine terminal voltage combinations. These combinations can produce a line-to-ground voltage at the output terminal that has seven distinct voltage levels. For phase *a*, these states are detailed intable 1, *Sa* is the switching state that is defined as being 0 for the lowest possible line-to-ground voltage

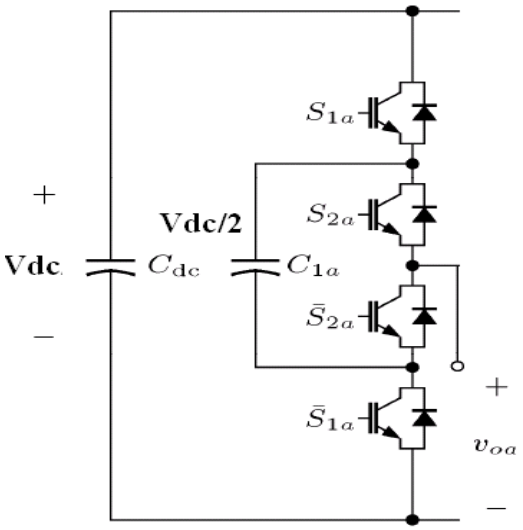

Fig. 3 Operation of one leg in phase 'a'

Table. 1 Seven level output

Vx1	Vx2	Vxg
0	0	0
0	Vdc/2	Vdc/6
Vdc/2	0	Vdc/3
Vdc/2	Vdc/2	Vdc/2
Vdc/2	Vdc	2Vdc/3
Vdc	Vdc/2	5Vdc/6
Vdc	Vdc	Vdc

V. NEW PROPOSAL

Unlike the centre-tapped interphase reactor, the reactor in the proposed topology has a tap terminal at its K position, as shown in fig 2. For the convenience of analysis, the reactor can be divided into two parts. In fig 2, part one, denoted as *L*1, consists of the portion from terminal *x*1 to the tap and has a number of turns *N*1 = *N*; part two, denoted as *L*2 , consists of the portion from the tap to terminal *x*2 and has a number of turns *N*2 = K*N*. Terminals *x*1 and *x*2 are defined as the input terminals while the tap terminal is defined as the output terminal *x*.
The voltage at the output terminal with respect to the common ground is

$$Vxg=KVx1+(1-K)\ Vx2$$

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Where K is tapping position of Inductor.
For K=1/4, Vxg= 1/4Vx1+3/4Vx2
The switching sequence and output voltage levels are shown in Table 2.

Table 2 Nine level output

Vx1	Vx2	Vxg
0	0	0
0	Vdc/2	Vdc/8
Vdc	0	2Vdc/8
Vdc/2	0	3Vdc/8
Vdc/2	Vdc/2	4Vdc/8
Vdc/2	Vdc	5Vdc/8
Vdc	0	6Vdc/8
Vdc	Vdc/2	7Vdc/8
Vdc	Vdc	Vdc

By connecting these two voltages with tapped inductor we can get more voltage levels in the output here we are getting 9 levels.

VI.SIMULATION RESULTS

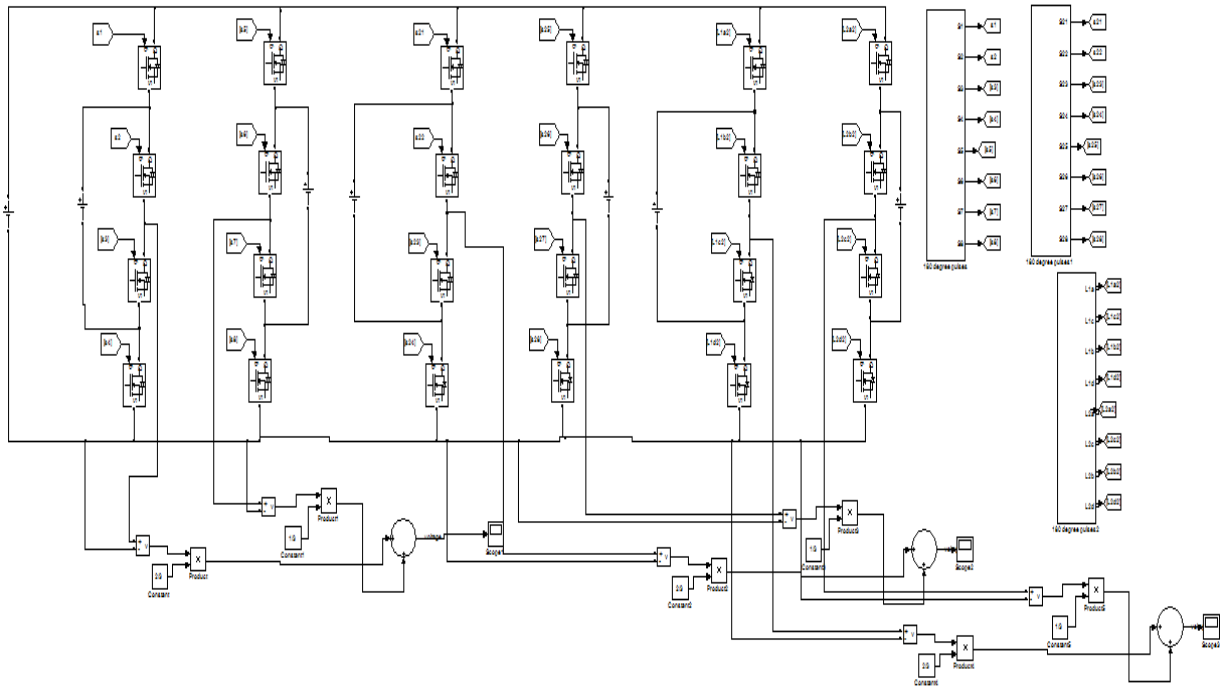

Fig 4 The Matlab/Simulink model of three phase seven level inverter

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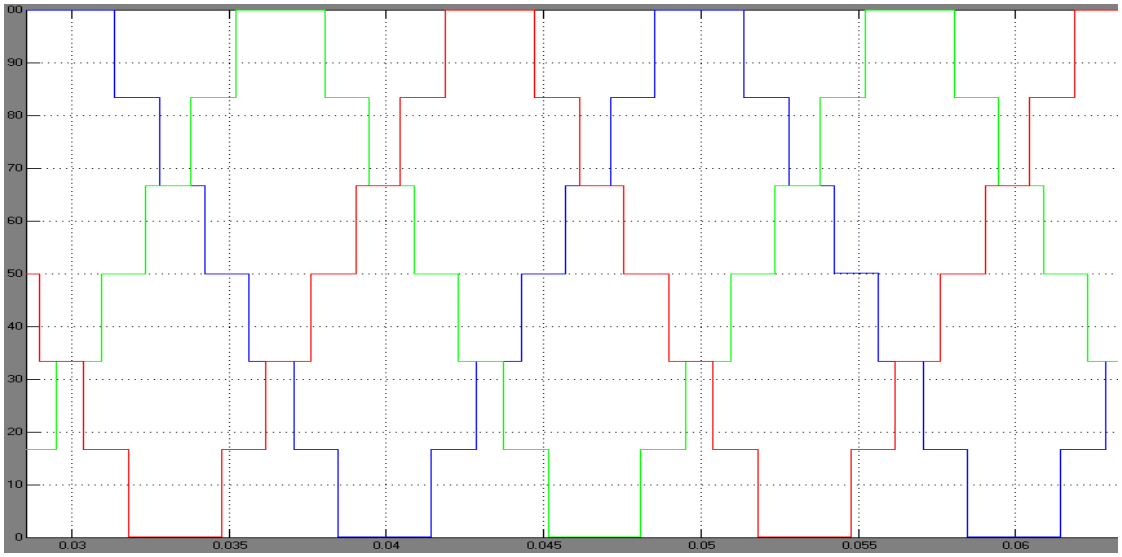

Fig 5 Three Phase seven level output

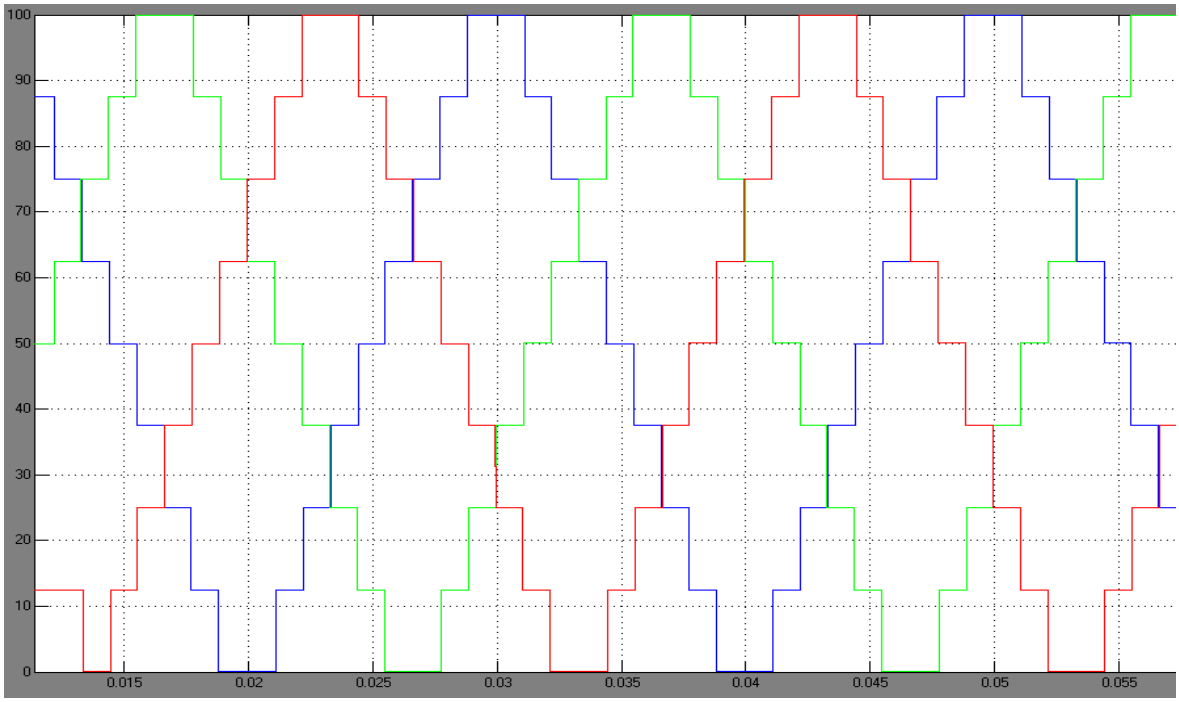

Fig 6 Three Phase nine level output

VII.CONCLUSION

Fig. 5 shows the three phase seven level output waveform. Here each voltage step is Vdc/6. So, the dv/dt rating is reduced by six times compared to conventional two-level inverter. Here total harmonic distortion is 16.77%.Fig. 6 shows the three phase nine level output waveform. Here each voltage step is Vdc/8. So, the dv/dt rating is reduced by eight times compared to conventional two-level inverter. Here total harmonic distortion is 14.82%. Finally, a new configuration of flying capacitor multilevel inverter with tapped reactor has been proposed. The proposed topology needs a smaller number of switching devices with minimum standing voltage. THD is also reduced. The simulation results are shown which are accorded with the theoretical results. The proposed inverter is used in high power applications like EV and HEV drives.

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