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VLSI Based Energy-Efficient 32-Bit Multiplier Architecture

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ABSTRACT: A fast and energy-efficient multiplier is always needed in electronics industry especially DSP, image processing and arithmetic units in microprocessors. Multiplier is such an important element which contributes substantially to the total power consumption of the system. On VLSI level, the area also becomes quite important as more area means more system cost. Speed is another key parameter while designing a multiplier for a specific application. These three parameters i.e. power, area and speed are always traded off. Speaking of DSP processors, area and speed of MAC unit are the most important factors. But sometimes, increasing speed also increases the power consumption, so there is an upper bound of speed for a given power criteria. Considering the battery operated portable multimedia devices, low power and fast designs of multipliers are more important than area.

KEYWORDS: Digital Signal Processing(DSP),Fast Fourier Transform(FFT),Multiply And Accmulate(MAC)

I.INTRODUCTION

The most important fundamental function in arithmetic operations is multiplication. Some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) are Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product[1]. These are presently used in many Digital Signal Processing (DSP) applications such as Fast Fourier Transform(FFT), convolution, filtering and in microprocessors in its arithmetic and logic unit. There is a need of high speed multiplier since multiplication dominates the execution time of most DSP algorithms[9]. At present the instruction cycle time of a DSP chip determination depends on multiplication time and this time is still a dominant factor.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications[11]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades[12]. Reducing the time delay and power consumption are very essential requirements for many applications. This work presents different multiplier architectures[2]. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design[10]. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application.

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II. DLSB IMPLEMENTATION

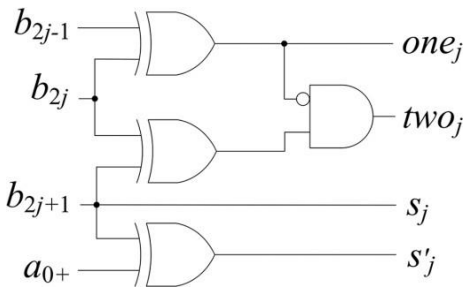

Fig.1.Proposed DLSB Modified Booth encoder

There are two kinds of multipliers i.e. unsigned and signed. In unsigned multiplier, it is assumed that both the multiplier and the multiplicand are positive integers, while in signed multipliers, the operands bear signs which is represented by the MSB of each operand[3]. A signed multiplier is a little bit more complex than an unsigned one due to the possibility that any number can be negative changing the result[4]. The sign bit creates some troubles while compressing the partial products. The sign bit of a partial product row has to be extended all the way to the MSB position which would require the sign bit to drive that many output loads. This makes the partial product rows unequal in length [3].

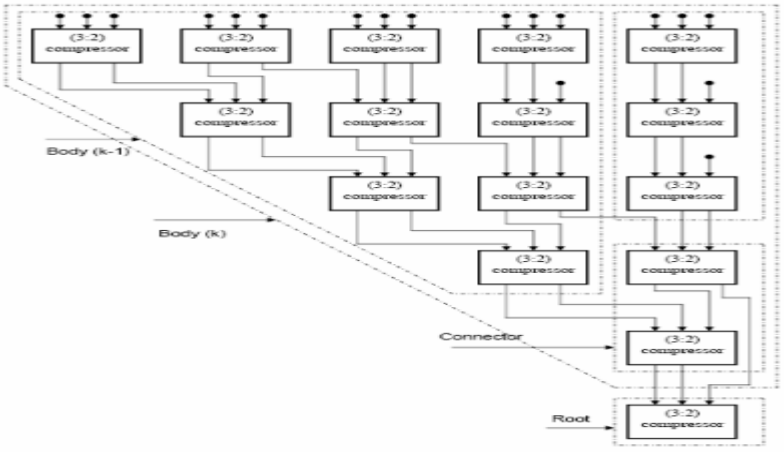

Fig.2.Overturned-staircase tree with 18 PPs

III.PROPOSED ARCHITECTURE

The Overturned-Staircase (OS) tree is a regular structure and is designed recursively. It achieves the same number of compressor levels as Wallace for many values of the PPs[5][6]. This tree is constructed from a root and the body. The root is the last [3:2] compressor. The body is a recursive concatenation of compressors. A body of height k, where k is the maximum number of [3:2] counters in series, is constructed from a body of height k-1 and a branch of serially connected [3:2] compressors[7]. The smaller body and the branch are connected using a connector. The connector is made of two [3:2] compressors, each of which takes five inputs and produces three outputs [2]. By this way, OS tree of type 1 is constructed. An OS2 tree is built by replacing each branch in the tree with an OS1 tree that has the same

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delay[8]. This method can be further extended to build even higher-order OS trees by replacing the branches in the OS2 tree with OS1 trees. An example of OS tree reducing 18 PPs.

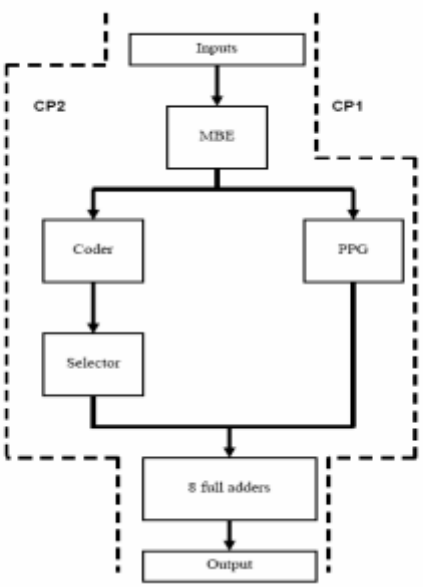

Fig.3.Critical path of new architecture

IV.SIMULATION RESULTS

Power, performance comparison The two multiplier architectures have been simulated using the circuit simulator Spectre and process data from a commercially available 130-nm CMOS technology. A Common test bench has been set up, where the power and performance have been evaluated. Figure 5 shows the power-delay plot of the simulation results.

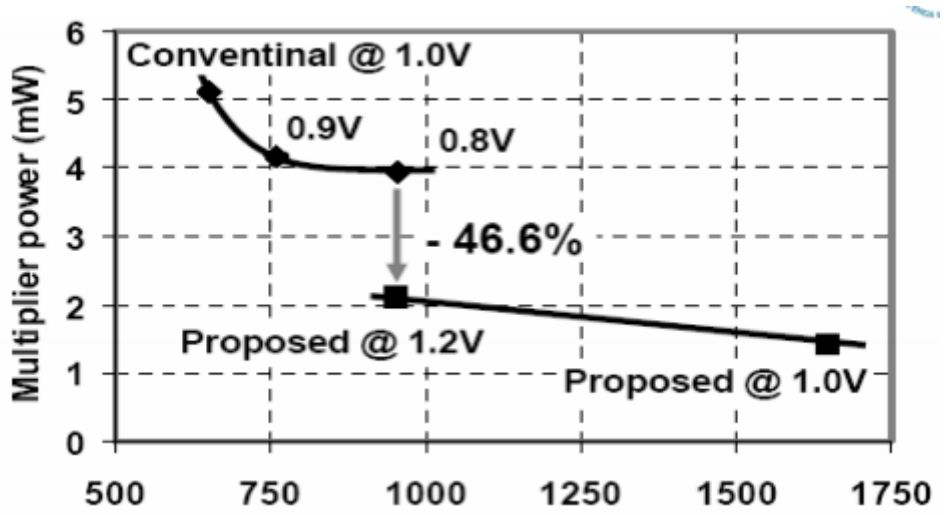

Fig.4.Power Vs Delay Report.

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The conventional multiplier has a delay of 652 ps with 5.11mW power dissipation at nominal power supply (1.0 V). The proposed structure with its more complex PPG resulted in 1648ps delay and 1.41mW power dissipation at nominal supply. Calculating the power delay-product (PDP) for the two architectures at nominal supply gives 3.33pJ and 2.32pJ for the conventional and proposed, respectively. In order to get a fair power comparison of the two multiplier architectures, the power supply of the conventional structure was reduced, while the same for the proposed multiplier was increased until equal latency was achieved. For the same delay, the PDP point of the conventional multiplier was 3.78pJ compared to 2.01pJ for the proposed architecture. Hence, the proposed architecture enables 47 % better energy-efficiency for equal throughput and latency.

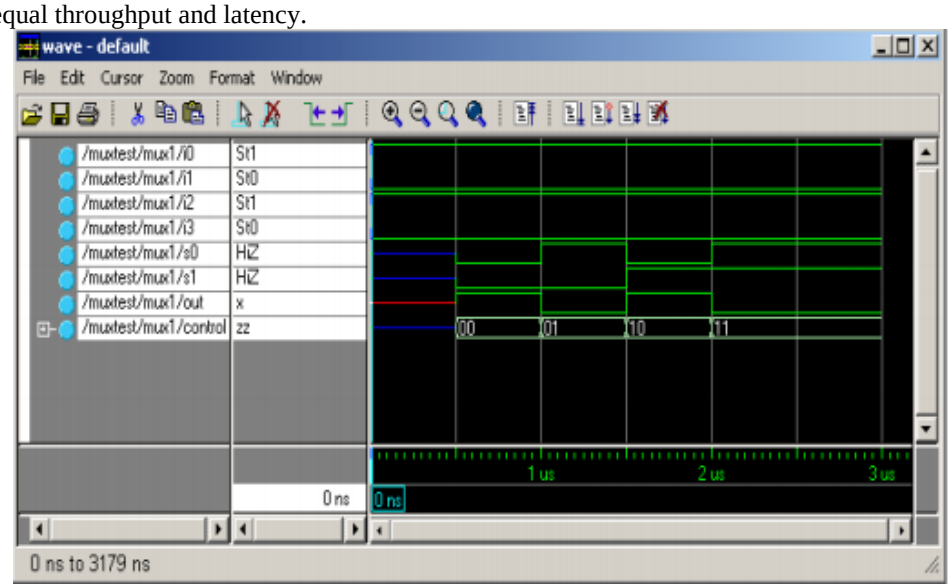

Fig.5.Proposed Multiplier 32-Bit output

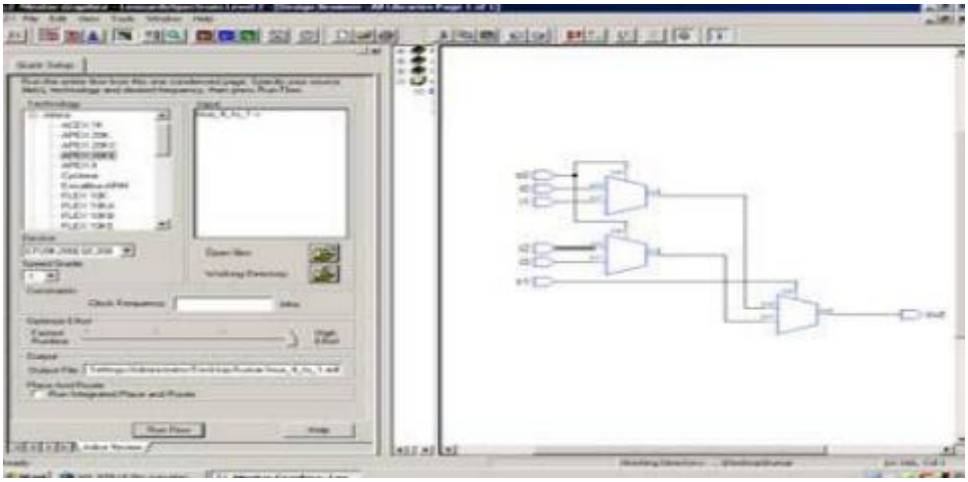

Fig.6.Proposed Multiplier 32-Bit Simulation Schematic

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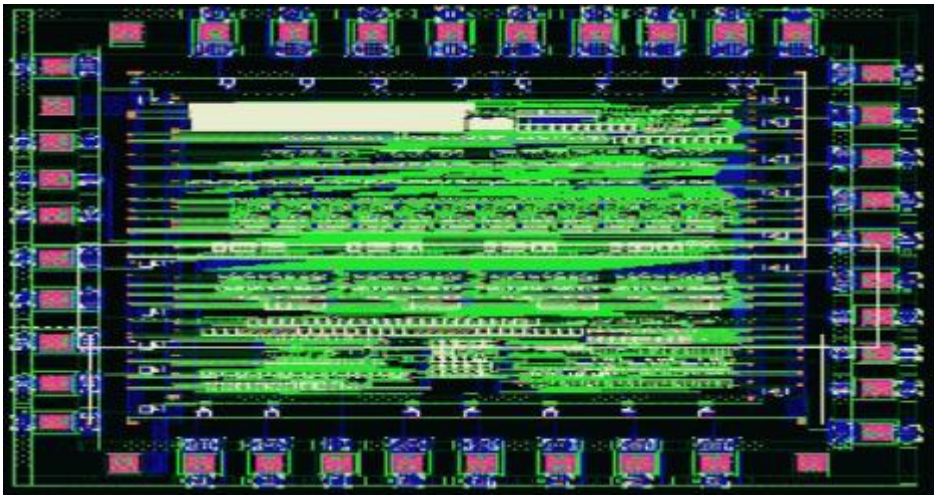

Fig.7.FPGA Nexys4DDR Kit .

V.FUTURE WORK DIRECTION

The present work on the new multiplier architecture can be extended in various directions. Some suggestions are given below. 1. In order to completely analyze the performance, the layout can be extended to chip level where the delays due to wiring, interconnects and PAD are included. 2. The multiplier can be designed in some other CMOS logic like Domino logic or Complementary Pass transistor Logic (CPL) etc. some logic families are faster than static CMOS logic, so it is important to analyze the performance for those families. 3. The adder tree structure can be changed by the use of other trees like delay-balanced, binary tree or overturned-staircase tree.

VI.CONCLUSION

In this thesis report energy-efficient 32-bit multiplier architecture has been presented. The architecture is based on a modified Booth-encoding scheme, which reduces the number of partial-products by half compared to a conventional implementation. Simulation results show that for equal delay the power-efficiency of the proposed architecture is improved by 47 % and the area is reduced by 24 % compared to a conventional implementation.

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