

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| <u>www.ijareeie.com</u> | Impact Factor: 7.122|

||Volume 9, Issue 8, August 2020||

Grid-Connected Symmetrical Cascaded Multilevel Converter for Power Quality Improvement

P. Saraswathisandhya¹, R.Gunasekaran², G.Syed Zabiyullah³, J. Gnana Mahim⁴

PG Student, Excel College of Engineering and Technology, Komarapalayam, Tamilnadu, India¹ Assistant Professor, Department of EEE, Excel College of Engineering and Technology, Komarapalayam, Tamilnadu, India² Assistant Professor, Department of EEE, Excel College of Engineering and Technology, Komarapalayam, Tamilnadu, India³ PG Student, Excel College of Engineering and Technology, Komarapalayam, Tamilnadu, India⁴

ABSTRACT: The cascaded multilevel converter is the converter for flexible power conditioning in smart grid applications. In the proposed method is the use of independent DC links, with reduced voltages, which makes such a topology an ideal candidate for medium and high-power applications with increased reliability. The system contain Cascaded multilevel converters to achieve higher power quality with a given switch count when compared to traditional multilevel converters it splits high-voltage/low-frequency and low-voltage pulse width modulation (PWM)-frequency power production The developed control strategy regulates independent DC-link voltages in each H-bridge cell and allows selective and flexible compensation of disturbing currents under a variety of voltage conditions without requiring any reference frame transformation. The selective control strategies are based on the decompositions that proposed in the Conservative Power Theory (CPT), which result in several current-related terms associated with specific load characteristics. These current components are independent of each other and may be used to define different compensation strategies, which can be selective in minimizing particular effects of disturbing loads. Experimental results are provided to validate the possibilities and performance of the proposed controlstrategies, considering ideal and deteriorated voltage conditions.

I.INTRODUCTION

There are alternative methodologies that may prove more flexible than the ones above, providing a simpler way to compensate for disturbances selectively, and simplifying our understanding of the related electrical characteristics. In this context, this method proposes to use CPT as an alternative framework for the development of electronic power processors (EPP), especially to the design of physical elements and to the definition of selective compensation strategies for multifunctional grid-tied inverters or shunt active filters. This is because the proper choice of which portions should be compensated is a critical factor for the project, since the actual nominal value directly influences the requirements of the active and passive elements of the EPP, and thus, the financial cost of their installations. From the converter's topology point of view, multilevel inverters have several merits over conventional inverters, such as low total harmonics distortion (THD), low switching losses, good power quality, reduced electromagnetic interference (EMI), modularity and low switch voltage stress of electronic components.

The primary component of the proposed conspire is the utilization of free dc joins with lessened voltages, which makes such a topology a perfect contender for medium-and high-control applications with expanded dependability.

The created control technique manages free dc-connect voltages in every H-connect cell, and permits the particular and adaptable pay of exasperating streams under an assortment of voltage conditions without requiring any reference outline change.

The Modified Cascaded Multilevel inverter consists of MOSFET switches and Power Diodes thus by using this inverter the switching losses are reduced because the power semiconductor switches are reduced and the complicity of circuit minimized thus the circuit having power semiconductor switches having more complex network. The main objective is to improve the quality output voltage of the multilevel inverter with reduced number of switches



| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| <u>www.ijareeie.com</u> | Impact Factor: 7.122|

||Volume 9, Issue 8, August 2020||

II.BLOCK DIAGRAM



BLOCK DIAGRAM EXPLANATION:

CASCADED MULTILEVEL INVERTER:

The CMI has been utilized in a wide range of applications. With itsmodularityand flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By adding more H-bridge converters, the amount of Var can simply increase without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized. A series of single-phase full bridges makes up a phase for the inverter. A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing. This feature is impossible in other VSC topologies utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. Phase-shifted transformers can supply the cells in medium-voltage systems in order to provide high power quality at the utility connection.

Operation of CMLI:

The converter topology is based on the series connection of single-phase inverters with separate dc sources. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from -Vdc to +Vdc with three levels, -2Vdc to +2Vdc with five-level and -3Vdc to +3Vdc with seven-level inverter. The staircase waveform is nearly sinusoidal, even without filtering. For a



| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| <u>www.ijareeie.com</u> | Impact Factor: 7.122|

||Volume 9, Issue 8, August 2020||

three-phase system, the output voltage of the three cascaded converters can be connected in either wye (Y) or delta (Δ) configurations

Features of CMLI:

For real power conversions, (ac to dc and dc to ac), the cascaded-inverter needs separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, and biomass, etc. Connecting separated dc sources between two converters in a back-to-back fashion is not possible because a short circuit will be introduced when two back-to-back converters are not switching synchronously.

Pulse Width Modulation (PWM) Controller:

Pulse Width Modulation (PWM) is a nifty current control technique that enables you to control the speed of motors, heat output of heaters, and much more in an energy-efficient manner. Existing applications for PWM include, but are not limited to:

- Variable speed fan controllers.
- VRF HVAC compressor drives.
- > Hybrid and electric vehicle motor drive circuits.
- LED Dimmers.

PWM works by pulsating DC current, and varying the amount of time that each pulse stays 'on' to control the amount of current that flows to a device such as an <u>LED</u>. PWM is digital, which means that it has two states: on and off (which correspond to 1 and 0 in the binary context, which will become more relevant to you if using microcontrollers). The longer each pulse is on, the brighter the LED will be. Due to the fact that the interval between pulses is so brief, the LED doesn't actually turn off. In other words, the LED's power source switches on and off so fast (thousands of times per second) that the LED actually stays on without flickering. This is called PWM dimming, and such as circuit is just called a PWM LED dimmer circuit.

SWITCHING CIRCUIT:

Circuit switching is a connection-oriented network switching technique. Here, a dedicated route is established between the source and the destination and the entire message is transferred through it.

Phases of Circuit Switch Connection

• **Circuit Establishment**: In this phase, a dedicated circuit is established from the source to the destination through a number of intermediate switching centers.

• The sender and receiver transmit communication signals to request and acknowledge establishment of circuits.

• **Data Transfer**: Once the circuit has been established, data and voice are transferred from the source to the destination. The dedicated connection remains as long as the end parties communicate.

• **Circuit Disconnection**: When data transfer is complete, the connection is relinquished. The disconnection is initiated by any one of the users. Disconnection involves removal of all intermediate links from the sender to the receiver. **ADVANTAGES**:

• It is suitable for long continuous transmission, since a continuous transmission route is established, that remains throughout the conversation.

• The dedicated path ensures a steady data rate of communication.

• No intermediate delays are found once the circuit is established. So, they are suitable for real time communication of both voice and data transmission.

III.SIMULATION RESULTS

3.1 SIMULATION OUTPUT:

Cascaded H-Bridge multilevel Inverter with and without any noise, and filter is designed using MATLAB-Simulink. Fig.5.1 shows the pulse generation for circuit is obtained by comparing the sinusoidal waveform with triangular waveform and the triangular wave added with constant



| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| <u>www.ijareeie.com</u> | Impact Factor: 7.122|

||Volume 9, Issue 8, August 2020||



Figure 2: Simulation output of Cascaded H-Bridge multilevel Inverter

SOURCE OUTPUT WAVE FORM:

- > The output AC voltage waveform is obtained
- > The phase voltage, line voltage and the 3-phase output voltage of multilevel level inverter.

> The time equivalents for individual phase voltages are obtained for multilevel level cascaded multilevel inverter topology



Figure 3: Output waveform of Cascaded H-Bridge multilevel Inverter



| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| <u>www.ijareeie.com</u> | Impact Factor: 7.122|

||Volume 9, Issue 8, August 2020||

THD ANALYSIS PHASE ANGLE A



• For the effectively utilize the supervisory control optimization the generation mode will reduce the total harmonics distortion the gain level of the THD is 5.35%

Method	Power	THD
	Source	(%)
EXISTING METHOD	DC input	29.98%
(Multilevel inverter)	source	
PROPOSED METHOD	DC input	5.35%
(PHASE ANGLE A)	source	
PROPOSED METHOD	DC input	5.27%
(PHASE ANGLE B)	source	
PROPOSED METHOD	DC input	2.40%
(PHASE ANGLE C)	source	
PROPOSED METHOD	DC input	5.35%
LINE VOLTAGE A	source	
PROPOSED METHOD	DC input	3.81%
LINE VOLTAGE B	source	
PROPOSED METHOD	DC input	1.10%
LINE VOLTAGE C	source	

Table 1: Comparison analysis of THD and Output power

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| <u>www.ijareeie.com</u> | Impact Factor: 7.122|

||Volume 9, Issue 8, August 2020||

Hardware	Speci- fication	Input Ranges	Output Ranges
Rectifier	Input power	110V AC	230V DC
Inverter	Output power	110V DC	110V AC
Current Transformer	Analog signal	5V	0-5A
Transformer	step-up	110v AC	230v AC
Motor	Load	230V	2A

Table 2 : HARDWARE SPECFICIATION

IV.CONCLUSION

This project proposes the use of a cascaded multilevel shunt converter as a flexible power conditioner, aiming to selective compensation of disturbing current components extracted using the Conservative Power Theory. Using multilevel converters has several merits, e.g., the modularity in the system configuration with increased reliability, also allowing the use of independent DC link voltages. These features by themselves already make this topology an ideal candidate for medium and high-power applications. Also, the developed control strategy regulates the output current by tracking references provided by CPT, without implementing any reference frame transformation. The proper choice of which portions should be compensated is a critical factor for the project, since the actual nominal value directly influences the requirements of the active and passive elements of the electronic power processor, and thus, the financial cost of its installation. Accordingly, the compensation strategy should meet the overall goals, within limits defined by regulatory standards, electricity operating constraints, and that is still favorable from the viewpoint of cost. Moreover, CPT-based compensation strategies allow for the specific compensation of disturbances caused by loads (reactive current, asymmetry, unbalances or nonlinearities). This is important regarding the appropriation of responsibilities in the case of smart micro grids or modern power grids.

V.FUTURE SCOPE

The cascaded converter, for example, can have four Capacitor-clamped multilevel inverter (CCMI), instead of three. In case of a semiconductor failure in one Capacitor-clamped multilevel inverter (CCMI) in the same phase leg, the rest of the Capacitor-clamped multilevel inverter (CCMI), can still generate a normal output voltage. The multilevel cascaded inverter configuration is simulated in open loop control using single PWM, multiple PWM and Sinusoidal PWM techniques. The simulation results are presented and analyzed. From this part of work, the sinusoidal PWM based simulation gives better results. Hence, it is taken for further studies in the proposed inverter.



| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| <u>www.ijareeie.com</u> | Impact Factor: 7.122|

||Volume 9, Issue 8, August 2020||

REFERENCES

1. Rajesh, B., & Manjesh. "Comparison of harmonics and THD suppression with three and 5 level multilevel invertercascaded H-bridge". International Conference on Circuit, Power and Computing Technologies (ICCPCT).year.2016

2. Mohamad, A. S., & Mariam, N. "Simulation of a 41-level inverter built by cascading two symmetric cascaded multilevel inverter". 7th IEEE Control and System Graduate Research Colloquium (ICSGRC).2016.

3. Kumar, S. S., & Sasikumar, M. "An approach of hybrid modulation in fusion seven-level cascaded multilevel inverter accomplishment to IM drive system". Second International Conference on Science Technology Engineering and Management (ICONSTEM). year.2016.

4. Sujitha, N., Karthika, B., Kumar, R. H., & Sasikumar, M. "Analysis of hybrid PWM control schemes for cascaded multilevel inverter fed industrial drives". International Conference on Circuits, Power and Computing Technologies, year.2014, PP, 978-1-4799-2397-7.

5. Javvaji, H. L., & Varaja, B. B. "Simulation & analysis of different parameters of various levels of cascaded H bridge multilevel inverter". IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics, year.2013, PP, 6731179.

6. Kumar, K. N., & Srinath, S. "Integration of UPQC with New Converter Transformer for Power Quality Improvement", National Power Engineering Conference (NPEC), 2018.

7. Rao, S. N., Kumar, D. V. A., & Babu, C. S. "New multilevel inverter topology with reduced number of switches using advanced modulation strategies". International Conference on Power, Energy and Control (ICPEC).Year, 2013. pp. 978-1-4673-6030.

8. Salehahari, S., & Babaei, E. "A new hybrid multilevel inverter based on coupled- inductor and cascaded Hbridge". International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON). year.2016.

P, S. P., Kalpana, R., Singh, B., & Bhuvaneswari, G. "Power quality improvement in front-end hybrid AC-DC converter based on current injection technique", IEEE Transportation Electrification Conference (ITEC-India), 2017
 Ovaskainen, M., Oorni, J., & Leinonen, A. "Superposed control strategies of a BESS for power exchange and Distribution of the power exchange and Distribution of

micro grid power quality improvement", IEEE International Conference on Environment and Electrical Engineering, 2018

BIOGRAPHY



R.GUNASEKARAN was completed his under graduation (B.E.,-EEE) in the year of 2003 at Kongu Engineering College, Perundurai and post graduated M.E (Power Electronics & Drives) atKSR College of Technology, Tiruchengode in the year of 2010. He isdoing Ph.D.,(parttime) in Anna university, Chennai at 2015 onwards.He is currently working as Assistant professor in the department of EEE at Excel College of Engineering and Technology, komarapalayamfrom June 2015. His teaching experience is more than 11 years and also published more than 03 reputed journals. He has membership inIndian society for Technical Education (ISTE). He was also published03 Engg. College books at Charulathapublication. His research interestinvolves in Power Electronics, Renewable Energy.