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Design and Analysis of Various Logic Circuits using Low Power VLSI Techniques

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ABSTRACT: In today's electronic industries low power is the major challenge. Power dissipation is the main consideration in the field of performance and in space for VLSI chip design. In this project there are different logic circuits which are combinational and sequential circuits, These are designed by reducing the number of transistors and power dissipation using low power VLSI techniques. Each and every proposed circuits has its own benefits in terms of speed, power consumption, driving ability, and so on. To determine the performance of the proposed designs, extensive mentor graphics simulations are used. The simulation output, based on the 65-nm CMOS process technology model, implies that the proposed designs have higher level speed and power against to other designs.

KEYWORDS: 4X1 multiplexer, full adder, d flip flop, ALU, pass transistor logic, transmission gate logic, adiabatic logic, conventional method, Mentor Graphics tool.

I.INTRODUCTION

With many of the latest advancements in the VLSI circuit designs delay, area and power have become a major constraint in high performance applications. For the compact or portable devices area is the prime constraint and power usage becomes an important issue in enhancement of reducing the charging time are becoming a challenging issues in present days. In addition to that of area and power, fast response of the system has become the essential criteria in the digital circuits. Intensified research in low power, high speed embedded systems has led the VLSI technology to scale down to nano technologies, allowing many of the functionality to be integrated on a single chip. These efforts led to several different design techniques for digital circuits apart from traditional CMOS design style. Pass transistor logic style is one of the new technique.

Aim of the Project: Main objective of this project is to implement some of the combinational and sequential logic circuits with low power design techniques and to compare the power dissipation produced in each technique, and with the help of less power dissipated logic circuits there will be implementation of an ALU using mentor graphics. To minimize the power consumption and to increase the speed there are different low power design styles used.

II. PROPOSED METHODOLOGY

1. Transmission gate logic

By the parallel connection of PMOS and NMOS devices we can create a primary bilateral CMOS switch, called as Transmission gate. A Transmission gate is an analog gate affiliated to a relay that can conduct in two directions or blocked by a control signal with any potential. In this PMOS passes a strong 1 but poor 0, and strong 0 but poor 1.Both PMOS and NMOS work at a time. By using this logic Full adder, D flip flop and 4x1 mux is implemented.

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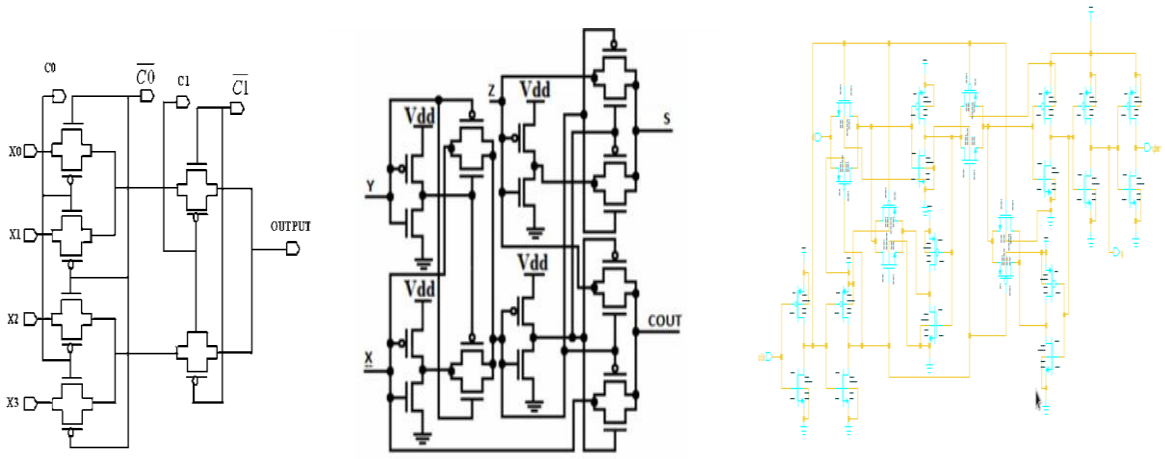
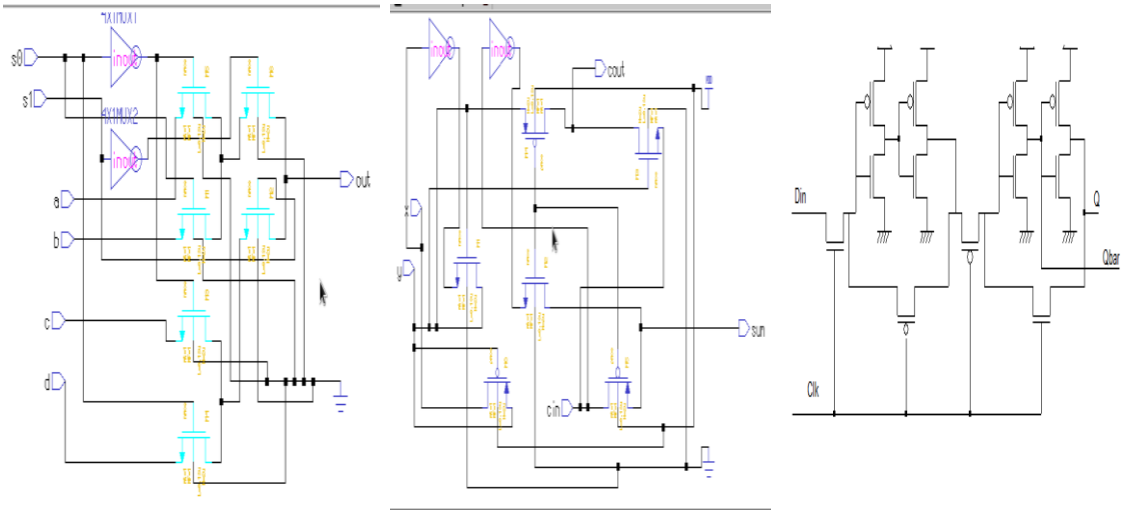


(a) 4X1 mux (b) full adder (c) D flip flop

Fig 1: Transmission gate logic implementation of circuits

2. Pass transistor logic:

Pass transistor logic reduces the count of transistors used to make several logic gates, by removing redundant transistors. This declines the number of active devices, but has the demerit that the difference of voltage between high and low logic levels reduced at each level. CMOS or complementary metal oxide semiconductor are said to offer better density along with decreasing nominal supply voltage. In this project by using the pass transistor logic Full adder, D flip flop and 4x1 mux are implemented.



(a)4X1 mux (b) full adder (c) D flip flop

Fig 2: pass transistor logic implementation of circuits

3. Adiabatic logic:

The adiabatic logic which is given to low power electronic circuits the implement reversible logic. In this case the total heat or energy in the system remains the same. By implementing this logic the circuits get smaller and faster, their energy dissipation greatly grows, a difficulty that adiabatic circuit promises to solve. Again by using this logic Full adder, D flip flop and 4x1 mux are implemented.

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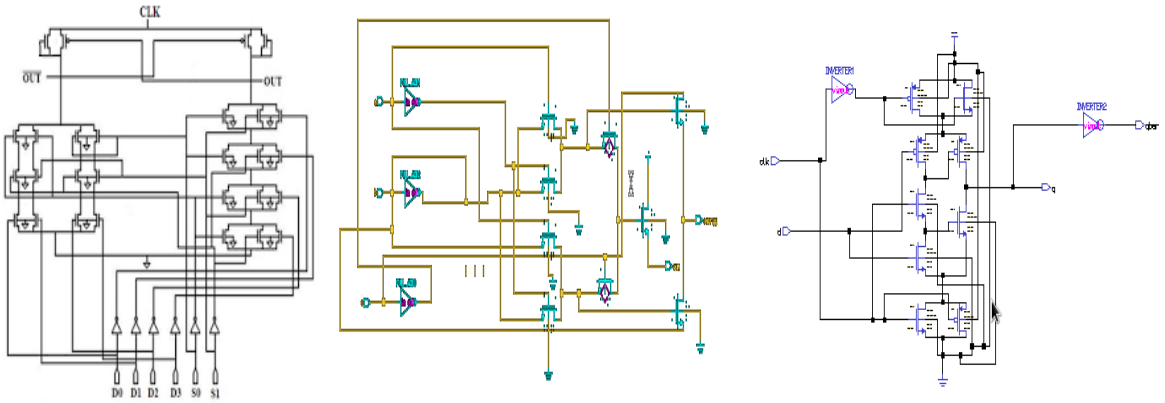

(a) 4X1 mux (b) full adder (c) D flip flop

(b)

Fig 3: adiabatic logic implementation of circuits

III. ALU IMPLEMENTATION

The conventional ALU circuit which contains inputs NAND, NOR, BUFFER, INVERTER, FULL ADDER, D FLIP FLOP and 2 selection lines and the output is taken out depends on selection lines. The Test bench is designed and the output waveform is obtained for the circuit.

In proposed ALU circuit which has inputs NAND, NOR, BUFFER, INVERTER, FULL ADDER, D FLIP FLOP and 2 selection lines and the output is extracted based on selection lines. The test bench is designed and the resultant waveform is produced for the circuit.

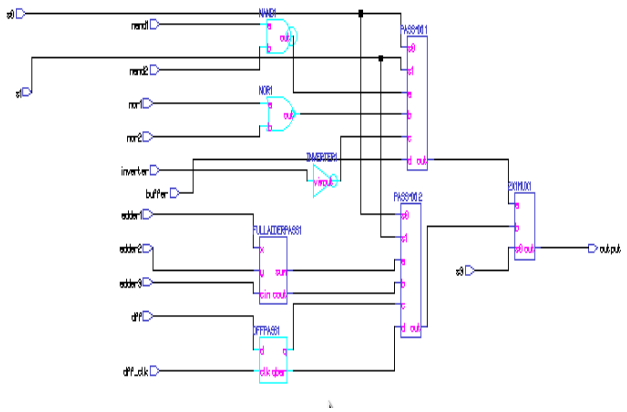

Fig 4 :ALU implementation using pass transistor based circuits

IV. RESULTS

All the circuits have been simulated using Mentorgraphics in the 130-nm CMOS process technology, and were supplied with 5v as well as the maximum frequency for the inputs was 1GHz. The simulated waveforms of various circuits are shown below.

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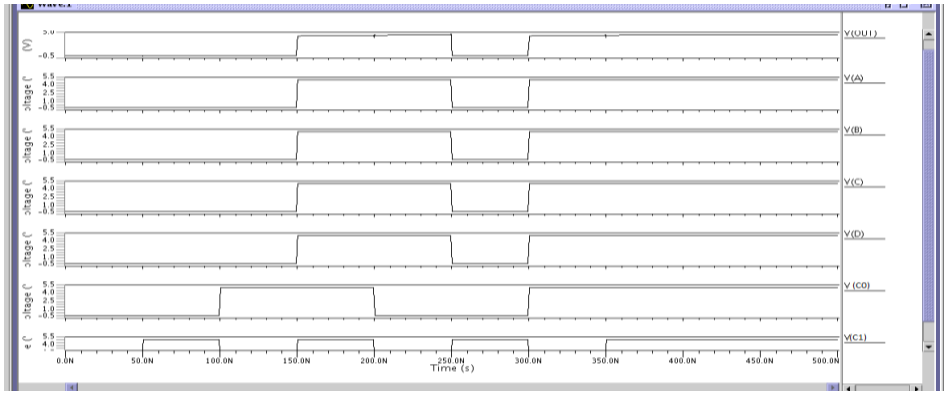


Fig V(A) simulated waveform of 4X1 mux

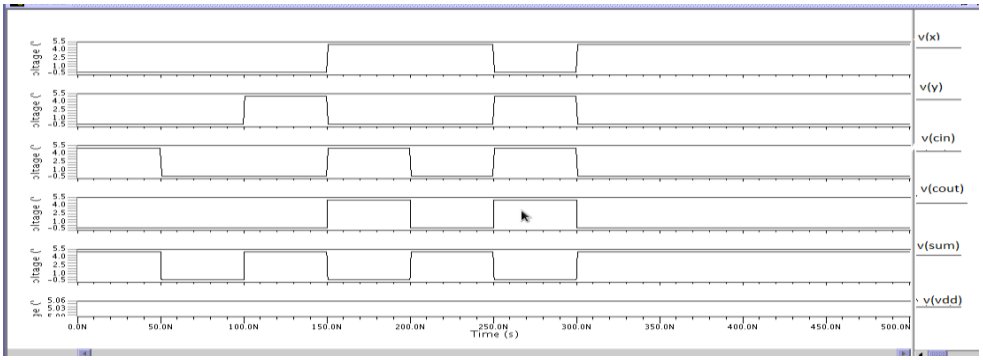


Fig:V(B)simulated waveform of full adder

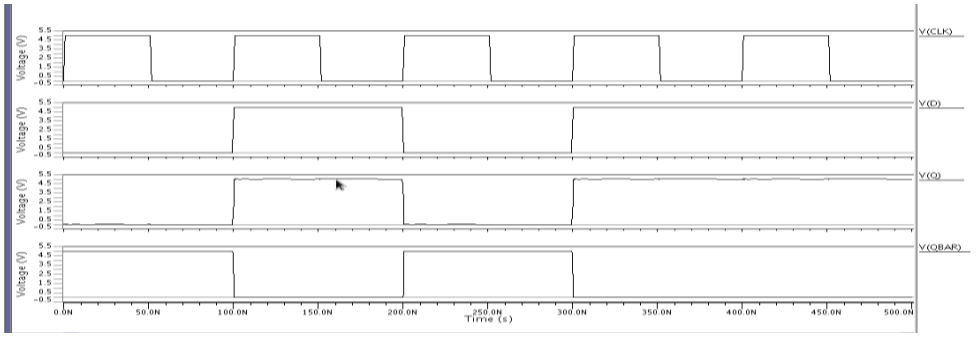
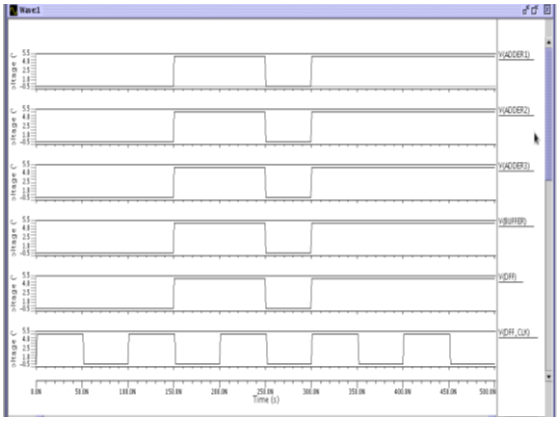
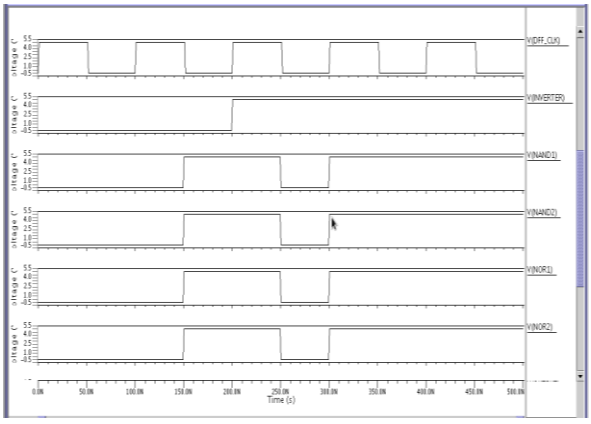


Fig: V(C)simulated waveform of D flipflop





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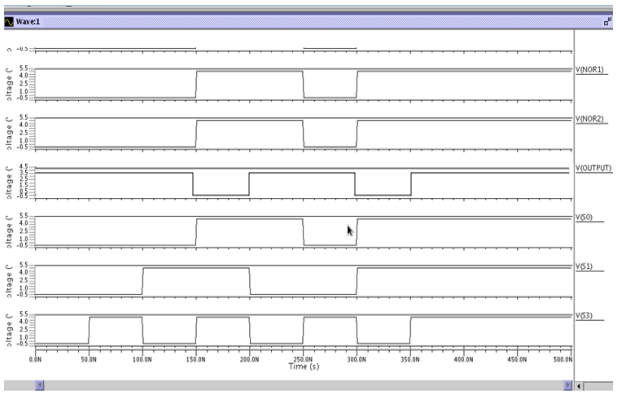

Fig:V(D)simulated waveforms for ALU

V. COMPARISON TABLES

Table 1: Power Dissipation and number of transistors in 4x1 multiplexer

Techniques	Conventional method	Transmission gate logic	Pass transistor logic	Adiabatic logic
Supply voltage	5v	5v	5v	5v
Power dissipation	53.3mw	152.8603nw	125.5603nw	457.7810nw
Number of transistors	42	12	6	28

Table 2: Power Dissipation and number of transistors in full adder

Techniques	conventional method	Transmission gate logic	Pass transistor logic	Adiabatic logic
Supply voltage	5v	5V	5v	5V
Power dissipation	700.9266nw	542.5739nw	250.1661nw	300nw
Number of transistors	28	20	6	9

Table 3: Power Dissipation and number of transistors in D flip flop

Techniques	Conventional method	Transmission gate logic	Pass transistor logic	Adiabatic logic
Supply voltage	5v	5v	5v	5v
Power dissipation	243.1793nw	487.5103nw	196.9402nw	297.6702nw
Number of transistors	18	24	12	9

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Table 4: Power Dissipation in ALU

Method	Conventional	proposed
Power dissipation	123mw	1.1635 microwatts

VI. CONCLUSION

Finally the result shows that using the conventional method for implementing the logic circuits there will be more power dissipation and number of transistors also increases. So that here three types of techniques used for implementing the same logic circuits and comparison is made between these techniques. Finally pass transistor logic is best logic for implementing the combinational and sequential circuits. Then the proposed new ALU based on pass transistor logic produces the best results compared to conventional ALU.

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