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Power Quality Improvement in TPFW Distribution System using Three-Leg Split Capacitor based DSTATCOM

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ABSTRACT:This paper suggests a DSTATCOM for TPFW systems based on three leg split capacitors. This topology uses an interfacing inductor, which also serves as a filter, to couple the DSTATCOM to the line. The voltage unbalance problem across the split capacitors at the front end of DSTATCOM is the main disadvantage of the split capacitor-based DSTATCOM. Neutral inductor is used to solve the voltage unbalance problem mentioned above. To avoid the voltage unbalancing problem associated with split capacitor-based DSTATCOM, the split capacitors are combined into a single dc link capacitor in this topology. The results of simulation studies for these topologies are presented.

KEYWORDS:Distribution Static Compensator (DSTATCOM), Voltage Source Inverter (VSI), Hysteresis Band Current Controller (HBCC), Proportional Integral (PI) Controller.

I. INTRODUCTION

The majority of our load systems are non-linear and unbalanced. These loads start to be used, which causes an excessive amount of neutral current to start flowing through the neutral conductor. This causes the neutral conductor to be overloaded and the source currents to be distorted, which heats up the system and shortens its lifespan. Other significant effects on the distribution systems will result from it. A corrective device called DSTATCOM is used to mitigate such power quality problems. DSTATCOM is nothing more than an inverter that adds reactive power to the line that is connected to the load. Reactive power compensation is what this is commonly known as. Due to the fact that DSTATCOM is connected parallel to the line using an interfacing inductor that also serves as a filter, it is essentially a shunt compensator. DSTATCOM must be able to carry out tasks like neutral current compensation, harmonic compensation, load balancing, and power factor correction.

By balancing the load, you can transform the distorted source current that results from using non-linear loads into a balanced sinusoidal current. The source currents become distorted when non-linear loads are used. This causes the neutral conductor to become overloaded as the difference between the source currents begins to flow through it as a neutral current. The neutral current in the system must also be able to be compensated for by DSTATCOM.Different DSTATCOM topologies come in various varieties. It is primarily categorised according to their structural makeup and the kinds of control algorithms employed. There has been a thorough analysis of the various DSTATCOM topologies reported. Transformer or magnetic-based topologies and inverter-based topologies are the two primary categories of DSTATCOM topologies. Magnetic-based topologies enable very straightforward and efficient compensation. This topology's primary flaw is that it adds bulk to the system. Therefore, inverter-based topology, another DSTATCOM topology, is utilised for compensation. Inverter-based topologies can be divided into four main categories. The four-leg VSI-based DSTATCOM, the three single-phase VSIs, the three-leg VSI with split capacitors, and the three-leg VSI with the neutral terminal at the positive or negative of the three legs are among them.

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II. STRUCTURE OF THREE LEG SPLIT CAPACITOR BASED DSTATCOM

Fig 1 represents the three leg split capacitor based DSTATCOM. In this topology, the split capacitor model is used before the DSTATCOM and to compensate the neutral current, both the source neutral and load neutral are connected to the middle of the two capacitors.

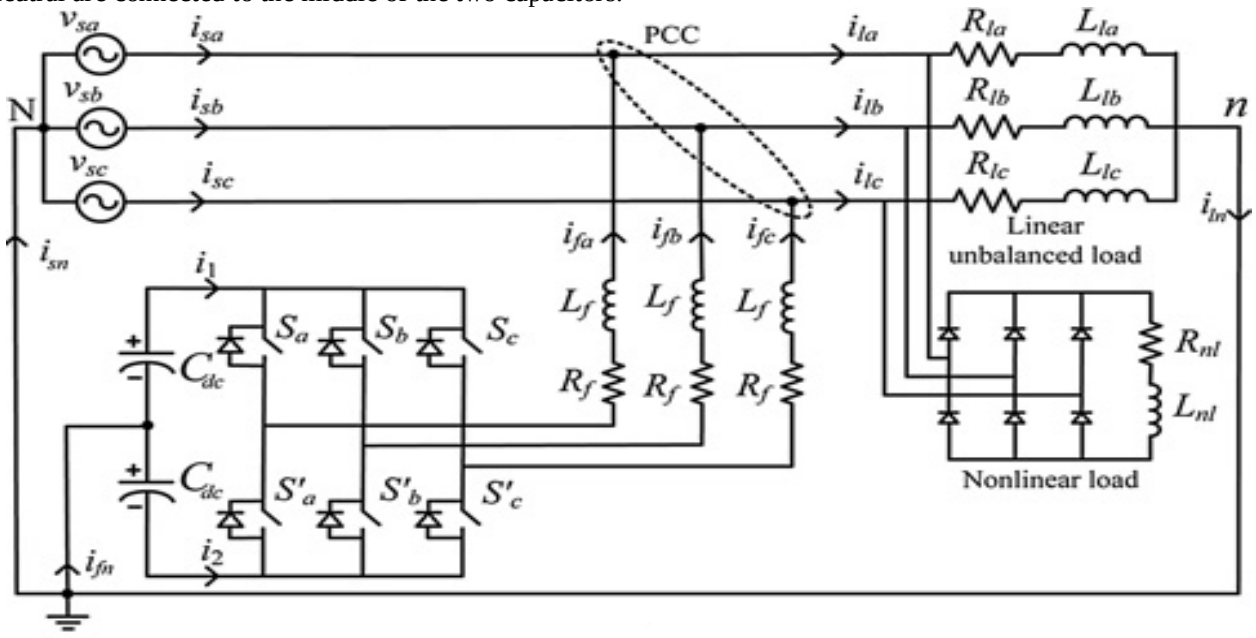

Fig. 1:Three leg split capacitor based DSTATCOM

III. DESIGN OF PROPOSED TOPOLOGY

A. Design of split capacitor based DSTATCOM

The criteria to be taken into account when designing are, (i) DC link voltage (V_{dc}) (ii) DC storage capacitor (C_{dc}) (iii) Interfacing inductance (L_f) (iv) Switching frequency (F_{sw})

A.1 DC link capacitor value (C_{dc})

It is given by,

$$C_{dc} = \frac{\left(2X - \frac{X}{2}\right)nT}{(1.8Vm)^2 - (1.4Vm)^2} \quad (1)$$

where, X is the DSTATCOM KVA rating, $V_m$is the peak value of source voltage, T is the time period of each cycle, n is the number of cycles.

A.2 Interfacing inductance (L_f)

It is given by,

$$L_f = \frac{1.6Vm}{4hF_{swmax}} \quad (2)$$

where, $h = \frac{k1}{k2}\frac{(2m^2-1)}{4m^2}F_{swmax}$ (3)

K_1, $K_2$is the proportionality constants. $F_{swmax}$is the maximum switching frequency. $F_{swmin}$is the minimum switching frequency.

m is given by,

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$$m = \frac{1}{\sqrt{1-(\frac{F_{swmin}}{F_{swmax}})}} \qquad (4)$$

A.3 DC link voltage (V_{dc})

The voltage reference (V_{dcref}) of DC link capacitopr has been taken as $1.6V_m$ for each capacitor.

IV. CONTROL ALGORITHM

The procedures are as follows:

(i) Produce the reference filter currents (i*fabc).

(ii) Produce the pulses for VSI switches by comparing the reference filter currents (i*fabc) with the actual filter currents (ifabc).

(iii) Use PI controllers to keep the dc link voltage (Vdc) at a predetermined level (Vdcref).

Step 1: Generate reference filter currents (i^*_{fabc})

Instantaneous Symmetrical Component Theory (ISCT) is used to produce it. It's stated as,

$$i^*_{fa} = i_{la} - \frac{V_{sa} + \beta\,(V_{sb} - V_{sc})}{\sum_{j=a,b,c} V_{sj}^2}(P_l + P_{loss}) \qquad (5)$$

$$i^*_{fb} = i_{lb} - \frac{V_{sb} + \beta\,(V_{sc} - V_{sa})}{\sum_{j=a,b,c} V_{sj}^2}(P_l + P_{loss}) \qquad (6)$$

$$i^*_{fc} = i_{lc} - \frac{V_{sc} + \beta\,(V_{sa} - V_{sb})}{\sum_{j=a,b,c} V_{sj}^2}(P_l + P_{loss}) \qquad (7)$$

where, (i_{la}, i_{lb}, i_{lc}) represents the three phase load currents, (V_{sa}, V_{sb}, V_{sc}) represents the three phase source voltages, P_l is the average load power, P_{loss} represents the switching and ohmic losses in the actual compensator. $\beta = \frac{\tan \Phi}{\sqrt{3}}$. Φ is the desired phase angle between source voltage and current. In order to obtain unity power factor (UPF), the value of β was chosen as zero.

Average load power (P_l) is given by the equation,

$$P_l = \frac{1}{T}\int_{t_1-T}^{t_1}(V_{sa}i_{la} + V_{sb}i_{lb} + V_{sc}i_{lc})\,dt \qquad (8)$$

P_{loss} is given by the equation,

$$P_{loss} = K_p e_{vdc} + K_i \int e_{vdc}\,dt \qquad (9)$$

where, $e_{vdc} = V_{dcref} - V_{dc}$. (i.e) the error difference between reference dc link voltage and actual dc link voltage, K_p is the proportional gain, K_i is the integral gain.

Step 2 : Generate the pulses for VSI switches

Using a Hysteresis Band Current Controller (HBCC) method, the pulses for VSI switches are produced. According to the switching control law,

(i) If $i_{fa} \geq i^*_{fa} + h$, then bottom switch is turned ON whereas the top switch is turned OFF. ($U_a = 0$, $\overline{U_a} = 1$).

U_a denotes all the VSI top switches.

$\overline{U_a}$ denotes all the VSI bottom switches.

(ii) If $i_{fa} \leq i^*_{fa} - h$, then bottom switch is turned OFF whereas the top switch is turned ON. ($U_a = 1$, $\overline{U_a} = 0$).

Only the 'a' phase is covered by the control law previously stated. The final two phases also employ the same control strategy.

The HBCC, where the value of hysteresis bandwidth is set, receives the error value between the three phase actual filter currents (ifabc) and the reference filter currents (i*fabc). To produce the pulses for the VSI switches, any switching control technique may be used in the HBCC.

Step 3: To maintain the dc link voltage (V_{dc}) at a reference value with the help of PI controller.

Using a PI controller, the voltage on the DC link capacitor is kept constant. The average value of dc current through the

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capacitor must be zero in order to maintain a constant average dc voltage across it. The formula for dc link voltage (vdc) is as follows:,

$$V_{dc} = \left(\frac{1}{C_{dc}}\right) \int i_{dc}\, dt \qquad (10)$$

It is evident from equation (9) that Vdc is only kept constant if idc is zero. Idc is a symbol for the average DC current flowing through the DC link capacitor. A small deviation of idc from zero is the result of the deviation of Vdc from the reference value Vdcref at the end of each cycle. Therefore, a small proportional-integral controller is used to prevent Vdc deviation. Equation (10 is used to design the PI controller.

V. SIMULATION RESULTS

The DSTATCOM topology's performance is using the same kind of unbalanced load and non-linear load.

V.A Steady state performance of proposed the DSTATCOM topology.

In steady state performance, the load remains constant for the duration of the simulation. The DSTATCOM topologies maintain the same three phase source voltage (Vsabc).

Table I:System parameters

Parameters	values
	Split capacitor based DSTATCOM
Grid voltage	400 V L-L (rms), 50 Hz
DC capacitor	C_{dc}= 1150 µF
DC-link voltage	V_{dc} = 520 (across each capacitor)
Neutral capacitor	No Neutral Capacitor is used
Interfacing inductor	L_f = 30 mH
Interfacing resistance	R_f = 0.5 Ω
Hysteresis band	±h = 5% of the compensator current
Voltage controller PI gains	K_p = 50, K_i = 0.05
Linear load	Zla = 17.5 + j7.8 Ω, Zlb = 27.5 + j12.5 Ω, Zlc = 37.5 + j31.4 Ω
Non-linear load	3 ϕ diode bridge rectifier

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V.A.1 Steady state performance of three leg split capacitor based DSTATCOM

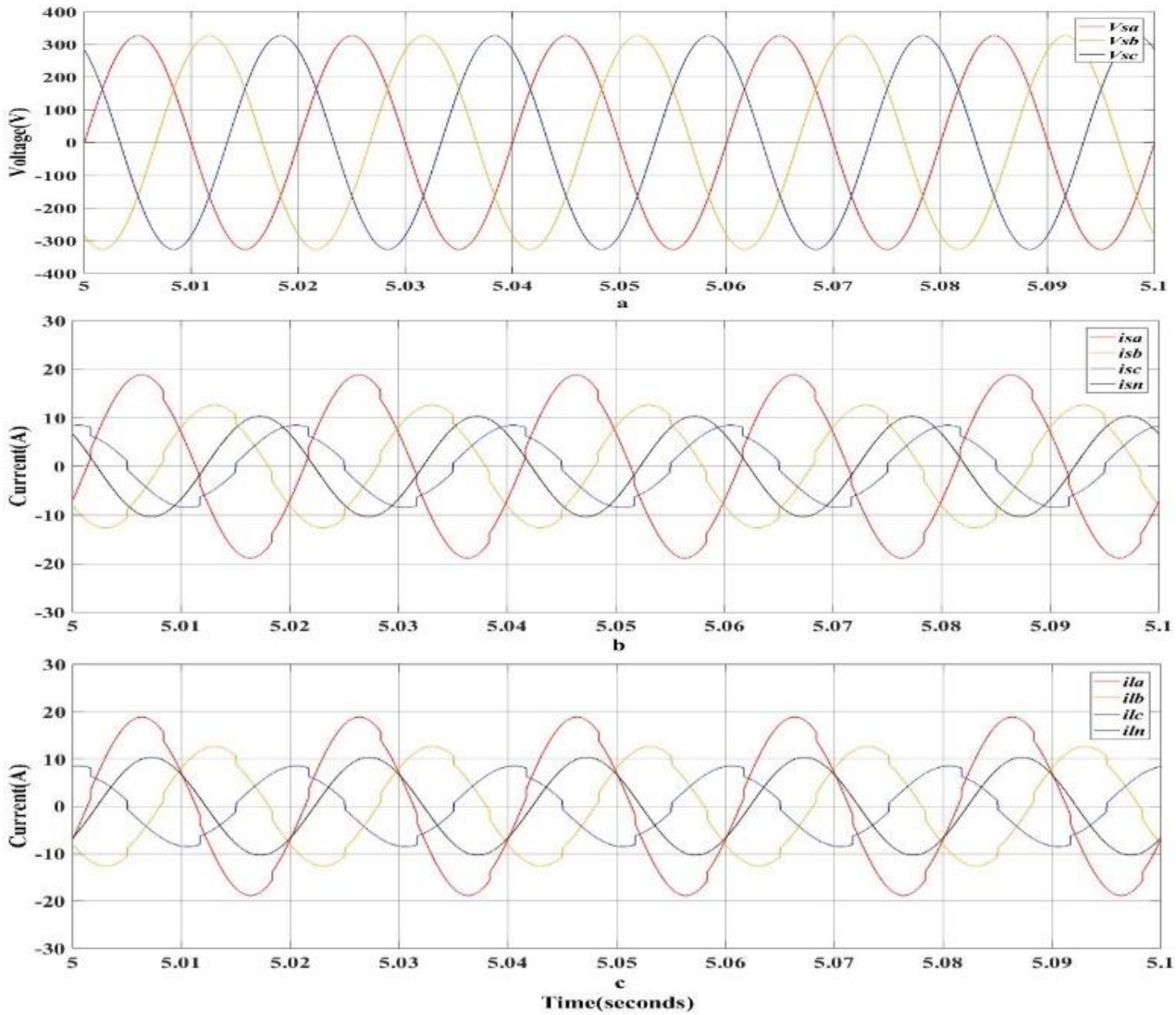

Fig. 2: Steady state performance of split capacitor based DSTATCOM before compensation

a) source voltages (V_{sabc})
b) source currents (i_{sabc}) and source neutral current (i_{sn}) before compensation
c) load currents (i_{labc}) and load neutral (i_{ln})

The source currents become distorted when non-linear loads are used. The distorted source currents and source neutral current are depicted in Fig. 2-a.

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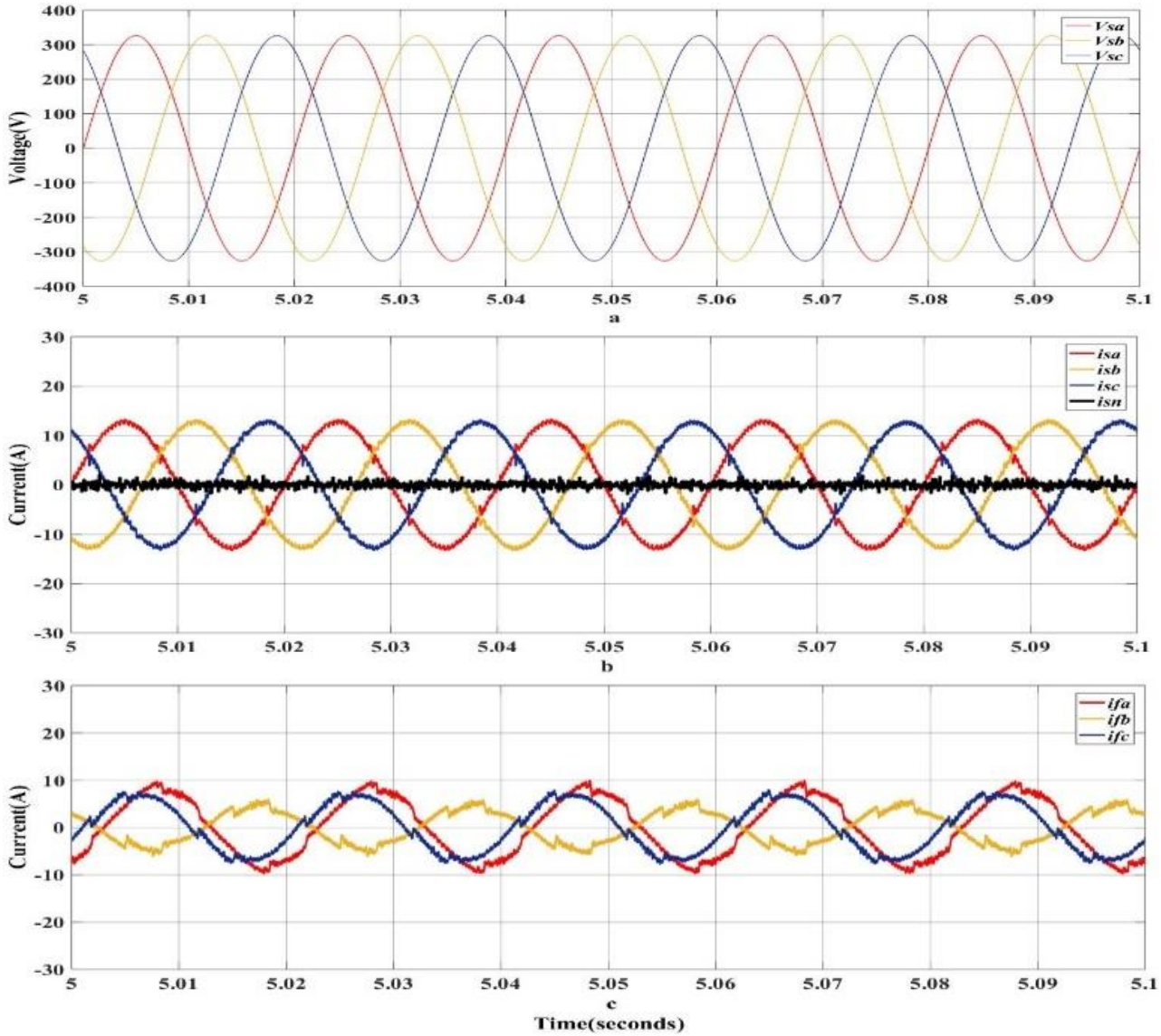

Fig. 3: Steady state performance of split capacitor based DSTATCOM after compensation

a) source voltages (V_{sabc})
b) source currents (i_{sabc}) and source neutral current (i_{sn}) after compensation
c) filter currents (i_{fabc})

The source currents and source neutral current are shown in Fig. 3-b following DSTATCOM's compensation. The compensator (filter) currents provided by DSTATCOM to balance the system's source parameters are shown in Fig.3-c.

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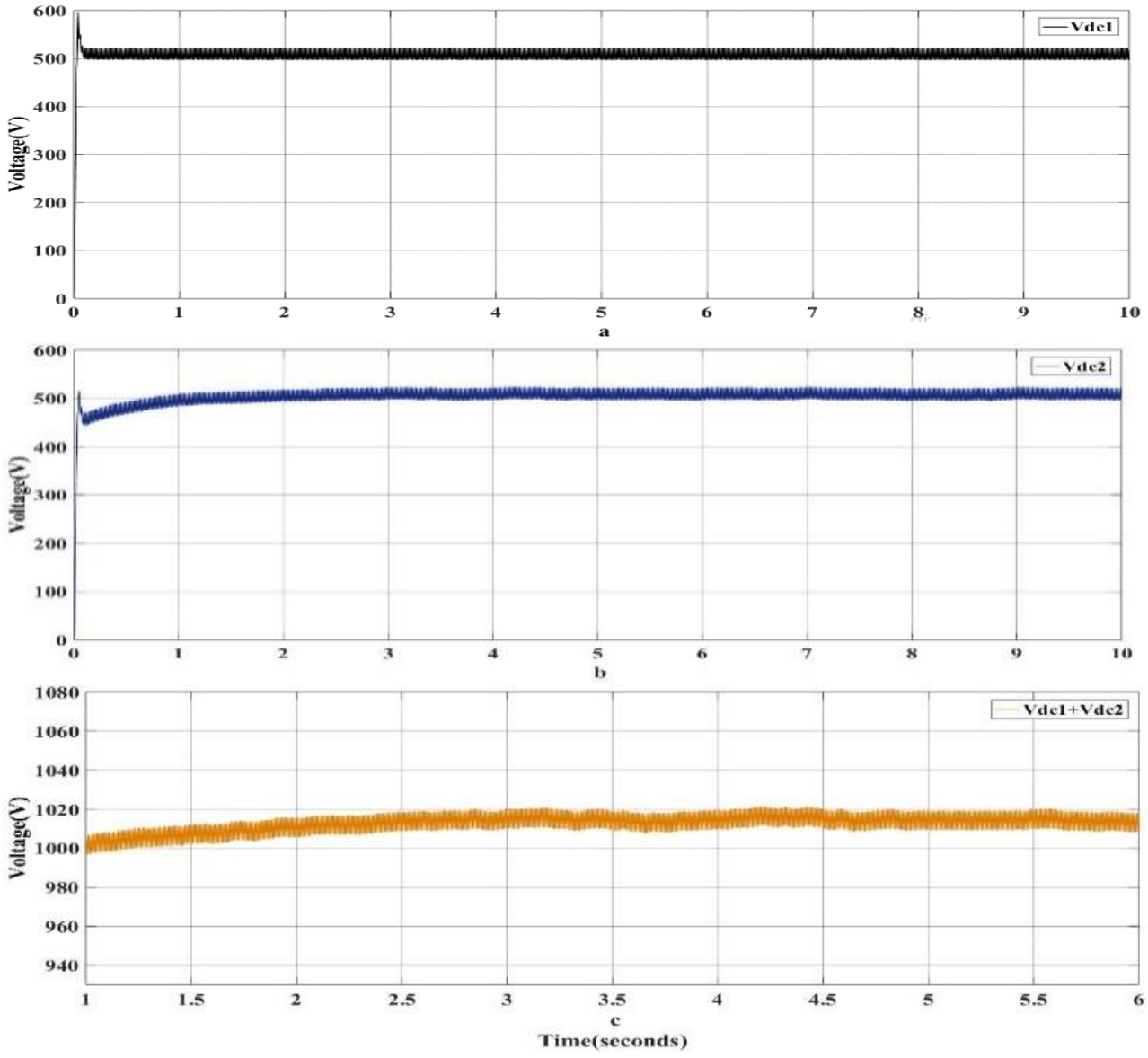

Fig. 4: DC link voltage (V_{dc}) across the dc link capacitors in split capacitor based DSTATCOM

a) dc link voltage across the first capacitor (V_{dc1})
b) dc link voltage across the second capacitor (V_{dc2})
c) zoomed view of voltage unbalance across the two split capacitors ($V_{dc1} + V_{dc2}$)

The voltage (Vdc1, Vdc2) is nearly maintained at 520 V with the aid of PI controllers. The voltage unbalancing problem is this topology's main flaw. In Fig. 4-c, the voltage imbalance is depicted. This voltage will put the VSI switches under more strain, which will reduce the system's performance.

Another important factor is when the load contains more amount of dc component, it will lead to major voltage unbalancing issue across the capacitors.

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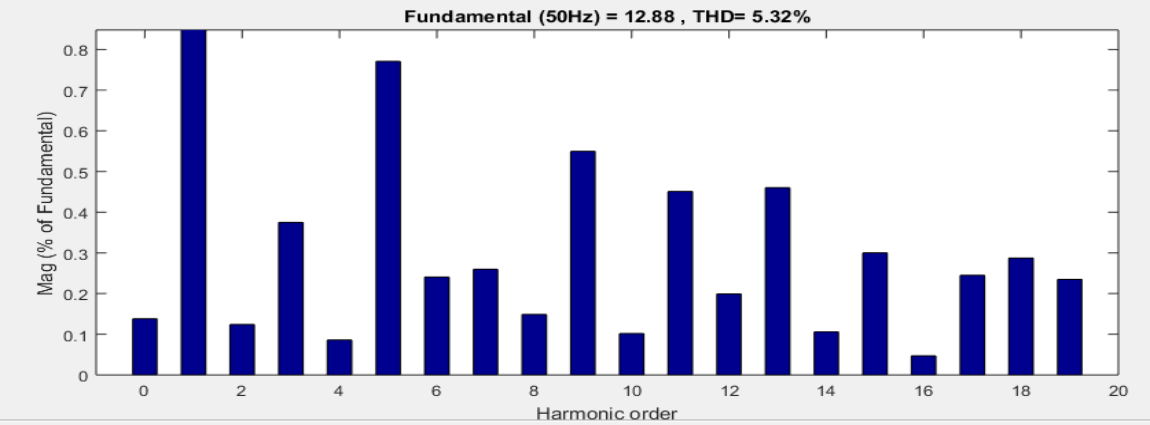

Fig. 5: Harmonic spectrum of phase 'a' in Split capacitor based DSTATCOM

VI. CONCLUSION

Through a number of simulation studies, the effectiveness of the proposed topology for power factor correction, load balancing, harmonic compensation, and neutral current compensation is shown. A major issue with the split capacitor-based DSTATCOM topology is that it has an excessive amount of dc components and voltage unbalance. However, it has the advantage of having no voltage unbalance issues, having a small ac neutral capacitor to eliminate source neutral current, and having a low dc component in source currents. Therefore, when split capacitor based DSTATCOM is used, it performs well overall.

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