ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 1, January 2018

Implementation of Cascaded H-Bridge Multilevel Inverter with Equal Dc Voltage Source

P.Rajyalakshmi[1], V.Praveen[2]

Assistant Professor, Dept. of EEE, Visvodaya Engineering College, Kavali, Andhrapradesh, India[1]

Assistant Professor, Dept. of EEE, PSCMR College of Engineering & Technology, Vijayawada, Andhrapradesh, India[2]

ABSTRACT: Now days it is not possible to link the semiconductor gadgets straight to medium and high voltage stages. In this situation new designs of inverters are presented as a outcome of implementing greater volts stages, which are known as Multiple stage Inverters or Multilevel inverters. The outcome currents of these multilevel inverters are shut to sinusoidal volts waveforms. Generally multi stage inverter produces the stairway–case volts trend types with some reduced harmonic material. This document offers with research and research of a single stage multilevel inverter with various stages. By using Matlab different multilevel inverter designs are simulated and get an outcome volts waveform and THD.

KEYWORDS: Multilevel Inverter, Matlab Simulink, FFT, THD

I.INTRODUCTION

Several multilevel inverter topologies have been designed. Almost 30 years ago, the NPC inverter techniques were proposed (A. Nabae, I.Takashahi, and H. Akagi), In 1992 travelling capacitor inverters are provided. One more substitute multiple stage inverter is the cascaded h-bridge inverter or sequence h-bridge inverters. These inverters are showed up in 1975. Mahesh Manvinna and Rama Reddy suggested a topology for stream h-bridge inverter[4]. This topology includes eight changes, eight diodes and two dc resources. The cascaded multilevel inverter was not completely noticed until two studies, Lai and peng. They trademarked it and provided various benefits in 1997. New inverter topology is provided here, inverter uses individual DC resources.

A multilevel inverter is an energy digital system that produces preferred outcome volts by linking several stages of dc feedback currents. The multilevel inverters have attracted remarkable interest in the energy market. Usually multilevel inverters are categorized into three kinds those are Diode Held, Flying-Capacitor, and Cascaded H-Bridge Inverter. The most important problem with diode- clamped inverter is to limit the high variety of energy function. In the same way travelling capacitor centred multilevel inverters also have a drawback such as more number of capacitors.

The above mentioned problems are getting over by using Stream H-bridge Inverters. The Stream H-bridge inverters have number of programs. The benefit includes ability to function at high voltage and medium voltage stages are improved, the quality of outcome indication is also enhanced. In addition to above benefits volts waveforms are shut to sinusoidal trend types.

Some of the primary popular functions of multilevel inverters are as follows:

1. For actual energy alterations from ac to dc and then dc to ac, the h link inverter need individual dc sources [1].
2. These inverters have greater performance because it can be turned at low regularity.
3. No transformer is needed in multiple stage inverters.

Advantages of stream h-bridge inverter:

1. When in contrast to other kinds of inverters, it needs least variety of elements with same variety of volts stages.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 1, January 2018

2. To limit the changing failures, the smooth changing methods are used.

II. CASCADE H-BRIDGE INVERTER

The ripper topology centred on the sequence relationship of individual stage inverters with individual dc resources. These inverters are showed up in 1975. Mahesh Manvinna and Rama Reddy suggested a topology for stream h-bridge inverter [4]. This topology includes eight changes, eight diodes and two dc resources. The cascaded multilevel inverter was not completely noticed until two studies, Lai and peng. They trademarked it and provided various benefits in 1997.

A three level inverter produces an output voltage level of 0, $+V_{dc}$ $-V_{dc}$. Three level inverter limits at high frequency because of switching losses and device rating constraints.

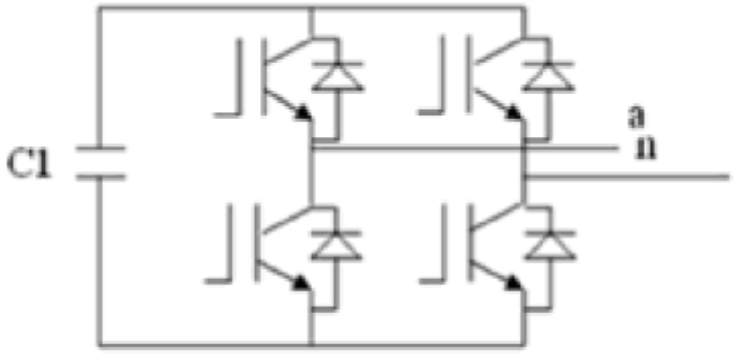

Fig. 1 Cascade H bridge multilevel inverter

Each level of inverter produces three different voltage output's namely, 0, $+V_{dc}$ $-V_{dc}$ by connecting an output with the dc supply using opposite combinations of the four switches, S_1,S_2,S_3,S_4. To taken $+V_{dc}$, switches $S_1$and S_4 are turned on, and $-V_{dc}$ can be taken by turning on S_2 and S_3. By turning on all the witches output becomes zero.

Voltage (Vo)	S1	S2	S3	S4
0	1	0	1	0
+Vdc	1	1	0	0
-Vdc	0	0	1	1
0	0	1	0	1

Switching table for Three level inverter

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 1, January 2018

***M* level cascade *h* bridge multi level inverter**

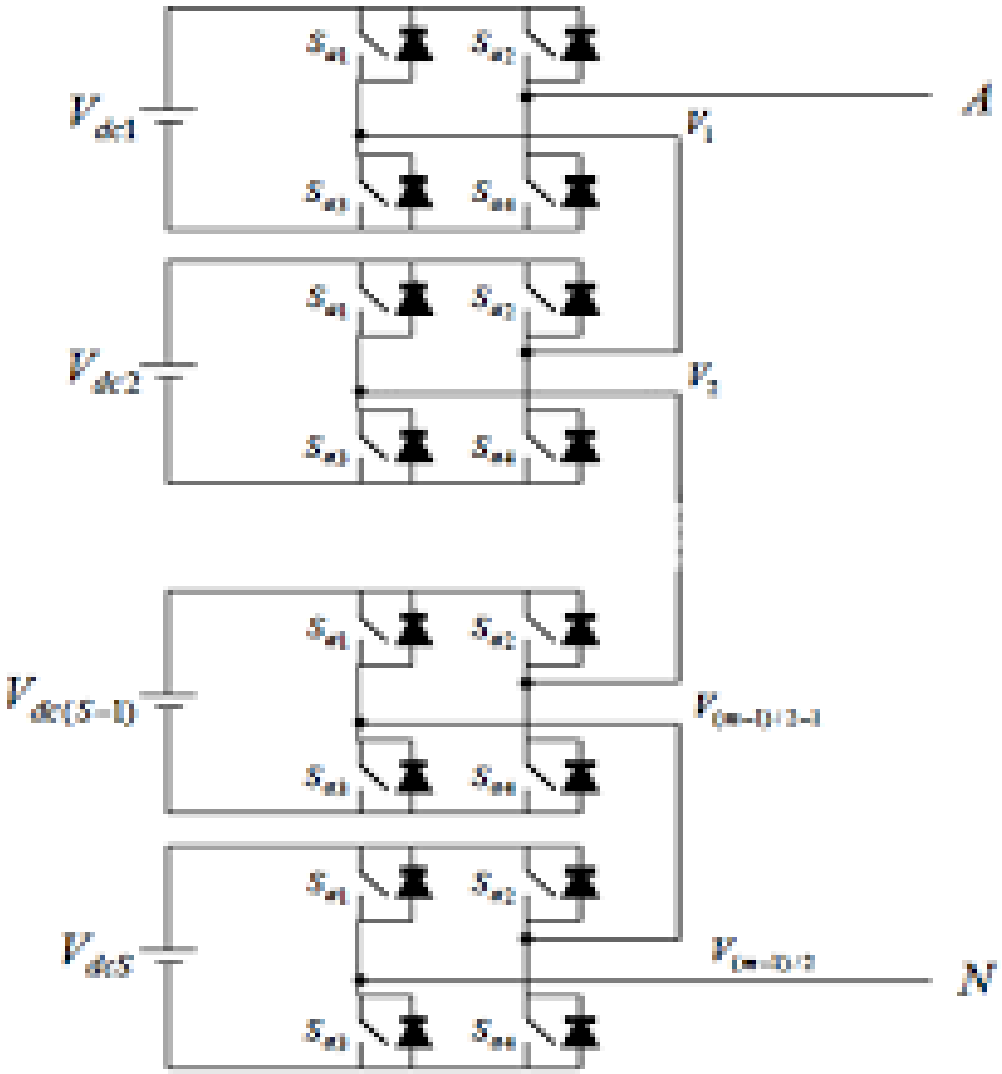

Fig 2. Circuit diagram of *m* level cascade *h* bridge multi level inverter.

In above figure each separate DC source is connected to an H-bridge inverter. The ac terminal voltages of different level inverters are connected in series.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 1, January 2018

The simulink model of Seventeen level inverter as shown in fig.3.

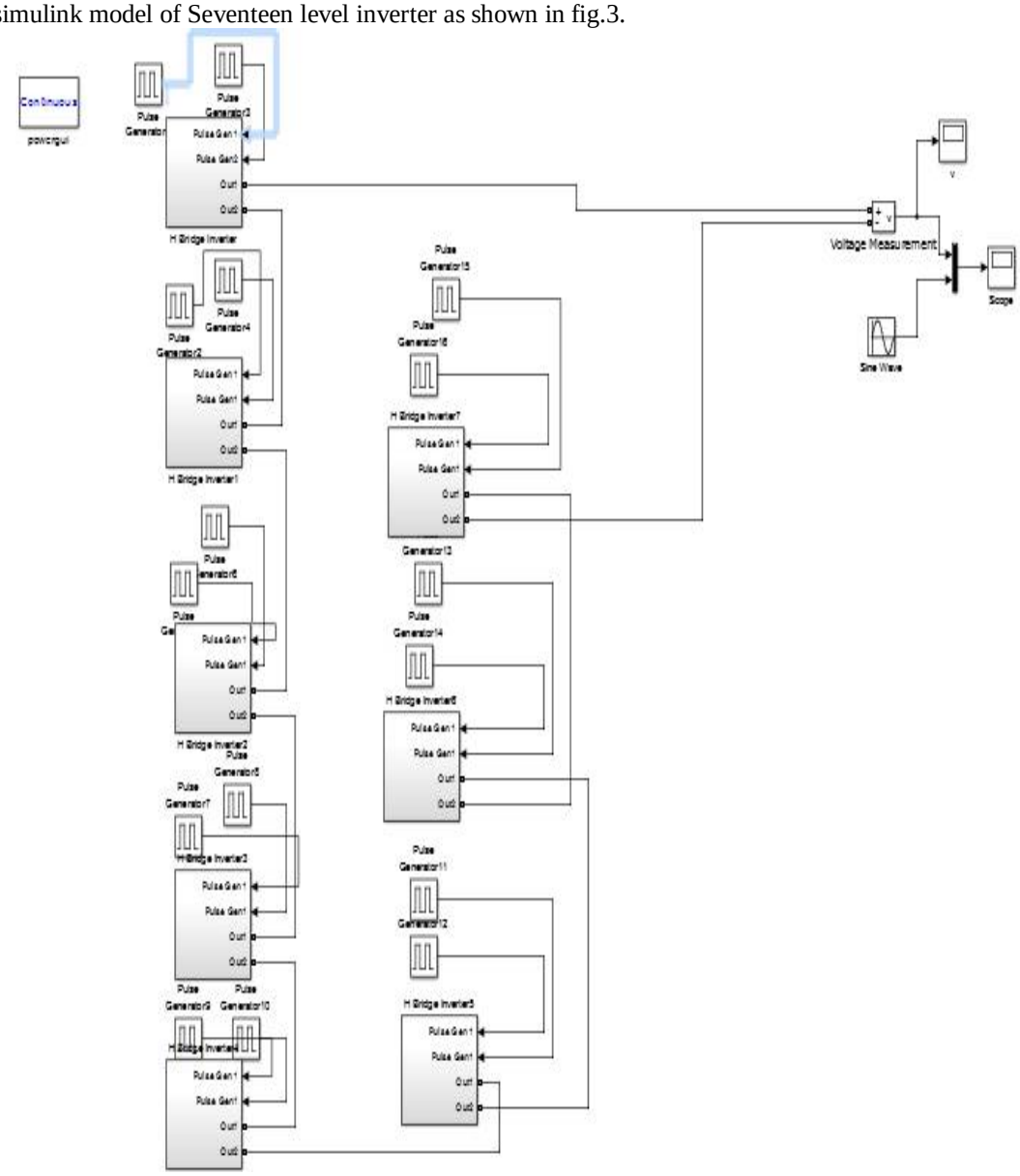

Fig.3 simulation diagram of seventeen level cascade h-bridge multilevel inverter.

The simulink design of 17 stage cascaded h-bridge multilevel inverter as proven in fig 4.The routine made up of eight subsystems, 16 beat turbines, one volts statistic, one scope and energy GUI. Each portion of dc resource is linked with an H-bridge inverter. The outcome volts of eight h-bridges is 17 stages are ($+V_{dc}$ to $8V_{dc}$, 0,$-V_{dc}$to -8_{Vdc}).

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 1, January 2018

III.RESULT

The corresponding output voltage waveform of this multilevel inverter is shown in fig.4.

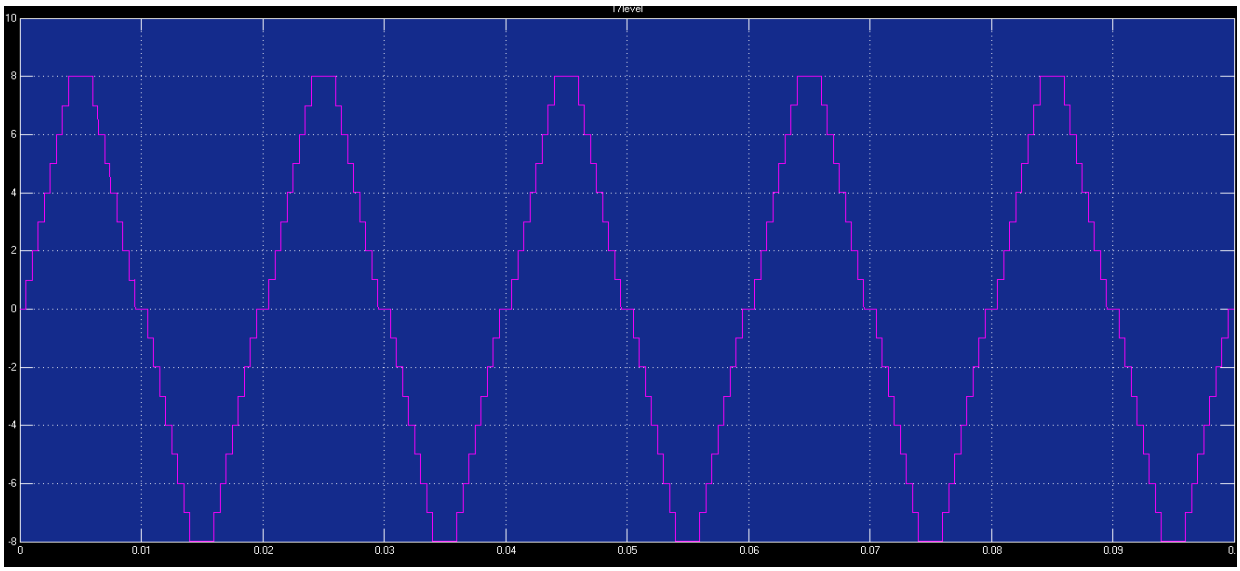

Fig. 4 output wave form of seventeen levels Cascade H-bridge multilevel inverter.

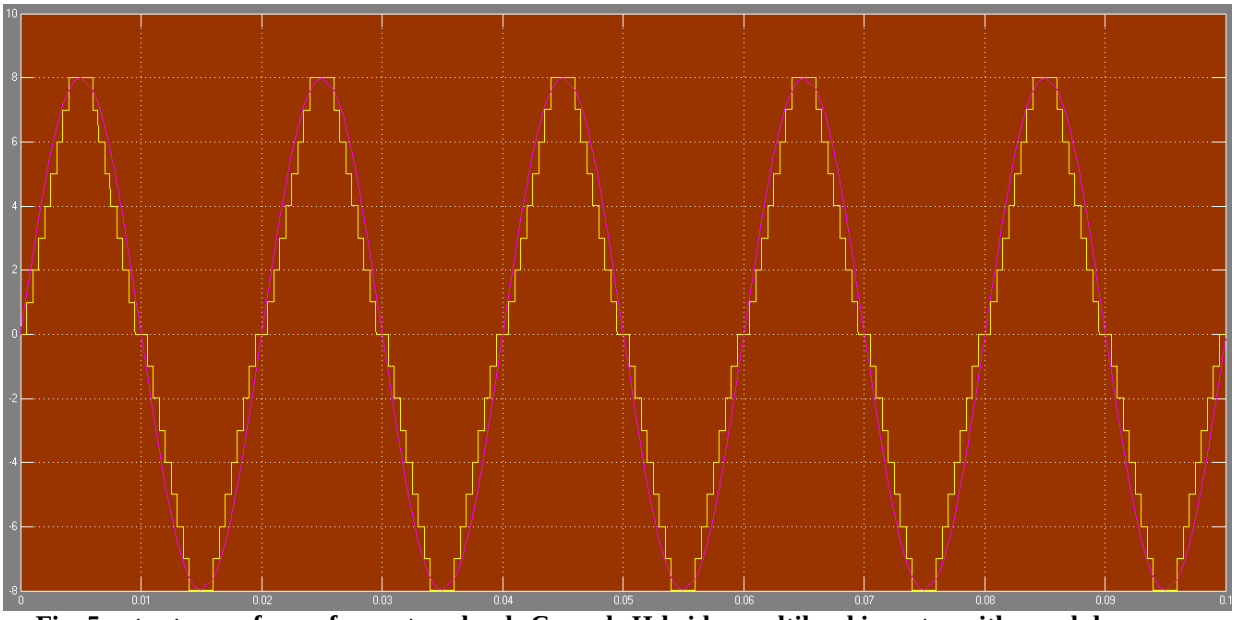

Fig. 5 output wave form of seventeen levels Cascade H-bridge multilevel inverter with equal dc source.

In 17 level inverters the beat turbines are working with different changing perspectives with simulator time frame is 0.1seconds and the causing outcome trend form as shown in above determine.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 1, January 2018

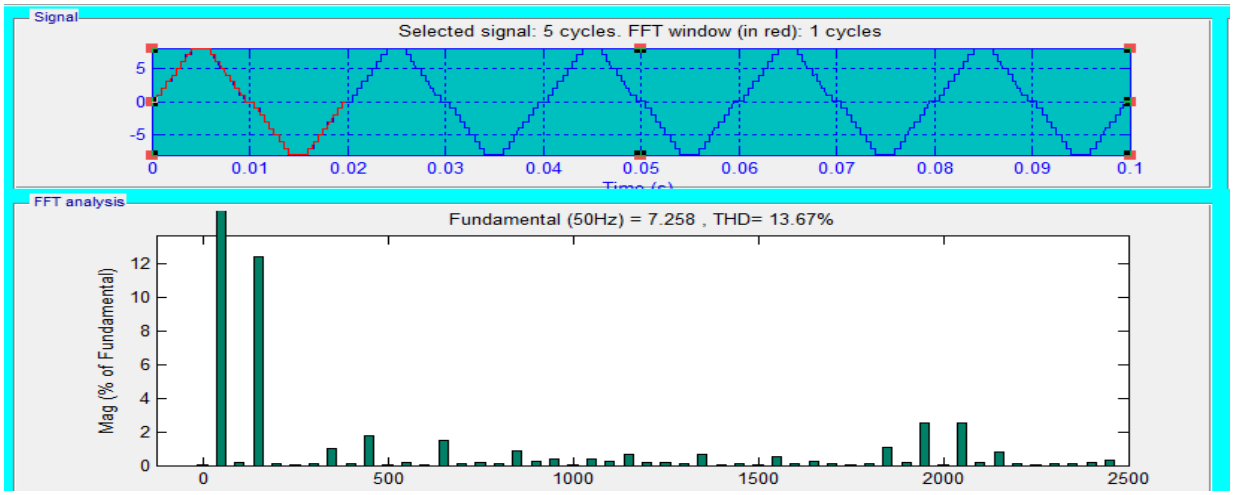

Fig. 6 FFT analysis of Seventeen level inverter.

By using FFT research the 17 stage inverter has decreasing complete harmonic disturbances with 13.67% proven in above determines.

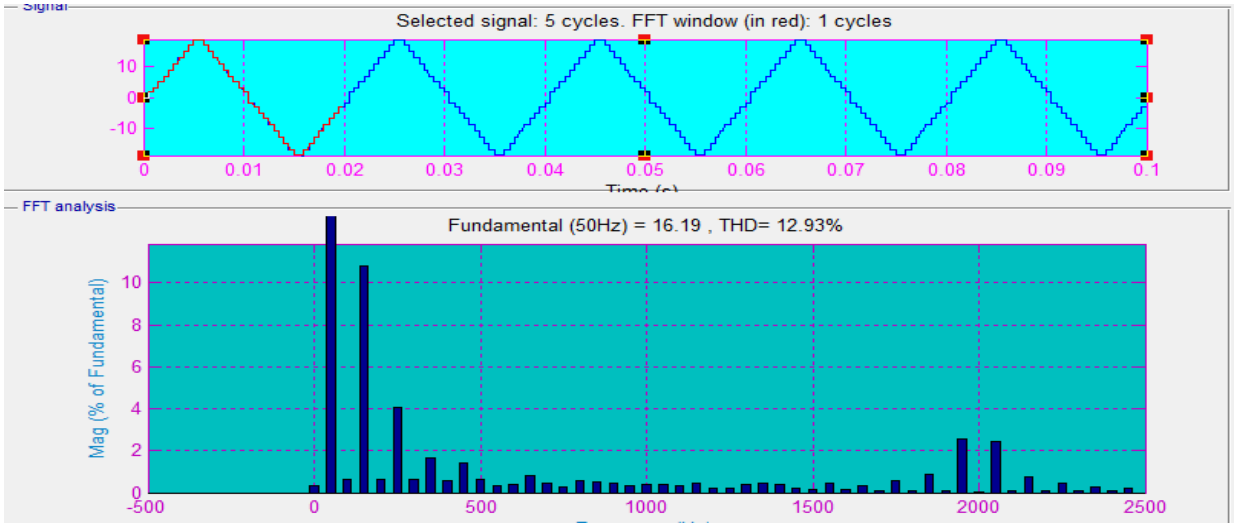

Fig. 7 FFT analysis of twenty three level inverter.

By using FFT research the 23 stage inverter has decreasing complete harmonic disturbances with 12.93 % proven in above determines.

In the same way simulator designs for 25, 27, 29 and 31 stages are simulated and the acquired answers are tabulated.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 1, January 2018

Table no.1 THD with different levels.

Sr. No.	Number of level	THD
1	9	26.59%
2	17	13.67%
3	23	12.93%
4	25	12.57%
5	27	12.34%

IV. CONCLUSION

This document includes with the various Cascaded H-link multilevel inverters with decreasing complete harmonic disturbances. Multilevel inverter is simulated by using matlab with sim energy techniques application and THD research is done by using the FFT research device in matlab application. It is eliminated that from the desk 1 the THD value of multilevel inverter is decreased by flowing h-bridge.

REFERENCES

1. Jose Rodriguez, Jih- Shenz Lai, Fang Zheng Peng,"Multi level inverters: A survey of Topologies, Controls, and applications", IEEE Transactions on Industrial Electronics, vol.49, no. 4, August 2002.
2. R.H. Baker "Bridge converter circuit", U.S. Patent 4270163 May 1981.
3.F.Z.Peng, J.S.Lai"Multi level inverter with separate DC sources" U.S. Patent 5 642 275, June 24,1997.
4.G.Mhesh Manvinna,S.Rama Reddy," Analysis and simulation of seven level inverter system", Int J engg Techsi VOL 1, PP.62-68,2010.