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Circuit Design Challenges for Nanoscale CMOS based Devices

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ABSTRACT:In recent years, subthreshold operation has gained a lot of attention due to ultra-low-power consumption in nanoscale based applications requiring low to medium performance. It has also been shown that by optimizing the device structure, power consumption of digital subthreshold logic can be further minimized while improving its performance. Therefore, subthreshold circuit design is very promising for future ultra-low-energy sensor applications as well as high-performance parallel processing. This paper deals with various device and circuit design challenges associated with the state of the art in optimal digital subthreshold circuit design and reviews device design methodologies and circuit topologies for optimal digital subthreshold operation. This paper identifies the suitable candidates for subthreshold operation at device and circuit levels for optimal subthreshold circuit design and provides an effective roadmap for digital designers interested to work with nanoscale applications.

I.INTRODUCTION

Maximum attention has been given to the high-performance microprocessors in digital VLSI system design space. However, the demand for power sensitive designs has grown significantly in recent years. This tremendous demand has mainly been due to the fast growth of battery-operated portable applications. Further, due to the aggressive scaling of transistor sizes for high-performance applications, not only does subthreshold leakage current increase exponentially, but also gate leakage and reverse-biased source-substrate and drain-substrate junction’s band-to-band tunneling (BTBT) currents increase significantly. The tunneling currents are detrimental to the functionality of the devices. Well-known methods of low power design (such as voltage scaling, switching activity reduction, architectural techniques of pipelining and parallelism, Computer-Aided Design (CAD) techniques of device sizing, interconnect, and logic optimization) may not be sufficient in many applications such as portable computing gadgets, medical electronics, where ultra-low power consumption with medium frequency of operation (tens to hundreds of MHz) is the primary requirement. To cope with this, several novel design techniques have been proposed. Energy recovery or adiabatic techniques promises to reduce power in computation by orders of magnitude. But it involves use of high-quality inductors which makes integration difficult. More recently, design of digital subthreshold logic was investigated with transistors operated in the subthreshold region (supply voltage (*V*dd) less than the threshold voltage (*V*th)) of the transistor). In such a technique, the subthreshold leakage current of the device is used for necessary computation. This results in high transconductance gain of the devices (thereby providing near ideal voltage transfer characteristics of the logic gates) and reduced gate input capacitance. Its impact on system design is an exponential reduction of power at the cost of reduced performance. Digital computation using subthreshold leakage current has gained a wide interest in recent years to achieve ultralow-power consumptions in portable computing devices. Both logic and memory circuits have been extensively studied with design consideration at various levels of abstraction. It has been shown that using subthreshold operation, significant power savings can be achieved in applications requiring low to medium (ten to hundreds of megahertz) frequency of operation [1]. This paper is organized as follows. Application areas in Section II. Various challenging issues confronting the current and future robust subthreshold circuit design are reviewed in Section III. Section IV presents various device level optimization methodologies identified for optimal subthreshold operation. Section V shows various circuit styles other than static CMOS suitable for robust subthreshold operation. Future work of sub-threshold, i.e. Near-threshold computing is discussed in section VI. Finally conclusions are drawn in Section VII.

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II. APPLICATION AREAS

Subthreshold digital circuits will be suitable only for specific applications which do not need high performance, but require extremely low power consumptions. This type of applications include medical equipments [2-4] such as sensors [5-7], nanowire detectors[8], aptamers [9], hearing aids and pace- maker [10, 11], and self-powered devices [1]. Subthreshold circuits can also be applied to applications with bursty characteristics in which the circuits remain idle for an extended period of time. The original active time period in strong inversion region is being extended throughout the idle time period running in subthreshold region. The same number of operations is performed in both cases, but with much lower power consumption in the subthreshold operation.

III. CHALLENING ISSUES IN SUB-THRESHOLD DESIGN

Various device and circuit challenges have been identified which need to be addressed for the advancement of the subthreshold design. This section provides an interesting insight and challenges for designers interested to work with energy-constrained applications, particularly taking advantage of subthreshold circuits.

- *Exploring Logic Families Optimal for Subthreshold Circuit Design.*

The low V_{dd} results in a reduced I_{ON}/I_{OFF} ratio that can reduce robustness. Static CMOS gates continue to function in subthreshold, but because of enhanced problem of short-channel effects due to variations at nano scale [7], logic families other than CMOSmay offer greater resiliency to certain variation sources such as voltage or process. Therefore, design of robust subthreshold logic circuits exploring logic families other than static CMOS is another open area for exploration [12].

- *Developing industrial subthreshold benchmark circuits*

Since there are no industrial subthreshold devices to compare the results with those of any optimized subthreshold devices [1], there is a need to build benchmark circuits with the subthreshold devices to compare issues such as variation immunity, power, and performance with respect to constructed subthreshold circuits with standard devices.

- *Advancement in CAD Tools*

Another significant issue for subthreshold operation is system verification. Using SPICE for verifying large systems rapidly becomes infeasible when the number of process corners, temperature corners, and voltage supply values increases. Hspice is too slow to run larger circuits and Nanosim can simulate large netlists in reasonable time, but will not correctly model the devices for supply voltages below 1V. Therefore, need for either modifications of current simulators or a new subthreshold circuit simulator to verify large systems running at such ultra-low voltages and to estimate the power dissipation of circuits. Advances in CAD tools to account for this problem become necessary. These tools must also address statistical distributions of delay and power introduced by local variations

- *Architectures for Optimal Subthreshold Circuits*

There is much future work opportunities in the area of architectures for subthreshold circuits. One area is the use of pipelining and massively parallel architectures that increase the activity factor of a circuit and requires minimum supply voltage operation. There is also great need for developing complete subthreshold standard cell library which will provide further opportunities to optimize for minimal energy dissipation.

V. DEVICE-LEVEL OPTIMIZATION METHODOLOGIES FOR SUB-THRESHOLD OPERATION

Standard transistors can be operated in the subthreshold region to implement subthreshold logic. Standard transistors are called “super-threshold transistors” that are design for ultrahigh-performance. After investigation, it has been concluded that standard transistors are not suitable for subthreshold operation. Hence some device optimization methodologies have been suggested, for subthreshold operation.

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- *CMOS Technology for Subthreshold Operation*

CMOS technology can be modified in the following ways for subthreshold operation.

1) Changing Channel Doping Profile for Subthreshold Operation

In bulk CMOS design halo and retrograde doping are used to suppress the short-channel effects. The main functions of halo doping and retrograde wells are to reduce drain-induced barrier lowering (DIBL), prevent body punch through, and control the threshold voltage of the device independent of its subthreshold slope. However, in subthreshold operation, the overall supply bias is small (in the order of 0.15V–0.3V).Consequently, the effects of DIBL and body punch through are also negligible.

Hence, we need not include this doping regions in our device. This results in the following conclusions:

- A simplified process technology in terms of process steps and cost.
- A reduction in the junction capacitances.
- Reduction in the capacitance of the bottom junction.
- Reduction in substrate noise effects and parasitic latch-up.

2) Oxide Thickness Optimization for Subthreshold Operation

In regular CMOS a minimum Tox is used for good subthreshold slope. However, minimum possible oxide thickness may not be suitable for subthreshold operation because it does not result in minimum energy consumption.

In the subthreshold operation, intrinsic gate capacitance is dominated by depletion capacitance but the parasitic capacitances like overlap and fringe capacitances will eventually dominate if the oxide is too thin. In the subthreshold operation, the effective gate capacitance *C*g of a transistor is dominated by the intrinsic depletion and the parasitic (both overlap and fringe) capacitances that strongly depend on *T*ox. So oxide thickness should be optimized considering both the transistor effective capacitance and the subthreshold slope to achieve lowest power consumption.

3) Utilizing Reverse Short-Channel Effects for Subthreshold Operation

The side effects that appear in regular MCOS can be used for our benefit in subthreshold operation. The RSCE are used to improve drive current, capacitance, process variation, subthreshold swing, and improved energy/dissipation.

SCE (or *V*th roll-off) is a phenomenon in short-channel devices where *V*th decreases as the channel length is reduced. Non-uniform HALO [9] doping is used to reduce this problem by making the depletion widths narrow and hence reducing the DIBL effect. As a byproduct of HALO, a short channel device shows RSCE behavior where the *V*th decreases as the channel length is increased. In subthreshold circuits, the SCE mechanism is not as strong as in super-threshold circuits because the drain-to-source voltage is very small. On the other hand, RSCE is still significant enough to affect the subthreshold performance. Moreover, current becomes an exponential function of *V*th in subthreshold region, which makes it possible to use longer channel-length devices that utilize RSCE for improving drive current.

4) New Device Sizing Based on Subthreshold Logical Effort

For regular CMOS, the optimal ratio of PMOS width (*Wp*) to NMOS width (*Wn*) for achieving equivalent current drivability is approximately 2.5:1 due to the mobility difference between the carriers between the PMOS and NMOS devices. But for subthreshold operation this ratio reduces to 1.5:1 which gives equal delays for the rise and fall transitions at *V*dd = 0.2V. This is because the drive-current in subthreshold designs is an exponential function of the terminal voltages

- *DGSOI Technology with Co-design Methodology for Optimal Subthreshold Operation*

It has been demonstrated that double gate MOSFETs are better suited for subthreshold operation than regular MOSFETs. This is because the DG-SOI has no intrinsic capacitance in the subthreshold region. Double Gate MOS

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(DGMOS) transistors have near ideal subthreshold slope and negligible junction capacitance which makes them suitable for subthreshold operation. The thin and fully depleted silicon body between the two gates, have an excellent gate control over the channel.
Also the un-doped thin silicon body provides negligible source/drain p-n junction capacitance, which greatly improves the circuit performance. It can be noted that due to near ideal subthreshold slope, the DG-SOI devices have higher ON-current compared to the bulk devices. DG-SOI inverter has almost one order of magnitude lower PDP than the corresponding bulk device. This is due to the fact that the intrinsic capacitance of DG-SOI is negligibly small and hence the switching energy is extremely low.

- *Carbon Nanotube (CNF*ETs) Technology for Subthreshold *Operation*

Carbon nano tubes (CNTs) and molecular transistors are a very attractive alternative to nanoscale transistors[13]. CNTs are sheets of graphite rolled in the shape of a tube. Absence of scattering in the channel is the characteristic of ballistic devices which make them ultrahigh speed and apt for high-performance circuit design.

V. LOGIC FAMILIES FOR SUB-THRESHOLD OPERATION

In this section, we will present the scope of various logic families other than static CMOS for designing optimal subthreshold logic circuits. The following logic families are suitable for designing more robust and energy efficient subthreshold circuits with some tradeoff.

Subthreshold CMOS Logic

Sub-threshold CMOS (Sub-CMOS) logic [14, 15] is the regular CMOS logic operated in the subthreshold region. The voltage transfer characteristics (VTC) of the inverter gate running in subthreshold mode is closer to ideal compared to the VTC in normal strong inversion region. The improvement is due to

- *Increase in the circuit gain, gm.*
- *Better noise margins.*
- *More freedom in sizing.*
- *Sensitivity to Power Supply Variation with decreasing power supply value for subthreshold CMOS.*

Subthreshold Pseudo-NMOS Logic

- In subthreshold region, Pseudo-NMOS logic is more robust than Pseudo- NMOS logic in strong-inversion,
- voltage levels swing rail-to-rail due to large gain in subthreshold region
- does not suffer from low logic level degradation problem
- Operates faster than CMOS[8] consuming less area.

Two main disadvantages of Pseudo-NMOS in strong inversion compared to CMOS are higher power consumption and less robustness, which are eliminated in subthreshold region due to ideal device characteristics. In summary, Pseudo nMOS for subthreshold has better PDP and comparable robustness to static CMOS.

VT Sub-CMOS Logic

VT-Sub-CMOS logic [2] is a sub-CMOS logic with an additional stabilization scheme (Fig. 1). The stabilization circuit monitors any change in the transistor current due to temperature and process variations and provides an appropriate bias to the substrate. Any increase of the current above certain prespecified threshold value is thus reduced by an appropriate bias to the substrate. Both logic and stabilization circuits of VT-sub-CMOS work in the subthreshold region i.e., with a supply voltage less than the threshold voltage of the transistor (Vdd<Vth).

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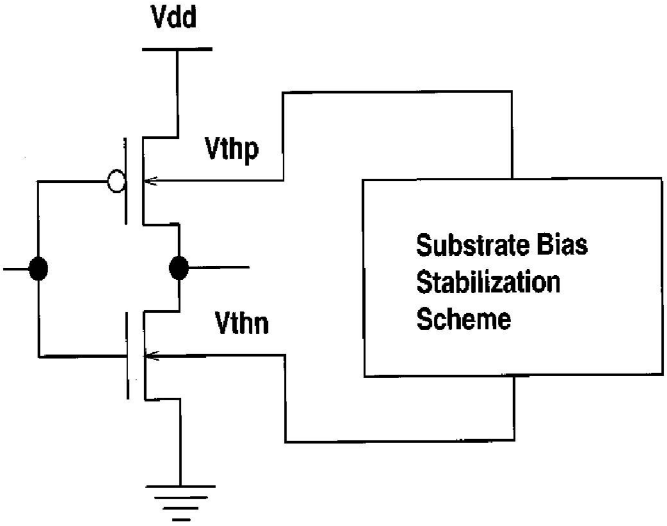

Fig. 1. VT-Sub-CMOS logic

This figure has been taken from the paper titled "Robust subthreshold logic for ultra-low power operation" written by Soeleman, H.; Roy, K. and Paul, B.C.

Sub-DTMOS logic

Sub-DTMOS logic provides an alternative way to achieve the same stability with direct substrate biasing without using additional control circuitry as in the case of VT-sub-CMOS logic. Sub-DTMOS logic uses transistors whose gates are tied to their substrates (Fig. 2). As the substrate voltage in sub-DTMOS logic changes with the gate input voltage, the threshold voltage is dynamically changed.

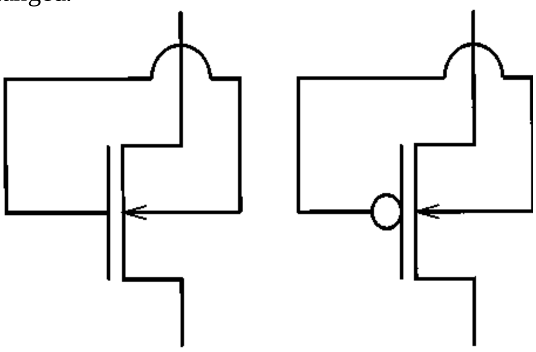

Fig. 2. DT-NMOS (left) and DT-PMOS (right)

This figure has been taken from the paper titled "Robust subthreshold logic for ultra-low power operation" written by Soeleman, H.; Roy, K. and Paul, B.C.

In the off-state, i.e., V_{in}=0 (V_{in}=V_{dd}) for NMOS (PMOS), the characteristics of DTMOS transistor is exactly the same as regular MOS transistor. Both have the same properties, such as the same off-current, subthreshold slope, and threshold voltage. In the on-state, however, the substrate-source voltage (V_{bs}) is forward- biased and thus reduces the threshold voltage of DTMOS transistor. The reduced threshold voltage is due to the reduction of body charge. The reduction of body charge leads to another advantage, namely higher carrier mobility because the reduced body charge

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causes a lower effective normal field. The reduced threshold voltage, lower normal effective electric field, and higher mobility results in higher on-current drive in DTMOS [16] than that of a regular MOS transistor.

VI. NEARTHRESHOLD COMPUTING

Near-threshold computing (NTC) can be considered as future work for sub-threshold computing. As we all know Moore's law has failed to ensure proportionate increases in performance or energy efficiency with decreasing feature size and integration capacity. From the 65 nm technology, device scaling no longer delivers the energy gains that supported the semiconductor industry. The supply voltage and dynamic energy efficiency improvements have stagnated, while leakage currents continue to increase. Heat removal limits have been placing a further restriction. The near-threshold strategy provides 10X or higher energy efficiency improvements at constant performance through widespread application of near-threshold computing (NTC), where devices are operated at or near their threshold voltage V_{th}. This a relatively new technology and there is a lot of ongoing research in this field.

VII.CONCLUSION

As supply voltage continues to scale with each new generation of CMOS technology, Sub-threshold design is an inevitable choice in the semi-conductor road map for achieving ultra-low power consumption. Device optimization is a must for optimal subthreshold operation to further reduce power and enhance performance. Comparative studies shows that double gate SOI devices and CNFETs are better candidates to work for subthreshold operation than Bulk CMOS devices. At circuit level, Sub-Pseudo-NMOS, Sub-DTPT and Sub-domino logics can be considered for robust subthreshold operation due to their improved performance and better stability for PVT variations with reduced or comparable energy/switching to that of conventional static CMOS logic. Device/Circuit Codesign methodology can further enhance subthreshold operation in terms of performance and robustness.

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