ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 6, Issue 11, November 2017

Designing of MOS Transistors in Two Stage OTA with Miller Compensation

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ABSTRACT:In this paper Designing of MOS Transistors in two stage OTA has been done and simulated in 180nm technology using cadence virtuoso environment. A comparison has been made between simulated results and the given specifications. A mathematical analysis also has been done to calculate the **W/L** ratios for all the MOS Transistors.The simulation results show that the designed two stage OTA achieves the DC gain of 70.88,GBW of 36.10MHz, $f_{3.dB}$ of 11.57KHz ,CMRR 77.80 and Slew Rate of 21.35V/μswhen operated using a 1.8 volt power supply with a total power consumption of 273.4**μW**.

KEYWORDS: Operational transconductance amplifier (OTA), Miller compensation,180nm Technology.

I.INTRODUCTION

There are basically three main reasons for the necessity of low voltage –low power design of integrated circuits.First one is related to the continuing down scaling of processes.As the channel length of the MOS transistor is decreased in the sub-micron region and the gate oxide thickness becomes nanometers thick,the supply voltage has to be reduced in order to ensure the device function and reliability.Now a days the supply voltage has been reduced due their smaller device sizes.The second reason comes from the increasing density of the components of chip.A chip can dissipate a limited amount of power per unit of area.Since the increasing density allows more components per unit area,The power dissipation is also increased due to their increased density.This power dissipation has to be lowered to prevent overheating of the silicon chip.The third reason is related to the portability of battery operated equipment.In order to achieve the long period operation the power dissipation should be low and it is possible with low supply voltage.

Op-amp works well for low frequency applications such as audio and video systems,Op-amp has limitations in Bandwidth and slew rate.For higher frequencies,Op-amp design becomes difficult due to their frequency limit.For higher frequencies,OTA is deemed to be promising to replace Op-amp as the building blocks.OTA is a basic building block of analog circuits.It is an integral part of many analog and mixed mode signal systems.OTA is a current mode circuit and a versatile amplifier that converts applied input voltage to linearly proportional output current with transconductance g_m.They provide better performance at higher frequencies because of current mode operation and they do not require any resistors for their internal circuitry.

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II. THEORY OF TWO STAGE OTA

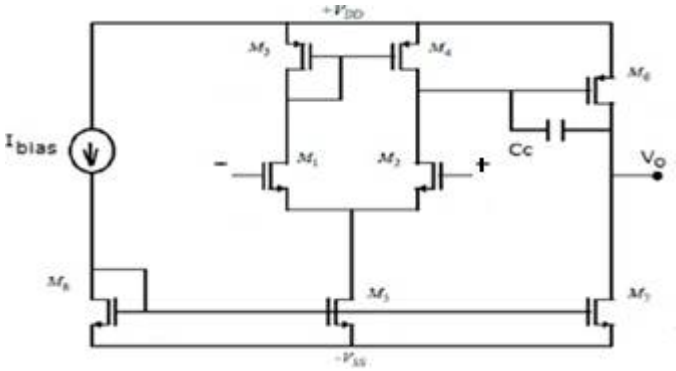

Fig. 1. Schematic Diagram of two stage OTA

As the name itself describes that this OTA(shown in figure 1) consists of two stage the first one is differential amplifier in which NMOS M_1&M_2 acting as a input differential pair and the PMOS M_3&M_4 forming a current mirror circuit acting as a load.The main reason behind this current mirror load instaed of resistor is to reduce chip area.We can also use diode connected load but it is having a limitation of limited output voltage swing.Second one is the common source stage which is acting as a gain stage.The need of this common source stage arises because the gain obtained with the differential amplifier is not high enough.MOS M_6&M_7 acting as a common source stage.

The biasing operation is achieved by current mirror containing transistor M_5&M_8 along with the reference current source.Transistor M_5&M_8 sink a certain amout of current based on their gate voltages. Capacitor C_c is acting as a Compensation capacitor .From small signal analysis we can find that it is a two pole system and the phase margin reduces to zero because of two poles.To obtain proper phase margin and good stability we should separate poles from each other so that dominant pole moves to the lower frequency and the non dominant pole moves to the higher frequency.The movement of poles becomes easier with miller effect because with the help of miller effect a small capacitance can be converted in to equivalent high capacitance value and in this circuit this compensastion capacitor is also known as the miller capacitor.

III.DESIGN SPECIFICATIONS OF TWO STAGE OTA

The design specifications of two stage miller OTA are given as follow:

Table 1.Design Specifications of two stage OTA

DC gain	60 dB
Gain Bandwidth product	30MHz
Phase Margin	≥ 60°
Slew Rate	20 V/μs
Maximum input common mode range	1.6
Minimum input common mode range	0.8
C_l	2pF
Power dissipation	≤ 300μW
V_{DD}	1.8 volt
Process	0.18μm

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IV.CALCULATION FOR SPECIFICATIONS

L=500 nm, $C_c \geq 0.22C_l$&C_l= 2pF (given) $\Rightarrow C_c \geq 0.22\times 2pF$,
For designing we are using C_c = 800 fF
From slew ratw we find I_5 and $I_5 = I_0 \Rightarrow I_5 = S.R\times C_c = 20V/\mu sec \times 800\ fF = 16\mu A$
For designing we are taking I_5= 20µA
$g_{m1} = GBW\times C_c \times 2\pi \Rightarrow g_{m1} = 30MHz\times 800f \times 2\pi 150.79\mu = 160\ \mu A/V$

$$\frac{W}{L} = \frac{g_m{}^2}{2\, I_D \mu_n C_{ox}}$$

For M_1 and M_2

$$2I_D = I_5 \& \left(\frac{W}{L}\right)_1 = \frac{g_{m1}{}^2}{\mu_n C_{ox} I_5}$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1}{}^2}{\mu_n C_{ox} I_5} = \frac{160^2}{300\times 20} = 4.266 \text{ \& Use } \left(\frac{W}{L}\right)_{1,2} = 5$$

For M_1 MOS in saturation

$$V_{in} < V_{D1} + V_{t1} \Rightarrow V_{inmax} = V_{D1} + V_{t1} \Rightarrow V_{D1} = V_{DD} - V_{SG3}$$

$$I_3 = \frac{\beta}{2}(V_{gs} - V_t)^2 \Rightarrow V_{GS} = \sqrt{\frac{2I_3}{\beta_p}} + |V_{t3}|$$

$$V_{D1} = V_{DD} - \left[\sqrt{\frac{2I_3}{\beta_p}} + |V_{t3}|\right]$$

$V_{inmax} \leq V_{D1} + V_{t1}$
$ICMR+ \leq V_{D1min} + V_{t1}$

$$V_{D1} = V_{DD} - \left[\sqrt{\frac{2I_3}{\beta_p}} + |V_{t3}|\right]$$

$$ICMR+ \leq \left[V_{DD} - \left[\sqrt{\frac{2I_3}{\beta_p}} + |V_{t3}|\right]\right]_{min} + V_{tmin}$$

$$ICMR+ \leq V_{DD} - \sqrt{\frac{2I_3}{\beta_3}} - |V_{t3}|_{max} + V_{tmin}$$

We can find through simulation:
$\mu_p C_{ox} = 60\ \mu A/V^2$, $\mu_n C_{ox} = 300\ \mu A/V^2$

$$\frac{2I_3}{\beta_3} = (V_{DD} - ICMR_{max} - |V_{t3}|_{max} + V_{t1min})^2$$

$$\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3} = (V_{DD} - ICMR_{max} - |V_{t3}|_{max} + V_{t1min})^2$$

$$\left(\frac{W}{L}\right)_3 = \frac{2I_{D3}}{\mu_p C_{ox}(V_{DD} - ICMR_{max} - |V_{t3}|_{max} + V_{t1min})^2}$$

$I_{D3} = \frac{I_{D5}}{2} = 10\ \mu A$
$ICMR+ = 1.6\ V, V_{t3max} = 0.51V$ &$V_{t1min} = 0.47V$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2\times 10\,\mu}{60\mu[1.8-1.6-0.51+0.47]^2} = 13.02$$

Use $\left(\frac{W}{L}\right)_{3,4} = 14$

For M_5 to be in saturation
$V_{D5} > V_G - V_t$,When V_{in} decreases M_5 will enter to triode region.Assume that required V_D is V_{Dsat}

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Vol. 6, Issue 11, November 2017

$V_{inmin} \geq V_{Gs1} + V_{Dsat5}$

$ICMR(min) \geq V_{Gs1max} + V_{Dsat}$

$ICMR \geq \left[\sqrt{\frac{2I_{D1}}{\beta_1}} + V_{t1}\right]_{max} + V_{Dsat}$

$ICMR \geq \sqrt{\frac{2I_{D1}}{\beta_1}} + V_{t1max} + V_{Dsat}$

$V_{Dsat} \geq ICMR(-) - \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{t1max}$

$V_{Dsat} \geq 0.8 - \sqrt{\frac{2\times10\mu}{300\mu\times5}} - V_{t1max}$

$V_{Dsat} = 0.8 - 0.1154 - 0.59 = 94.6$ Mv

Here is a problem we have M_1&M_5 .Here we have small voltage across M_5 i.e 94.6 mV .Generally we have voltage across M_1 is 100 mV .If V_{DS} across M_5 is less we have to make big MOSFET to ensure MOS in saturation.If we make M_5 very big then corresponding MOS M_7 is also very big reduces gain.Generally we prefer V_{Dsat} higher than 100mV.In our case it is 94.6 mV only.In last equation of V_{Dsat} we can not change V_{t1max} and ICMR also (given specifications) only thing we can change only β_1 value $\left(\beta_1 = \mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}\right)$ if we increase $\left(\frac{W}{L}\right)_1$ and voltage drop across M_1 less and we will get more voltage across M_5 .

Generally $\left(\frac{W}{L}\right)_{M1} = 5$, Now $\left(\frac{W}{L}\right)_{M1} = 6$

Now $V_{Dsat} = 0.8 - 0.1054 - 0.59 = 105$mV

It is greater than 100 mV and it is good value to proceed.

$$I_{D5} = \frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_5}{2}(V_{Dsat})^2$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D5}}{(V_{Dsat})^2\mu_n C_{ox}} = \frac{2\times20}{300\times(105mV)^2}$$

$\left(\frac{W}{L}\right)_5 = 12.09 \approx 12$, Now we have modified the value of $\left(\frac{W}{L}\right)_{1,2} = 6$

Now let us go for the of M_6 . M_6 is closely related to M_3&M_4

For 60° PM

$gm_6 \geq 10\, gm_1 \geq 10\times160\ \mu A/V$

$gm_6 \geq 1600\ \mu A/V$

If M_3&M_4 are mirrored then V_{GS} of $M_3 = V_{GS}$ of M_4 and also drain voltage is same.

$V_{DS,M3} = V_{DS,M4} \approx V_{DS,M6}$(approx)

Current flowing through M_3 , M_4&M_6 will be proportional to $\frac{W}{L}$. Ratio of that MOSFET i.e according to their width and all other conditions are same.All MOS connected to V_{DD}&their V_t are also same.

$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = \frac{I_6}{I_4}$, Similarly we can write $\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = \frac{gm_6}{gn_4}$

We know $\left(\frac{W}{L}\right)_4 = 14$

$g_m = \sqrt{\mu_p C_{ox}\frac{W}{L}\,2\,I_D}$

$gm_4 = \sqrt{60\times14\times2\times10} = 129.61\ \mu A/V$

$\left(\frac{W}{L}\right)_6 = \frac{gm_6}{gm_4}\times\left(\frac{W}{L}\right)_4 = \frac{1600}{129.61}\times14$

$\left(\frac{W}{L}\right)_6 = 172.82 \approx 173$ or 174 also

Now we have to find current I_6 and $\left(\frac{W}{L}\right)_{M7}$.

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$$\frac{I_6}{I_4} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = \frac{174}{14} \times 10\ \mu A$$

$I_6 = 124.28\ \mu A \approx 125\ \mu A$

$$\frac{I_7}{I_5} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5}$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5} \times \left(\frac{W}{L}\right)_5 = \frac{125}{20} \times 12 = 75$$

Table 2.Calculated Parameters

	M1,M2	M3,M4	M5	M6	M7
W	3µ	7µ	6µ	87µ	37.5µ
L	500n	500n	500n	500n	500n

$I_5 = 20\ \mu A$ and Cc = 800 fF

V. SIMULATION RESULTS

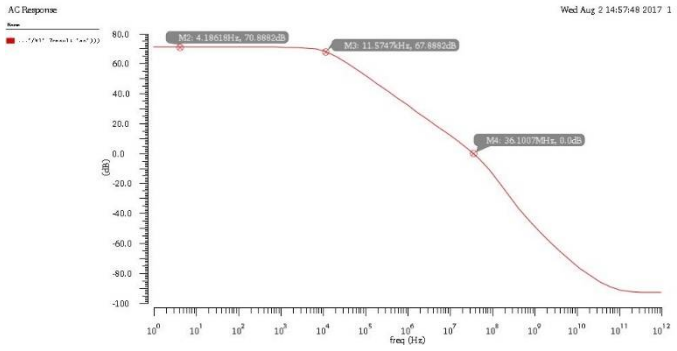

Fig.2.Gain Plot

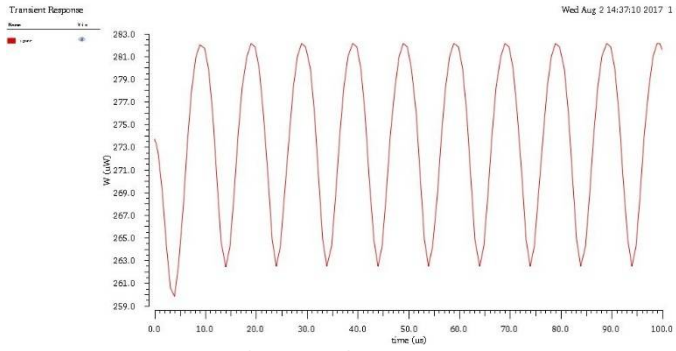

Fig.3.Power Consumption

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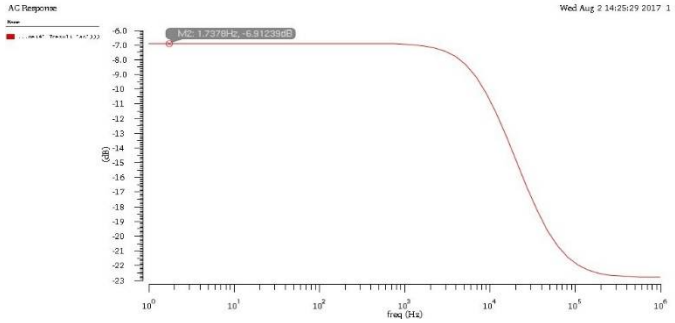

Fig. 4.Common Mode Gain

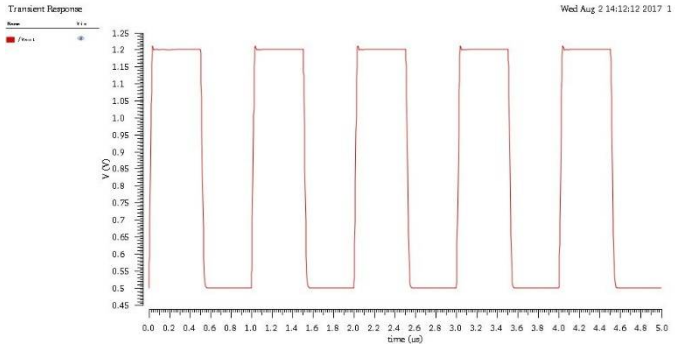

Fig.5.Slew Rate

Table 3. Simulation Results of Two Stage OTA

Gain(dB)	70.88
GBW(MHz)	36.10
f_{3dB}(KHz)	11.57
Power(µW)	273.4
Slew Rate($V/\mu sec$)	21.35
CMRR	77.80

VI.CONCLUSION

In this paper Two Stage OTA is presented. Simulation Results satisfy the design specifications.The designed Two Stage OTA is suitable for High Gain ,High CMRR and GBW. OTA can be used in Filters,Oscillators and Voltage amplifiers etc.

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