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High Gain SEPIC Rectification Using Switched Capacitor Module

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ABSTRACT: A single phase rectifier, based on SEPIC converter integrated with switched capacitor cells is proposed to achieve double gain at the output voltage, high power factor by a bridgeless converter. The structure has the absence of the diode bridge at the input port reducing the number of components and conduction losses. A comparison with the classic Sepic shows that the proposed converter might either provide reduced voltage stress on the semiconductors for doubled output voltage or to the same output voltage with same voltage stress. By adding the switched capacitor cells, achieve a very high gain in the output voltage with reduced power devices and achieves high power factor in the input. The modified switched capacitor cell, which does not change the operation of the storage capacitor structure. Therefore the proposed structure can be applied in DCM SEPIC rectifiers improving the converter static gain, making suitable for higher voltage applications.

KEYWORDS: AC-DC converters, SEPIC converters, single stage PFC

I.INTRODUCTION

The implementation single phase PWM (pulse width modulated) rectifiers at large scale industries in applications with different power, voltage and current levels. The available single phase PWM rectifiers are based on classic dc-dc converters, as boost, buck-boost, cuk, zeta and Sepic, and an input current in phase with the input voltage without a current control, can be obtained when they operate in dcm(discontinuous conduction mode).

In DCM mode, the conventional Sepic can produce continuous current. As the power level increases, the high conduction loss caused by the high forward voltage drop of the diode begins to degrade the overall efficiency, and the heat generated within the bridge rectifier may destroy the individual diodes. Hence it is not applicable for high output voltage applications.

In the other hand, converters based on switched capacitors have the feature of multiplying or dividing voltage without increasing the stress on the components of the circuit, thus the integration of switched capacitor cell to basic converters can result in new structures that add this feature.

In DCM mode, the Sepic based rectifier has the characteristics of emulating resistor. Thus the input currents naturally follow their respective supply voltages. Also the system has the advantage of simplicity of its control system, since current sensors and the implementation of control loop for the input currents are not required.

Based on the Sepic rectifier approached in[ix], Sepic dc-dc converter in [xi], switched capacitor cell in [xii], hybrid rectifiers in [xiv] and on the studies of [iii]-[viii], [x], [xiii] this paper proposes the analysis and experimental verification of a novel hybrid single phase rectifier, in which the switched capacitor cell is modified to work on the dcm Sepic. The novel structure provides reduced voltage stress on the semiconductors to the same output voltage level, or it supplies double the gain in the output voltage with the same output voltage stress across the semiconductors, when compared to the topology approached in [ix]. Besides, it maintains the characteristics of Sepic rectifier operating in dcm.

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II. OPERATION OF THE PROPOSED CONVERTER AND CONVENTIONAL SYSTEM

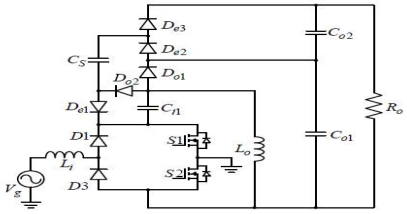

Fig: 1 Bridgeless Structure Of The Conventional System

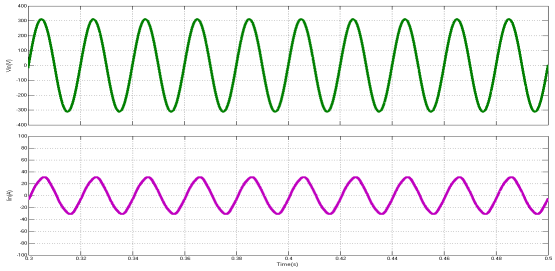

Fig:1.2 Input Voltage And Current Waveforms Conventional Method

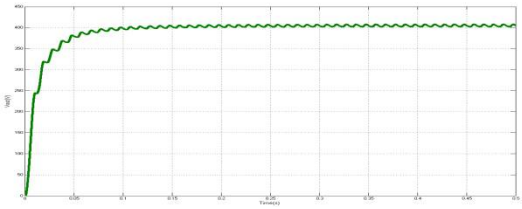

Fig:1.3 Output Voltage Of Conventional Method

III. PROPOSED RECTIFIER STRUCTURE

In the proposed topology of the single phase of the single phase bridgeless Sepic rectifier integrated with a voltage multiplier is shown in the figure. The bridgeless rectifier structure is composed of the following components: Li1, D1, D3, S1, S2, Cil1, Do1, lo1 and Co1. the absence of an input diode bridge reduces the number of components and only one diode and one switch is present in the flowing current path, during each switching period. The bridges use the same gate signal.

The proposed topology of the single phase sepic rectifier with a voltage multiplier stage, which is based on the switched capacitor cell, is shown. The multiplier stage is built with Cs, Co2, De1, De2, De3, Do2. At the DCM sepic rectifier stage, the capacitor Cil1 has to reproduce the harmonics of the rectified input voltage [viii]. The proposed two diodes (De1 and De2) is used to divert the charge and uncharged of the switched capacitor Cs and Cil1.therefore the new switched capacitor cell maintains the voltage characteristics in Cil1 similar to the classic sepic rectifier. Consequently, the proposed structure ensures an input current with lower distortion, multiplies the output voltage and preserves the voltage across semiconductors.

IV. OPERATIONAL STAGES

Mode I:

During stage 1 Δt1 (initial time period)in fig 1.1, the switches S1 and S2 are turned on and thus the diodes De1 and De2 are forward biased, while the diodes De3 and Do1 and Do2 are reversed biased. The current passing through the inductor Li and Lo increases and their values are given by the relation Vg/Li and Vg/Lo respectively. The capacitor

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Cs is charged by the capacitor Co1, Cs1 is charged by the capacitor Co2 (they are parallel connected) and load Ro is fed by the capacitor Co1, Co2 and Co3.

Mode II:

During the stage 2 Δt2 (second time period) in fig 1.2, the switches S1 and S2 are turned off, hence the diodes De3, Do1 and Do2 are forward biased and the diodes De1 and De2 are blocked. The previously energy stored in capacitor Cs and Cs1 and in the inductors Li and Lo are transferred to the load Ro capacitor Co2 is fed by the Cs and Co3 is fed by Cs1 because they are parallel connected and the current passing through Li and Lo are reduced continuously according to the relation –Vo/Li and –Vo/Lo respectively.

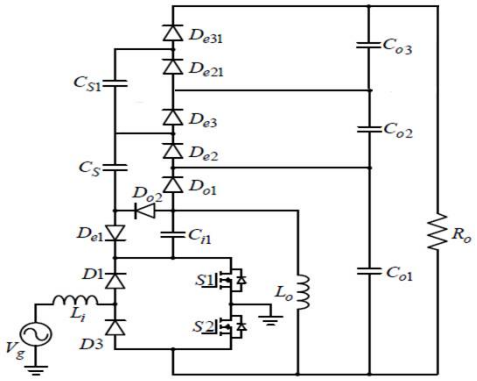

Fig 1.4: Proposed Structure

Mode-III:

The time period Δt3 (stage-3)in fig1.3 starts when the forward current in Do1 becomes null. In this stage, the capacitor Cs and the inductors Li and Lo maintain the energy transference to the capacitors C01, C02 and to the load Ro. this is an additional stage that does not occur on Sepic rectifier.

MODE IV:

The time period Δt4 starts (stage-4) in fig 1.4 start when the currents through input inductance (ILmin) and output inductance (ILomin) are equal, however with opposite signs. Therefore the forward current in diode Do2 is null and the converter is in the discontinuous conduction mode of Sepic. During this stage the capacitors Co1 and Co2 fed the load Ro.

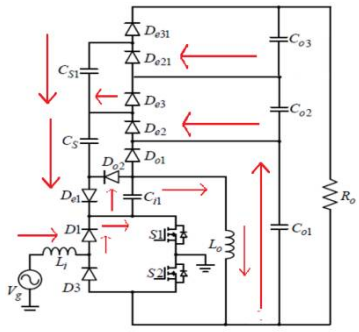

Fig 1.41 Mode-1 Operation Of Proposed Structure

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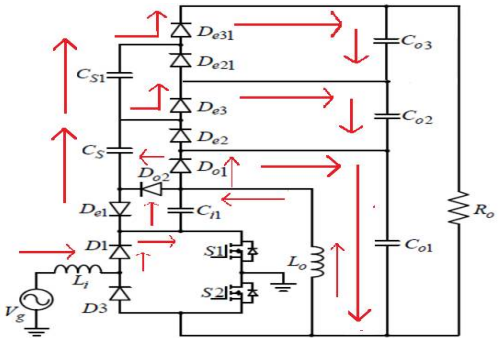

Fig 1.42 Mode-2 Operation Of Proposed Structure

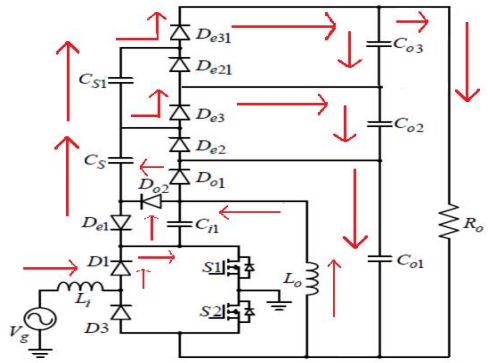

Fig: 1.43 Mode -3 Operation Of Proposed Structure

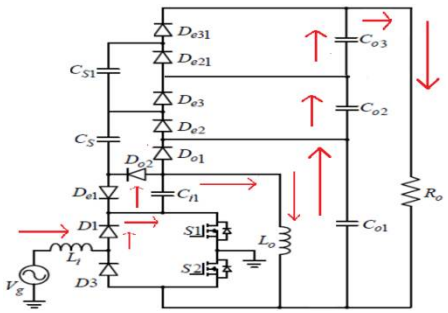

Fig: 1.44 Mode-4 Operation Of Proposed Structure

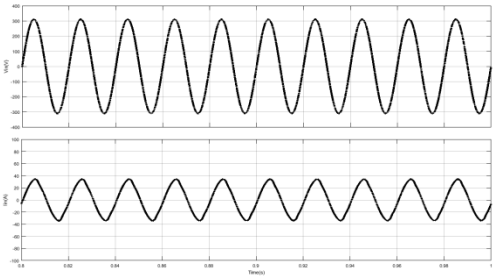

Fig:1.5 Input And Current Waveform Of Proposed Method

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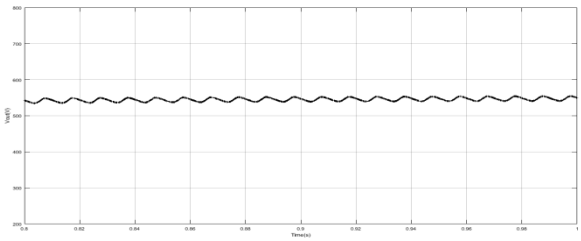

Fig:1.6 Output Voltage Of Proposed Method

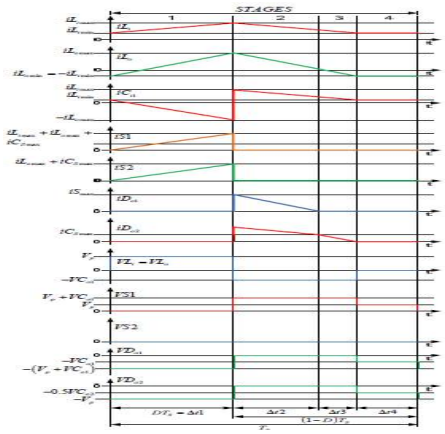

Fig:1.7 Switching Period Of Proposed Structure

The main ideal waveforms of the proposed converter for a switching period and for a grid period are illustrated in fig1.7 and fig1.8, respectively. The input voltage Vg and current iLi of the converter are shown in the graph of fig1.8, while the output voltage Vo and the voltages across Co1 and Co2 are sown in the same graph. The rectifier has zero harmonics because the input current is in phase with the input voltage and it ensures the multiplication of the output voltage(VC01= VC02 and VC0=2VC01).currents and voltages in all components is shown for only one time period in fig 1.7.

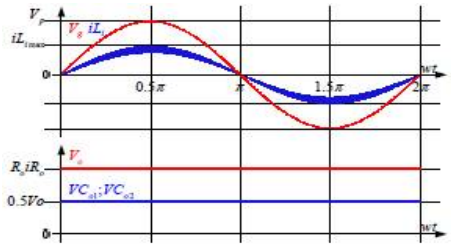

Fig:1.8 Voltage And Current Waveforms Of Proposed Structure

Design equations:

The static gain and the main equations for the design of passive components of the proposed hybrid rectifier are presented below. These equations allow the reproducibility of this design of this system with other specifications.

Static gain:

The static gain of the proposed rectifier is defined by the ratio between output voltage (Vo) and the input voltage peak (Vp), as can be seen by the expression(1).

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$$G = \frac{V_0}{V_p} = D\sqrt{\frac{R_0\left(L_i + L_o\right)}{4L_i L_0 f_s}} \tag{1}$$

Inductors design:

The values of inductors Li and Lo are showed in (2) and (3) equations, respectively. The inductor Li is calculated from a ripple current specification. The output inductor Lo is obtained from the values of Li, thus it ensures that the rectifier will operate in discontinuous conduction mode.

$$L_i = \frac{V_p D}{\Delta i_{Li} f_s} \tag{2}$$

$$L_o = \frac{L_i R_o {V_p}^2 D^2}{2L_i {V_o}^2 f_s - R_o {V_p}^2 D^2} \tag{3}$$

The average and rms values of input and output inductor currents are presented in (4),(5)and (6)

$$I_{Lief} = \frac{\sqrt{6}}{24}\sqrt{\frac{D^3 {V_p}^2\left({V_o}^2 L_i D\left(12L_i + 24L_o\right) + {L_o}^2\left(16{V_o}^2 - 9{V_p}^2 D^2\right)\right)}{{V_o}^2 {L_i}^2 {L_o}^2 {f_s}^2}} \tag{4}$$

$$I_{Lomed} = \frac{D^2 {V_p}^2 (L_i + L_o)}{4V_o L_i L_o f_s} \tag{5}$$

$$I_{loef} = \frac{1}{24}\sqrt{\frac{V_p V_o {L_i}^2 (128 - 192D) + {V_p}^2 L_o D\pi\left(-27L_{oa} + 54L_i\right) + {V_o}^2 {L_i}^2 \pi(48 - 36D)}{{V_o}^2 {L_i}^2 {L_o}^2 {f_s}^2 \pi}} \tag{6}$$

Capacitors design:

Equation (7) and (8) define, respectively. The capacitance value of capacitors Ci1, Co1, Co2, Co3 and Cs, Cs1. The capacitor Ci1 is designed from the ripple voltage specification and capacitors Co1, Co2, Co3 and Cs, Cs1 are designed from the hold- up time.

$$C_{i1} = \frac{D^2 V_p [D\left(V_p L_o - V_o L_i\right) + 2V_o L_i]^2}{8{V_o}^2 {L_i}^2 L_o \Delta V_{cil} {f_s}^2} \tag{7}$$

$$C_s = C_{S1} = C_{o1} = C_{o2} = C_{o3} = \frac{2P_o t_{hut}}{{V_o}^2 - (0.9V_o)^2} \tag{8}$$

V. SIMULATION CIRCUITS AND RESULTS

The prototype of the proposed hybrid bridgeless rectifier was implemented according to the specifications present in the table I. The simulation parameters used in the proposed structure is presented table II.
The experimental results were obtained with the rectifier operating with output voltage in open loop and rated power.

Figure 1.5 presents the waveform of input current in phase with the input voltage. The harmonic spectrum of the input current is shown in figure, which has a total harmonic distortion, around 1.93%.thus it leads to power factor of 0.998.

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Figure 1.6 presents the waveform of output voltage and output current. The average value of output voltage is about 550V and average output current is1.35 A. thus the output power processed by rectifier is 728 W.
Though the output voltage Vo and voltage across capacitors Co1, Co2 and Co3 are measured. As expected, the capacitor voltages are balanced and they are approximately half of the output voltage value.
The voltage values across capacitors Cs, Co1, Co2 and Co3 is noted that the values of these voltages are about 200V.The RMS value of current through Cs is about 9.55A and 3.79A, respectively.
The voltage across switch S and diode Do1 is measured. The maximum voltage across switch is about 527.8 V while the maximum reverse voltage across the diode is about 555.1 V.

Table-I Comparison Table Of Conventional And Proposed Specifications

Specifications	Conventional values	Proposed values
Input peak voltage(V_p)	311	311
Output voltage(V_o)	400	550
Switching frequency(f_s)	50hz	50hz
Maximum duty cycle(D)	0.35	0.35
Hold up time(t_{hut})	8.33ms	8.33ms
C_{il} ripple voltage	20%	20%
L_i ripple current	10%	10%

Table-II Simulation Parameters

Parameters	Values
Inductor L_i	6.67 mH
Inductor L_o	120 µH
IGBT S_1 and S_2	SPW47N60C3(650 V/47 A)
Diodes D_{o1}, D_{o2}, D_{e1}, D_{e2}, D_{e3}, D_{e4}, D_{e5}	MUR860(600 V/8 A)
Capacitor C_{il}	2x470 nf/400V
Diodes , D_1, D_2	IN5408(1000 V/3A)
Capacitors C_{o1}, C_{o2}, C_{o3}, C_s, C_{s1}	2x1 mf/250 V
Control circuit	UC235

VI. CONCLUSIONS

This paper proposes a hybrid PWM dcm sepic rectifier with a modified switched capacitor cell. The resulting structure maintains the sepic rectifier characteristics and adds the multiplier characteristics of switched capacitor.

When compared to the conventional sepic rectifier, the proposed topology employs more components, however it supplies double gain in the output voltage. Therefore, the converter has potential to appliances in which a higher output bus is required.

The modified switched capacitor cell, proposed in this paper, ensured multiplying the output voltage of the converter and keeping the reproduction of the input rectified voltage harmonics on the capacitor of the sepic. The experimental results corroborate the adequate operation of the proposed hybrid rectifier, which drains practically sinusoidal current from mains with a total harmonic distortion nearly 1.93% and supplies double gain in the output voltage. Based on these beginnings it was verified the integration of classic rectifier sepic with switched capacitor

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