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Design and Implementation of FPGA-based High Speed DQPSK Modulation System

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ABSTRACT: Differential QPSK or DQPSK is similar to QPSK system, but in the DQPSK the initial phase of modulated signal is effected by the initial phase of the previous modulated signal. The QPSK phase shift is based on assumption that the previous modulated signal has the initial phase zero. In the DQPSK the initial phase of transmitted signal is the addition result from the phase shift with the initial phase of previous modulated signal. Here we introduce the implementation principle and scheme of an all-digital high speed differential quadrature phase-shift keying (DQPSK) modulator. The modulator adopts FPGA and DAC to realize DQPSK modulation. FPGA accomplishes data randomization, differential encoding, channel coding, symbol mapping and transfers I/Q data to DAC. The index test by instrument and application in pilotless aircraft indicate that the modulator's index is far excellent than the other method.

KEYWORDS: DQPSK, FPGA, all-digital, DAC, QPSK

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I. INTRODUCTION

With lots of merits, such as high spectrum utilization, fine spectral performance, strong anti- interfere capability, rapid transmit speed, the quadrature phase-shift keying (QPSK) modulation has been used in wireless wideband digital communication systems extensively, and becomes an important modulation and demodulation method in telemetry transmitting and receiving systems. DQPSK is an improvement modulation of QPSK, which overcomes the carrier signal's phase fuzziness in QPSK. The binary data for Direct Digital Synthesizer (DDS) in DQPSK is the phase change between the adjacent codes in QPSK. In the QPSK by using coherent detection the receiver part must understand the frequency an phase of transmitted signal exactly. But in the real condition this process is very difficult, and carrier recovery process never gets this ideal condition. Same with the DPSK system in the DQPSK the important thing is different value of present and previous phase of received signal. By using this technique the receiver part doesn't need recover the phase of received signal exactly as like in the QPSK system. Or it can be said that the DQPSK system is easier to build than the QPSK system

II. SYSTEM MODEL

1. Direct Digital Synthesis

A digitally-controlled method of generating multiple frequencies from a reference frequency is called Direct Digital Synthesis (DDS). A stable clock drives a programmable-read-only-memory (PROM) which stores one or more integral number of cycles of a sine wave (or other arbitrary waveform, for that matter). As the address counter steps through each memory location, the corresponding digital amplitude of the signal at each location drives a DAC which in turn generates the analog output signal.

2. FPGA Implementation

Field Programmable Gate Array(FPGA) implements data randomization, differential encoding, channel encoding, symbol mapping, through DDS that work concurrently. FPGA can output high center frequency modulation signal through LVDS transmission interface.

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III. DESIGN AND ANALYSIS

Fig. 1 defines the structure of modulator comprising FPGA and DDS. The output of DDS is fed to DAC circuit to get the analog sine wave output signal

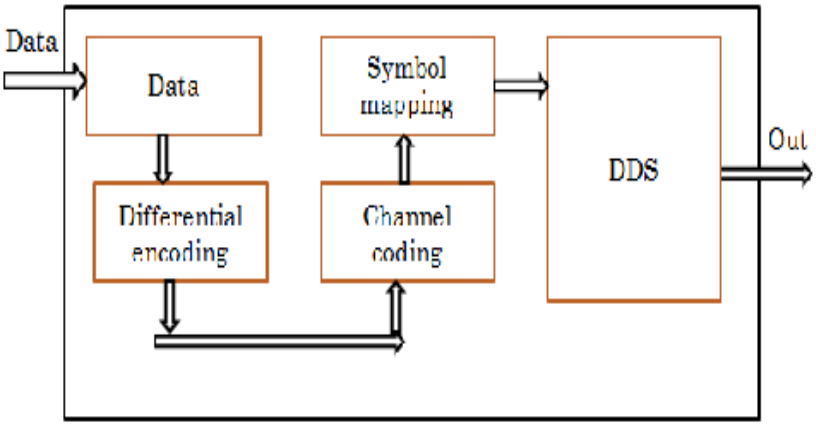

Fig. 1: Structure of modulator

The spectral purity of the final analog output signal is determined primarily by the DAC. The phase noise is basically that of the reference clock. The heart of the system is the phase accumulator whose contents are updated once each clock cycle. Each time the phase accumulator is updated, the digital number, M, stored in the phase register is added to the number in the phase accumulator register. Assume that the number in the delta phase register is 00...01 and that the initial contents of the phase accumulator are 00...00. The phase accumulator is updated by 00...01 on each clock cycle. If the accumulator is 32-bits wide, 2^{32} clock cycles (over 4 billion) are required before the phase accumulator returns to 00...00, and the cycle repeats. The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each address in the lookup table corresponds to a phase point on the sine wave from 0° to 360°. The lookup table contains the corresponding digital amplitude information for one complete cycle of a sine wave. (Actually, only data for 90° is required because the quadrature data is contained in the two MSBs). The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC.

FPGA implements the following:

1. Data Randomization is to maintain bit (or symbol) synchronization with the received communications signal; every data capture system at the receiving end requires that the incoming signals have a minimum bit transition density. In order to ensure proper receiver operation, the data stream must be sufficiently random. Data randomization can randomize the input serial data and reduce the continuous 0 or 1 in serial data.
2. Differential Encoding is used to protect against phase ambiguity. It is one of the simplest forms of error protection coding done on a baseband sequence prior to modulation. Main purpose of Differential Encoding is to protect against polarity reversals of input bit sequences. Differentially Encoded data sequences have a slightly superior error performance.
3. Channel coding can map information space of general serial code into larger information space to increase the difference level between different codes, which is called coding gain. The modulator adopts convolutional coding to fulfill channel coding, convolutional coding is usual channel coding method.
4. Symbol Mapping is an easier way to separate the original signal into a set of independent components or channels: *I* (In-phase) and *Q* (Quadrature). This is obtained from symbol mapping. A single carrier generated by a local oscillator (L.O.) circuit is split into two paths. One path is delayed by an amount of time equal to ¼ of the carrier's cycle time, or 90 degrees. The two carriers are amplitude modulated—one by the I signal, the other by the Q signal. The two modulated carriers are added together in a summing circuit. The output is a digitally modulated signal whose amplitude and phase are determined by the amplitudes of the two modulating signals.

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IV. MODULATION TECHNIQUE

The power and elegance of DDS are most apparent when a modulated source is required. The frequency of the output may be changed instantly to any frequency from DC to f_{max} by simply changing the number in the phase increment register. The graph below (next page) shows the block diagram of a DDS phase accumulator with programmable modulation capabilities. This phase accumulator, which has been optimized for function generator applications, has two phase increment registers: PIRA and PIRB. A 48-bit wide multiplexer can switch between the PIRs in a single clock cycle. The modulation processor can modify the PIRs at a rate of up to 10 million bytes per second, filling one PIR while the other is used as an input to the adder. Complex modulation programs may be stored in the modulation RAM. This RAM contains op-codes and data for the modulation processor. Frequency scans illustrate the operation of this processor. When programmed for a log frequency sweep, a list of up to 4000 discrete frequencies is stored in the modulation RAM by the host system. The modulation processor modifies PIRA while the adder is using PIRB and vice-versa. More complex modulation programs may be stored, such as frequency modulation by any arbitrary function, linear or log sweeps, frequency hopping, etc. Phase modulation is easily done by programming PIRA with the nominal frequency, and using PIRB, which contains the nominal phase increment plus any desired phase shift, for a single clock cycle. Wide frequency or phase deviations are no problem. Any phase or frequency hop may be programmed and executed in a single clock cycle. And since the PIRs may be modified very quickly, modulation frequencies up to several hundred kilohertz are possible. In fact, arbitrary modulation programs may be stored. This feature allows the function generator to be used for modem testing, communications, bit error rate determination, etc

.V. RESULT AND DISCUSSION

In the fig 2, it shows the Simulation Waveform of DDS Output. The dout is the output of system comprising DDS through the communication channel.

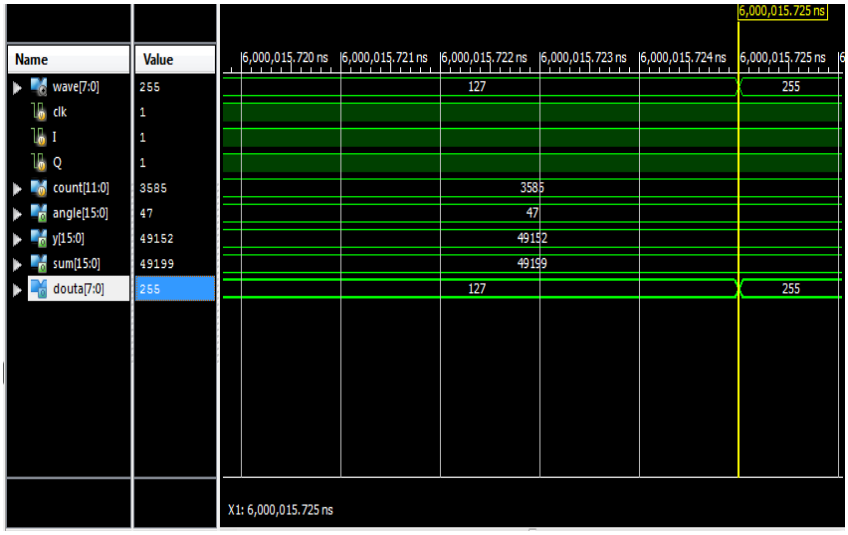

Fig. 2: Simulation Waveform of DDS Output

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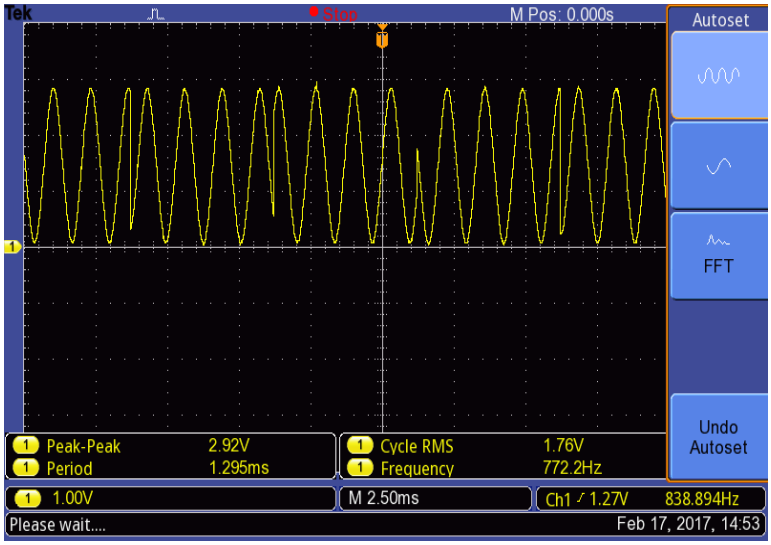

Fig. 3: DSO Output of DDS

In the fig 2, it shows the DSO Output of DDS. This is the hardware implementation of DDS when fed to DAC circuit.

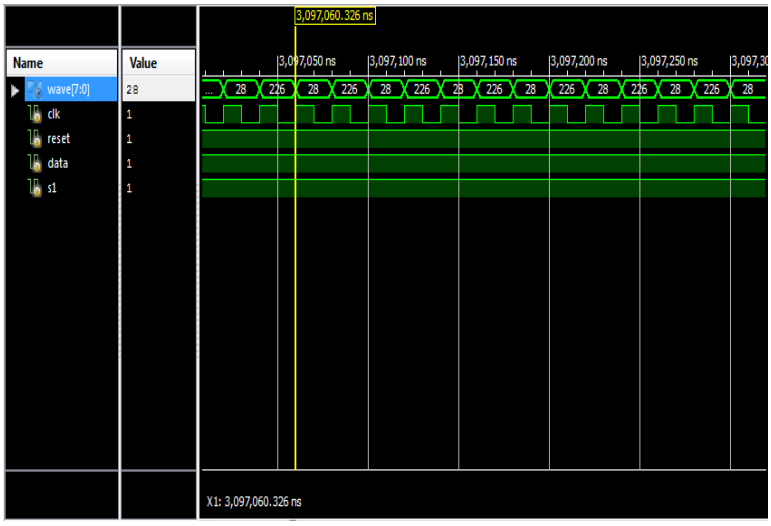

Fig .4: Simulation Waveform of Modulator Output

In Fig 3, Simulation Waveform of Modulator Output .This is the realization of FPGA comprising of data randomization, differential encoding, channel coding, symbol mapping.

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VI. CONCLUSION

The design of an all-digital high speed DQPSK modulator is implemented and discussed principle of algorithm. With novel algorithm and concurrent processing hardware, the modulator has good real-time performance. According to the practical laboratory experiment and fight test, the sensitivity performance of DQPSK channel is excellent. Because of excellent flexible architecture, the modulator can be used in high speed data transmission in pilotless aircraft or other occasion.

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