



Feature Extraction of Moving Objects with Edge Detection

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ABSTRACT: For many applications such as medicine, space exploration, surveillance, authentication, automated industry inspection and many more areas digital image processing is an expanding and dynamic area with applications reaching out into our everyday life. Edge Detection and Feature-Extraction are the important process in motion recognition is required to be processed for building high speed systems. Edge is a basic feature of an image. Edges define the boundaries between regions in an image by locating sharp discontinuities in pixel values, which helps with segmentation and object recognition. Image Edge detection significantly reduces the amount of data and filters out useless information, while preserving the important structural properties in an image. Since edge detection is in the forefront of image processing for object detection. This project describes Sobel Edge Detection algorithm and labeling algorithm for extracting features of images. And feature extraction moving images that is video is done using subtraction method.

KEYWORDS: Sobel Edge Detection, Two Pass connected component labelling, MATLAB/ Simulink, Virtex-5 (xc5vsx50t-1ff1136) FPGA

I. INTRODUCTION

Nowadays, in various applications such as video surveillance, automotive vehicle control, efficient human-computer interaction, remote gesture control and so on motion recognition is becoming increasingly important. For this applications high speed image processing can significantly provide much details of the motion, which is very useful for improving the speed and precision of the recognition. For the applications which are useful for our everyday life such as in medicine, space exploration, surveillance, authentication, automated industry inspection and in many more areas digital image processing is an ever expanding and dynamic area. For building such high speed systems, Motion Feature-Extraction is an important and computationally heavy process in motion recognition. Firstly edge detection is required to be done before the process of feature extraction of images. Application specific hardware offers much greater speed than a software implementation. There are two types of technologies available for hardware design. Full custom hardware design called as Application Specific Integrated Circuits (ASIC) and semi custom hardware device, which are programmable devices like Digital Signal Processors (DSP) and Field Programmable Gate Arrays (FPGA). ASIC design offers highest performance, but the complexity and the cost is very high and time taken to design the hardware is also very high. DSP's are well suited to extremely complex math intensive tasks such as image processing but hardware design knowledge is still required and the learning curve is much lower than some other design choices. Field Programmable Gate Arrays are programmable devices. They are also called reconfigurable devices. Hardware design techniques such as parallelism and pipelining can be developed on a FPGA because of which speed of operation increases, so it will be beneficial in reduction of execution time. So FPGAs are ideal choice for implementation of image edge detection. Software implementation of edge detection and feature extraction carried out in MATLAB. Edge detection can also be implemented on Spartan 3, Spartan 6, Virtex5 FPGA boards.

Edge detection is the process of classifying and locating discontinuities in digital image intensity. In many image processing algorithms edge detection is always first step as it reduces the amount of data and filters out useless information.

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II. SYSTEM ARCHITECTURE

For feature extraction of images firstly edge detection of images and after that labeling algorithm is used. A system block diagram explains basic idea about implementation of the system.

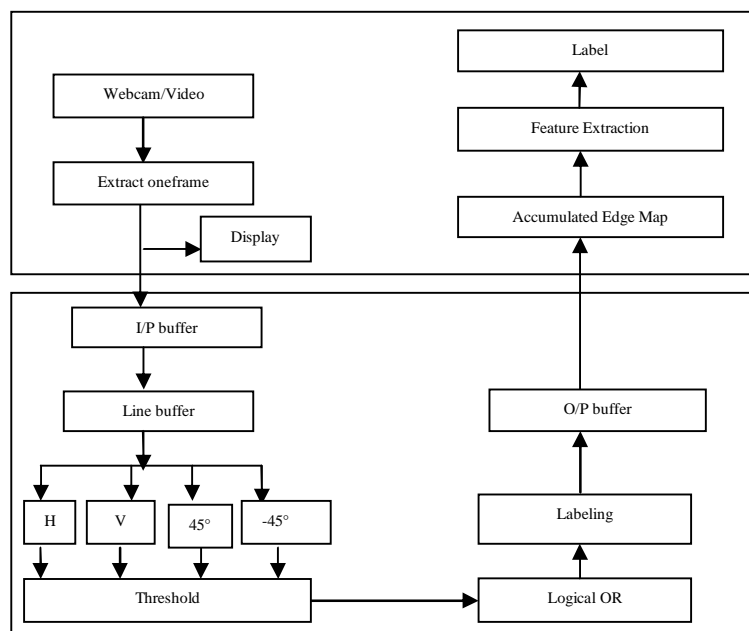


Fig.1 System Block Diagram

A. Edge Detection

Basic idea about hardware implementation of sobel edge detection algorithm on FPGA board is shown in Fig.2 The overall system consists of following blocks input image & image pre-processing, image edge detection process, Merged Significant Edge Map generation, Virtex5 FPGA board.

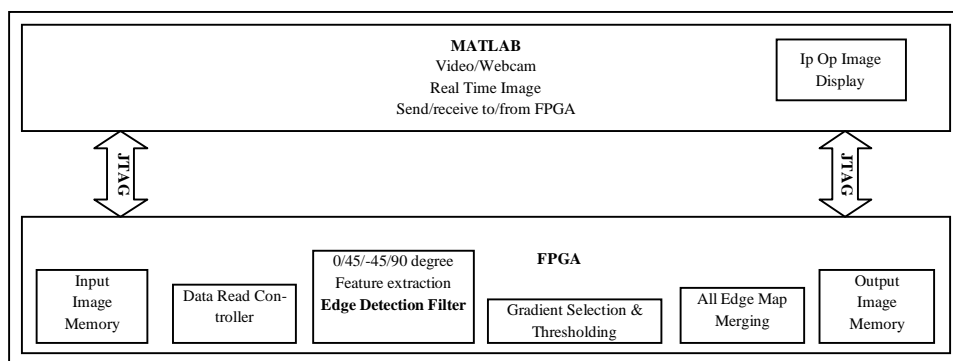


Fig.2 Block Diagram of Edge Detection

The block diagram shown above explains edge mapping and edge detection by hardware co simulation. By using FPGA and MATLAB edge detection and mapping take place. In this process firstly video frames are captured through the MATLAB and this video frames are captured via stored video or webcam. And after that this video frames are



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passed to share memory. During this, Image will be stored to FPGA memory and MATLAB Tool will manage automatically. After that input image data is read by using data read controller block. Then this image data will be passed to edge detection block. In edge detection filter block four different filters will work simultaneously. These four filters are the 0/45/-45/90 degree filters. Then output of these filters will be given to the next block that is Gradient Selection and Thresholding block. Therefore all the output of filters will be threshold. Now all edge map images will be combined as shown in above fig. by using edge map merging block and store in to memory. Here also Image will be read from FPGA memory and MATLAB Tool will manage automatically. Finally both input and output that is edge map frames will be displayed in real time in MATLAB.

B. Labeling algorithm

Labeling component is a commonly used technique for extracting high-order objects. Labeling Components are the basic ingredients of all high-order objects therefore a commonly used technique for extracting objects. Labels each component using a contour tracing technique. This method is based on the principle that a component is fully determined by its contours, just as a polygon is fully determined by its vertices. This method also provides a procedure for finding all component pixels. An image can be scan the same way as it would be encountered by a scanner, i.e., from top to bottom and from left to right per each line.

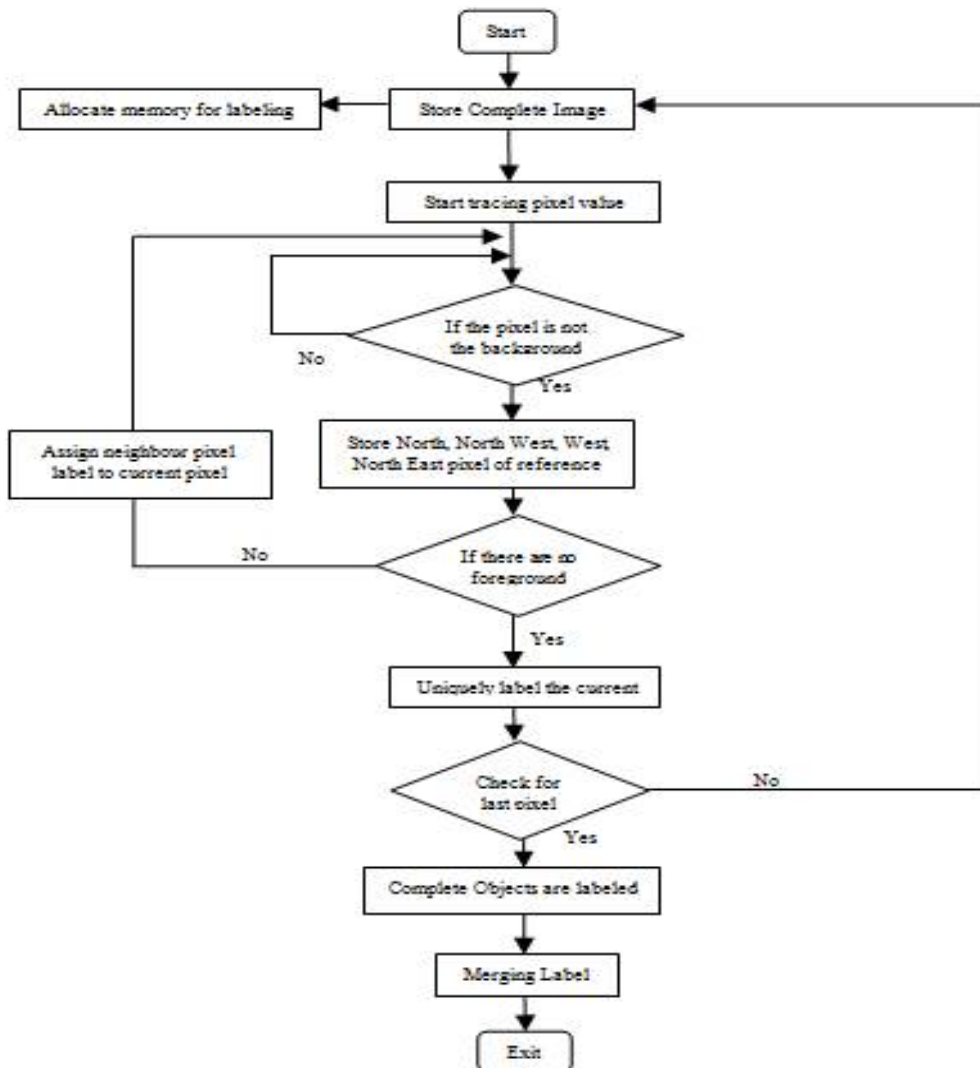
1) Overview of Two Pass Connected Component Labeling Algorithm: Algorithms discussed thus far are mostly suitable for all foregrounds or all background distinct pixels and their immediate neighbors. Here we are considering middle ground between the set of all foreground pixels and background pixels. This arises the general concept of connected components which is also called as objects in further discussion.

Two-pass algorithms: Many algorithms in this group operate in three distinct phases.

(i) Scanning phase: In this phase, the image is scanned once to assign provisional labels to object pixels, and to record the equivalence information among provisional labels.

(ii) Analysis phase: This phase analyzes the label equivalence information to determine the final labels.

(iii) Labeling phase: This third phase assigns final labels to object pixels using a second pass through the image. The system flow diagram carries out the process of tracing and labeling of an object in given input image. This method uses multiple tracing. The flow chart given below explains the flow of connected component labeling algorithm. It gives the detail idea about working of algorithm.



III. RESULTS

A. System Generator model of Edge detection

By double-clicking on the Simulink icon in MATLAB, the Simulink Library Browser opens. The Video and Image Processing toolbox from the Simulink library is used to design this model. From this toolbox, we access the different elements used to design this model. The various blocks, elements and the sub-systems included in this model are described in detail below. Fig.10 shows the Simulink design of image edge detection algorithm based on sobel operator.

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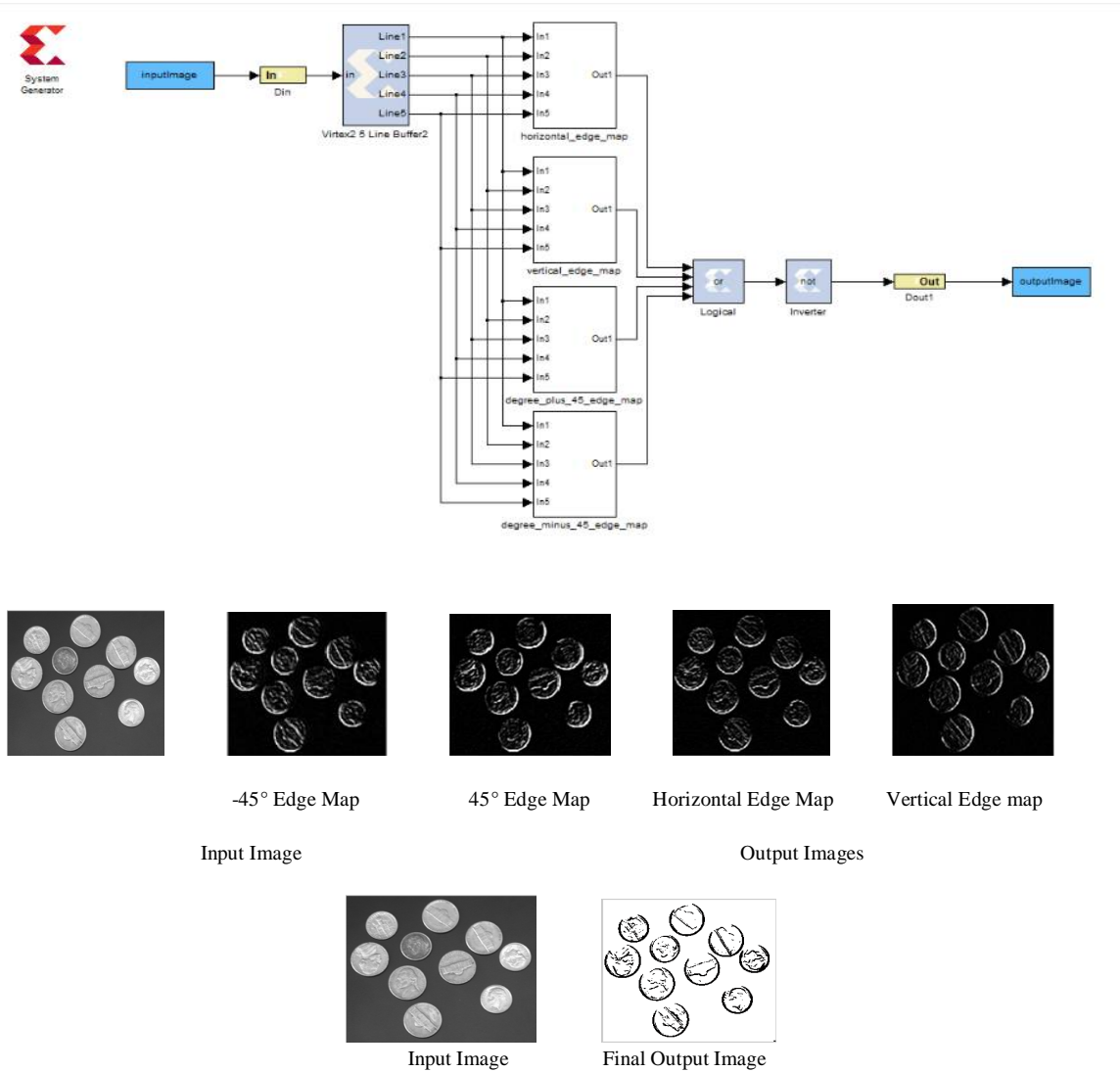


Fig.10 System generator model of Edge Detection algorithm and input and output images

B) FPGA Results for Edge Detection

1) For Inbuilt Input Image from MATLAB:

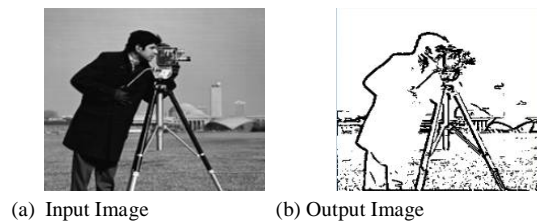


Fig. 11 FPGA Result for Inbuilt MATLAB Image of Cameraman

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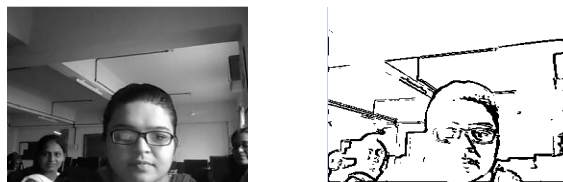
2) For Inbuilt Video:



(a) Input Video (b) Output Video

Fig.12 FPGA Result for Inbuilt MATLAB Video

3) For Real Time Input via Webcam:



(a) Real Time Input (b) Real Time Output

Fig.13 FPGA Result for Real Time Input via Webcam

C) Modeling of FPGA Implementation using Two Pass Connected Component Labeling Algorithm

By double-clicking on the System Generator icon in Matlab, the System Generator Library Browser opens. The Video and Image Processing toolbox from the library is used to design this model. From this toolbox, access the different elements used to design this model. The various blocks, elements and the sub-systems included in this model are described in detail below. Fig.14 shows the System generator model design of Two Pass Labeling algorithm based on connected component labeling.

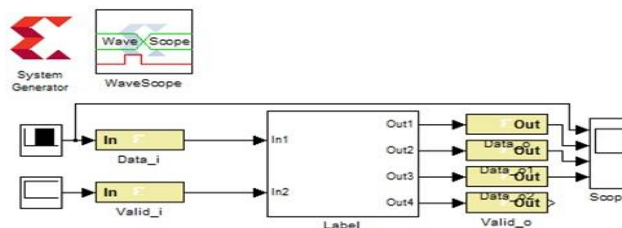


Fig. 14 System generator Model of Two Pass connected component Algorithm

1) *MATLAB Results:* The Fig.16 shows the MATLAB output of labeling method. There are three images displayed at the output. First image is simple binary image, second is primary labeled image and third is merged image. Following are the results of MATLAB simulation for different images.

From the output it can be observe that for primary labeled objects some portion at the upper side have different color and remaining portion have different color .This is because in primary labeling we are using multiple tracing and same object is divided in two parts while tracing. This causes same object to be labeled with two different labels.

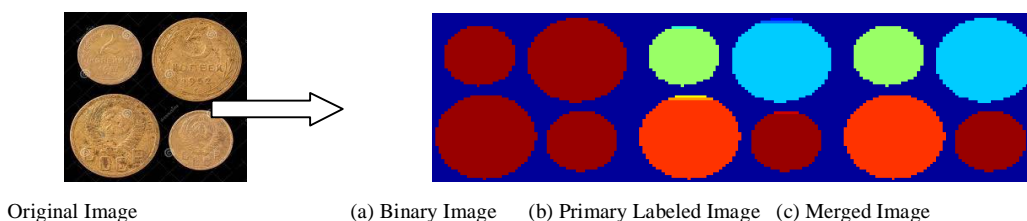


Fig. 16 Results of Two Pass Connected Component Labeling Algorithm of Image of Coins

D) Merging Model of Edge Map and Labeling

In this model merging of edge map and labeling is done for extracting features like area, centroid and bounding box of the objects present in the images. Here, two morphological operations that are erosion and dilation are used for the merging of edge mapping and labeling.

1) *System Generator Model for Merged Model of Edge Map and Labeling for Feature Extraction:*

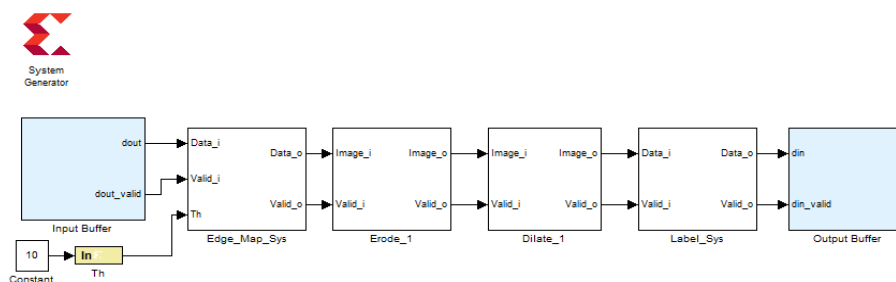


Fig. 17 Merged Top Model

Above Figure shows the System Generator Model for merging of Edge Map and Labeling algorithm. As shown in figure there are many blocks like Input buffer for Input to the Model, Edge Map block for the Edge Detection of images. Erode block is used to perform the morphological operation on edge detected images that means unwanted edges removed due to use of this erosion operator. Erosion operation not only removes the unwanted edges but also shrink another edges and this is the disadvantage of erosion. Therefore to overcome this disadvantage of erosion here dilate operator is used. Dilate block is used to gain the original shape of the image which changed due to use of erosion. Further Labeling block is used to perform the labeling and then merging operation of the images. And finally output buffer stores the output images and displayed on MATLAB. Morphological Operations and concept of Erosion and Dilation are described below in detail.

E) Results with FPGA Implementation

The figure below shows the system generator model result of Two Pass Labeling algorithm on hardware. Figure shows the system generator results for the image “Fruits” with Fig. (a) is the original input image. Fig. (b) is the simple labeled output image. Fig (c) shows output where different colors are assign to different objects. Fig.(d)is the final output after merging in second pass.

The Hardware Model displays different features of the detected objects. The Blob Analysis block is used to calculate following Features for labeled regions in a binary image. The Blob Analysis block supports input and output variable size signals.

- 1) No of objects detected
- 2) Bounding Box
- 3) Centroid of detected object
- 4) Area of object

Fig.18 shows original input image which is taken as input in MATLAB. The image consists of multiple different fruits with different shapes.



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IV. CONCLUSIONS

The implementation of Image Edge Detection Algorithm, Labeling algorithm and merged model of Edge Map and Labeling algorithm for extracting features on FPGA is present in this paper, and it is carried out successfully. The hardware and software implementation of system is found to be working properly. The MATLAB/Simulink models are used for the compatibility of implementing the image processing system on FPGA. The Virtex-5 ML506 evaluation board is user friendly which is used to implement this system. Implementation of Sobel Image edge detection algorithms using MATLAB/ SIMULINK is described. Edge Detection and feature extraction is done for still input images, inbuilt video and for Real time input from webcam of Laptop. By using two connected component labeling algorithm objects of images are labeled for distinguishing the objects. Therefore with the help of edge detection and labeling of images the various features i.e. area, bounding box and centroid are extracted.

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