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Design of Low Power Multiplier Architectures Using Vedic Mathematics

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ABSTRACT: A Multiplier is an important function in arithmetic operations. The mostly problems faced in a multiplier are power dissipation and more delay. Multipliers are widely used for calculation of DCT, DST and DFT in the field of DSP and image processing .To design operations for digital signal processor, multiplication plays an important role. Signal processing operations can be performed using multiplier such as convolution and correlation [DSP]. These multiplication operations can be implemented using Vedic Multiplication algorithms mainly the "Urdhva Tiryakbhyam (UT) Sutra", which is the most used one Vedic Multiplication algorithm [Vedic Book] that is fast techniques that have been in practice for a long time. This paper proposes an 8- bit Vedic Multiplier which consists of UT Sutra (Vertical and Crosswise). This process is done by using Tanner EDA software. There is 0.776µW power consumption and propagation delay o.408 at 400mV.

KEYWORDS: Multiplier, Vedic Mathematics, Urdhva Tiryakbhyam Sutra, Half Adder, Full Adder.

I.INTRODUCTION

One of the most important block in any processor is a Multiplier. A binary Multiplier is an electronic circuit used in digital electronics. Multipliers are widely used in the field of DSP [14] and image processing which involves multiplication operations, whose performance depends on the effectiveness of the multiplier units. The field of communication involves multiplication of two signals for modulation and demodulation. A conventional multiplier block consists of a chain of AND gates to generate the partial product terms and an adder assembly to add them. The speed limitation associated with the conventional multiplier is due to the latency introduced by long adder tree structures. [7] The power consumption and propagation delay of a multiplier unit is a major design concern. Many researchers have tried to design multipliers which offer either of the following – low power consumption, high speed and hence less area. The use of Vedic Mathematics for multiplication [4] with UT Sutra is applied to the binary number system and is used to develop digital multiplier architecture resulted in significant improvement in the overall speed and power consumption of multiplier.

The paper proposes low lower multiplier architectures based on Vedic Mathematics for high speed computing. The proposed 4-bit and 8- bit multiplier architectures based on the Urdhva Tiryakbhyam (Vertical and Crosswise) [3] Sutra of Vedic Mathematic are realized using 22nm CMOS process technology in Tanner EDA tool. A 5T AND gate design based on pas transistor logic and transmission gate logic, has been used in this work for generation of partial products instead of the conventional 6T CMOS based design. The adder chains used in the multiplier units uses 14T full adders and 9T half adders optimized for low power and high speed arithmetic. The use of such modified topologies results in smaller chip area. The delay associated with the proposed architectures is also reduced with reduced number of transistors.

The paper organization is as follows, Section II provides a general overview of the Vedic Mathematics utilized in the design. Section III gives a detailed discussion on the multiplier architecture with detailed discussion on the various building blocks. The Section IV summarizes the performance analysis and the result. Section V concludes the paper.

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II. URDHVA TIRYAKBHYAM (UT) SUTRA

Veda means knowledge which is a Sanskrit word. Vedic mathematics provide effective computing methods for high speed arithmetic. Veda is rediscovered by the Jagad Guru Shree Bharti Krishna Tirth Ji Maharaj. According to him the Vedic Mathematics is based on 16- Sutras (algorithm) [3] .

The *Urdhva Tiryakbhyam* (UT) sutras are applicable for all cases of multiplication. The formulae itself is very short and terse, consisting of only one compound word and means "vertically and crosswise". The use of UT sutra for multiplication reduces the latency of a multiplier unit by introducing parallel computing of partial products. The Multiplication for 2-digit decimal numbers multiplication is illustrated in fig.1

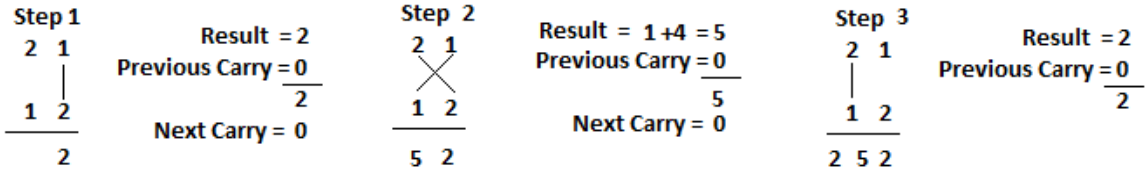

Fig. 1 UT based multiplication for 2 digit decimal numbers

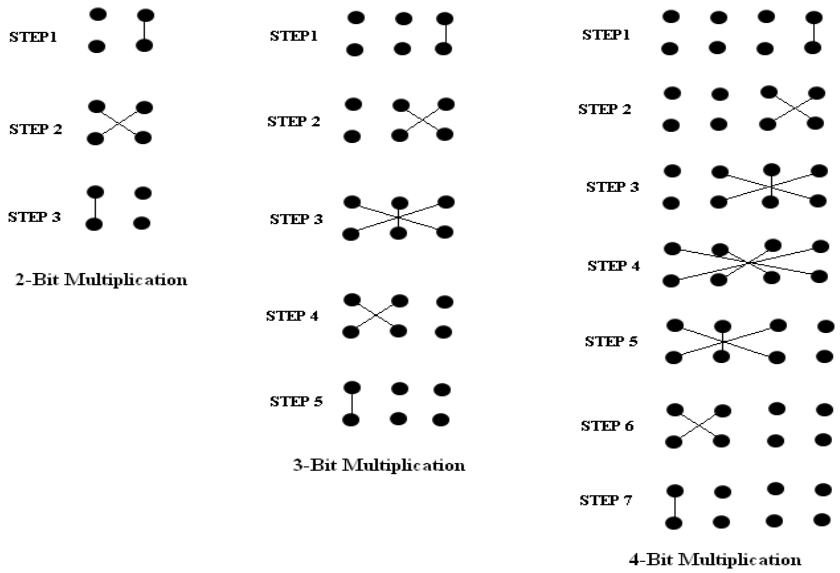

Fig. 2 Line diagram for binary multiplication using UT sutra

In decimal number system, this UT sutra is mostly used for multiplication. However it can be extended to execute binary number arithmetic operations. The line diagram of binary multiplication using UT method for 2-bit, 3-bit and 4-bit numbers is as shown in Fig. 2.

The partial product generation as indicated by the vertical and crosswise lines as shown in the figure is primarily an AND operation. The 2-bit multiplication with two inputs A [1:0] and B [1:0] the following expressions are obtained.

P0= B0A0 (1)
C1P1= B0A1 + B1A0 (2)
C2P2= C1 + B1A1 (3)

Where, B*i*A*j* represents the partial product terms for corresponding bit positions *i* and *j* of the operands. From partial product addition C1 and C2 are the carries generated and C2P2P1P0 is the result of the multiplication. The 4-bit Multiplication, as shown in the line diagram of Fig. 2, can be carried out by using 2-bit Vedic multipliers [5-10]. Any 4-bit binary number A can be represented as AhAl where Ah denotes the most significant 2 bit positions and Al is the least significant 2 bit positions. A similar concept is used for the number B which is represented as BhBl. Following the

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same process, two 8-bit binary numbers A and B, represented as AhAl and BhBl respectively, where Ah and Bh are the higher nibbles and Al and Bl are the lower nibbles, can be multiplied using 4-bit multiplier blocks. The line diagram for 8-bit multiplication [13] is provided in Fig. 7.

III. MULTIPLIER ARCHITECTURE

This paper proposes the multiplier architectures which are based on UT sutra of Vedic mathematics. The partial product generation is realized by 5T pass transistor and transmission gate based AND gates which is described in this paper [2]. The overall on-chip area occupied by the multiplier can be reduced by use of such a modified AND gate design. As the number of AND gates used for partial product generation increases with the word length, the use of this modified design plays a greater role for higher order multipliers (32-bit, 64-bit *etc.*). New full adder and half adder topologies are used in the adder chain, for the proposed multiplier architectures, incorporate that are optimized for low power, high speed and full swing applications. New adder units provides the overall improvement in delay characteristics of the multipliers which addresses the main performance associated with the conventional designs i.e. the latency introduced by the adder assembly. The adder architectures are also discussed below.

A. AND Gate

In this paper a 5T based AND gate, given in Fig. 3, is utilized for the partial product generation. The pass transistor logic and transmission gate based logic is utilized for designing AND gate [ ]. It is basically a multiplexer based approach which implies the output A AND B, with any arbitrary operands A and B, is same as B for A being equal to logic 1 and is grounded for A being logic 0. The design makes use of one less (i.e. 5) transistors as compared to the conventional 6T based CMOS design and hence results in a reduction of the overall on chip area requirement of the complete multiplier architecture. An 8-bit binary multiplier uses 64 AND gates for partial product generation and thus the use of the new AND gate topology brings down the number of transistors by 64 per each multiplier unit. However, the use of such designs does not affect the delay characteristics significantly as the partial product generation is performed.

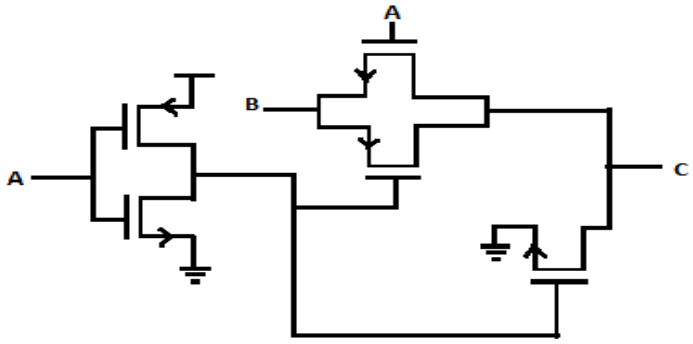

Fig.3 Modified AND gate design

B. Half Adder

A 9T half adder block used in this paper ensures that high speed, low power and full swing arithmetic can be achieved with this design. As shown in Fig. 3, the topology uses a 5T AND gate for carry generation while the sum generation unit comprises of a 4T XOR gate. The smaller power dissipation along with an improved delay characteristic can be achieved by using the smaller transistor count which ensures a compact design. The full swing output logic realization enables the topologies to be used in cascaded arrangements efficiently without the need of any additional swing restoring buffer units.

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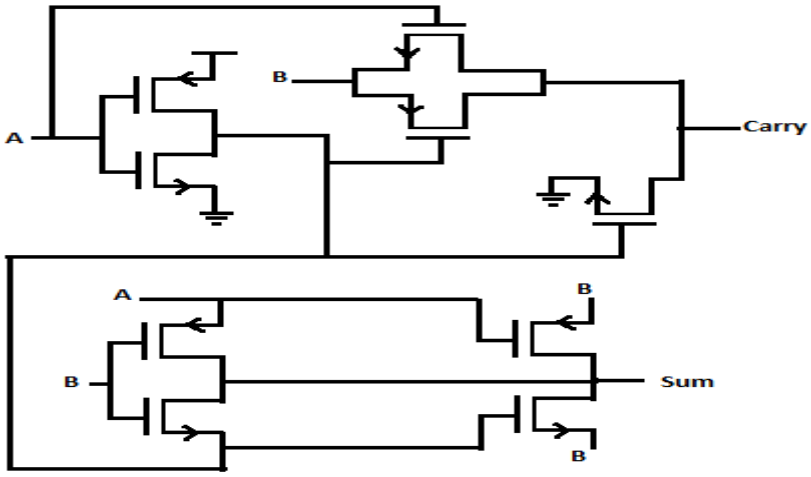

Fig. 4 Half Adder design

C. Full Adder

The speed of a multiplier block is essentially limited due to the latency introduced by the adder assembly incorporated in it for adding the partial products. The use of conventional adder architectures for realizing these long adder chains would not suffice the need of high speed computing of the modern day signal processors because of the large propagation delay and high power consumption associated with them [ ]. Hence there is a need to use new full adder architectures that could ensure high speed and low power arithmetic [ ]. The 14T topology [ ], presented in Fig. 6,is basically a multiplexer based architecture that ensures full swing output voltages at both sum and carry-out terminals. The compact design and smaller transistor count associated with this topology provides significant improvement in the performance of the adder chains embedded in the multiplier. The inherent full swing based adder architecture also eliminates the need of additional swing restoring buffer units and is suitable for cascaded arrangements (as carry save adder blocks as used in this work). The low power dissipation associated with the adder topology essentially reduces the overall power consumption of the multiplier unit and ensures a power efficient high speed computing.

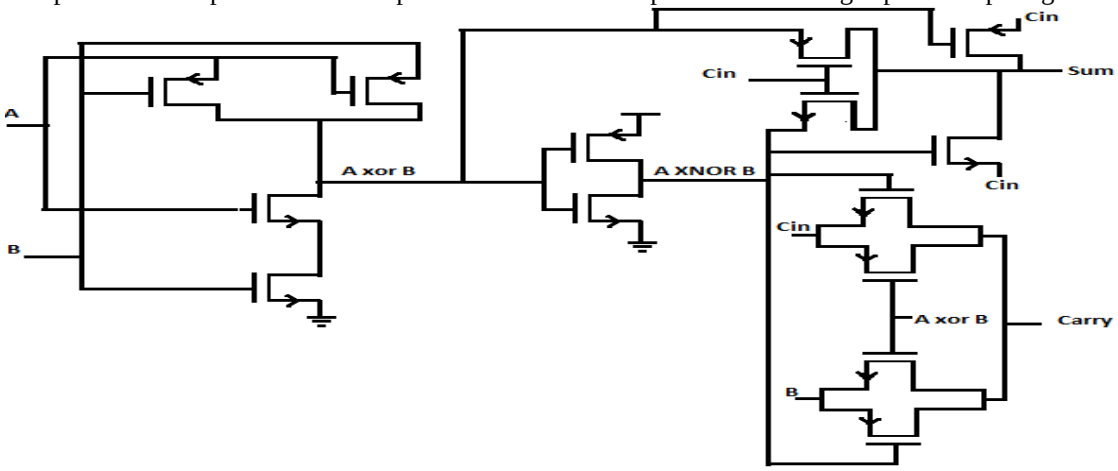

Fig. 5 Full Adder design

D. 2-bit Vedic Multiplier Architecture

The UT based 2-bit Vedic multiplier presented in this work is designed with the use of four AND gates for partial product generation and two half adders to realize the required addition process. The overall propagation delay associated with the design can be calculated as one AND gate delay (because all the AND gates are used for a parallel computation of the partial products) plus two half adder delays. The overall performance of the multiplier is improved because of the high speed adder architectures and the modified AND gate topology, significantly. The topology, shown in Fig. 6, is a 38T design.

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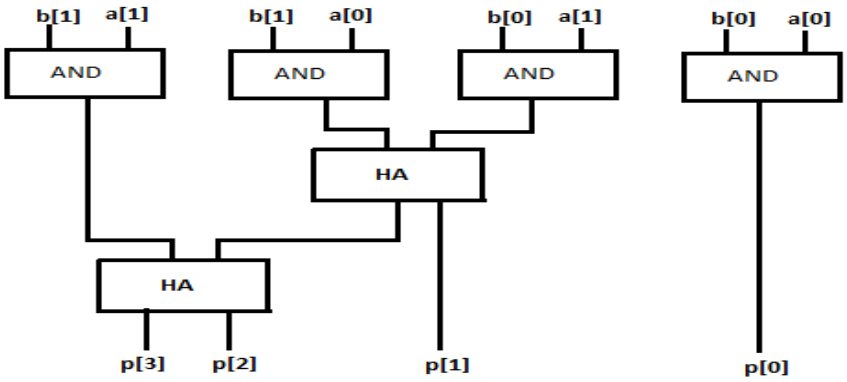

Fig. 6 UT based 2-bit Multiplier Architecture

E. 4-bit Vedic Multiplier Architecture

4-bit binary multiplier based on the Vedic mathematics can be realized using the Urdhva Tiryakbhyam sutra as explained in the line diagram of Fig. 2. All the partial products are generated using a chain of AND gates. The 4-bit binary multiplier can be realized using 2-bit multiplier method. . The paper proposes a novel architecture to implement such a design. This UT based architecture, as shown in Fig. 7, uses four 2×2 Vedic multiplier units which ensure a parallel computing approach. Several adder blocks are incorporated in the proposed architecture for addition of the intermediate results generated from the 2-bit multiplier blocks. In this architecture, two 4-bit carry save adder arrangements and one 4-bit vector merging adder are used. The compactness of the design can be incorporated by reducing the hardware requirement; hence the proposed topology ensures an improved performance. The use of high speed and power efficient adder units also provides a significant improvement in the propagation delay and the power dissipation. After one 2-bit Vedic multiplier delay, the least significant two bits of the output are stable whereas the most significant bit of the result is obtained after a larger delay. The exact propagation delay can be calculated as one 2-bit multiplier delay plus two full adder delays (due to the Carry Save MSB. The ripple carry adder is realized with an assembly of four full adders (14T).

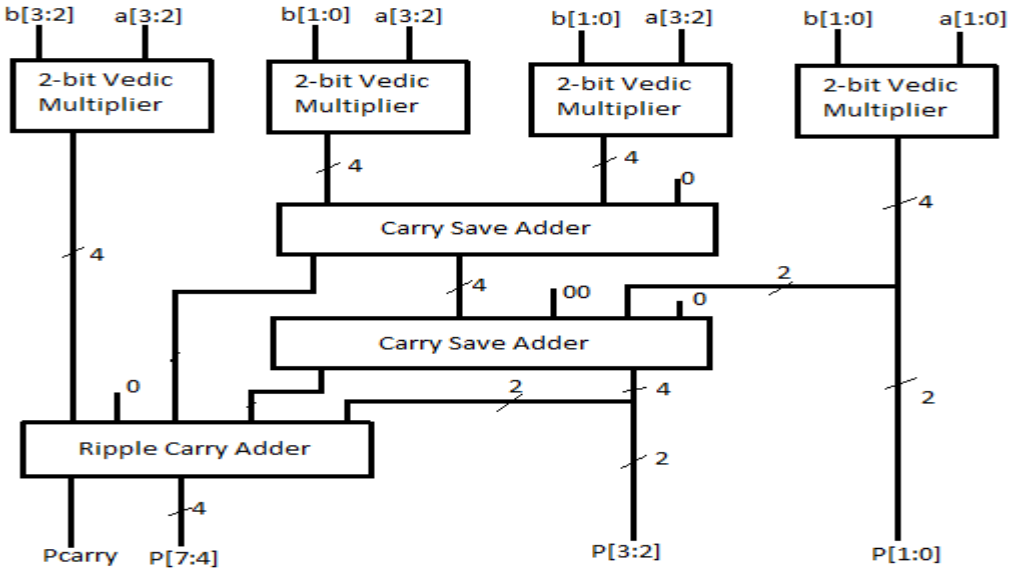

Fig. 7 Design of 4-bit multiplier

F. 8-bit Vedic Multiplier Architecture

The UT based 8-bit Vedic multiplier presented in this work is as shown in Fig. 8.Design is implemented with four 4×4 multiplier blocks and several adder to realize the proposed topology. The design, presented in Fig.8, is a carry save architecture based on the UT sutra for improvement in overall speed of the topology. Two 8-bit inputs A [7:0] and B [7:0] are multiplied to generate a 16-bit output P [15-0]. The latency is reduced by using adder blocks in the design

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which are used in a carry save arrangement. The overall propagation delay of the architecture can be estimated as one 4×4 multiplier delay, full adder delays and the delay introduced by the 8-bit ripple carry adder in the final addition stage. The transistor count associated with this design is reduced; however the hardware complexity is justified as it results in an improved performance. The 4-bit multipliers used in the proposed architecture are UT based 4-bit Vedic multipliers as shown in Fig. 6. It can be seen in Fig. 7 that some of the inputs to the carry save adder blocks are given as zero so that uniform bit-lengths for all the inputs to a particular carry save adder stage can be achieved.

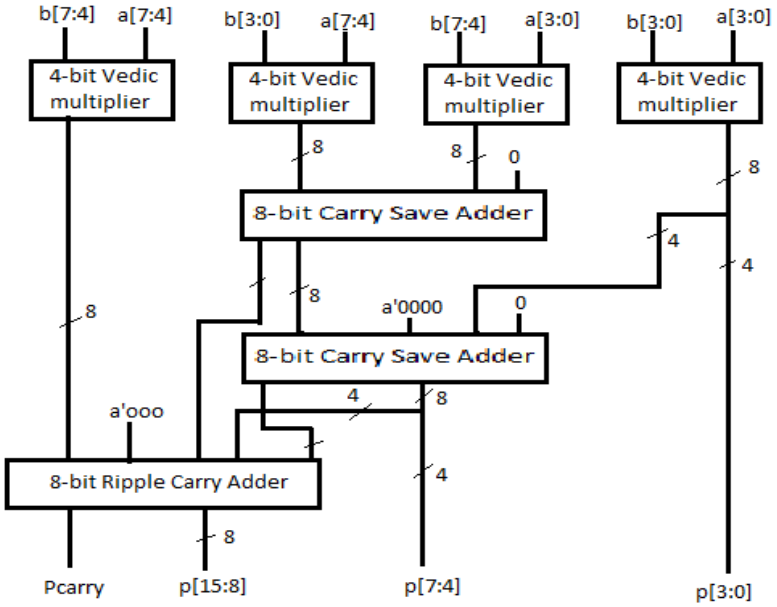

Fig. 8 Design of 8-bit multiplier based on UT sutra

IV. PERFORMANCE ANALYSIS

Performance analysis of the multiplier topologies presented in this paper is performed using the Tanner EDA tool, in 22nm CMOS process technology. The schematics views of the topologies are available at a power supply of 0.4 volt, to analyze the power consumption and overall operating speed. The results obtained are compared between different architectures and the proposed architectures. The results are given in TABLE I-III. TABLE I gives the transistor count associated with the topologies. The use of modified designs for the AND gate ,the half adder and the full adder units provides the overall reduction in area of the multiplier architectures as these topologies utilize less number of transistors as opposed to the conventional designs.. TABLE II lists the propagation delays and power consumptions associated with the proposed designs, both for the schematic.

TABLE I. Transistor Count and Layout Area

Name of the topology	**Transistor count**
4-bit Multiplier of [4]	320
4-bit Multiplier of proposed Multiplier	320
8-bit Multiplier of [4]	1648
8-bit Multiplier of proposed Multiplier	1616

A comparative analysis of propagation delays and power dissipation of different existing 8-bit multiplier architectures reported in the literature with the proposed architecture is presented in TABLE III. The comparison indicates that with

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respect to the different existing multiplier algorithms and architectures, the proposed design offers improved speed at considerably smaller power consumption with 0.4 volt power supply.

TABLE II. Propagation Delay and Power Consumption of different multiplier topologies

Name of the topology	Propagation Delay (in ns)	Power Consumption (in µW)
4-bit Multiplier of [4]	0.268	0.842
4-bit Multiplier of proposed Multiplier	0.019	0.134
8-bit Multiplier of [4]	0.635	7.460
8-bit Multiplier of proposed Multiplier	0.408	0.776

TABLE III. Performance Comparison

Name of the topology	Power Supply in V	Propagation Delay (in ns)	Power Consumption (in µW)
Proposed 8-bit Multiplier	0.4	0.408	0.776
[4]	1	0.635	7.460
[6]	--	21.5	--
[7]	--	22.216	--
[12]	--	18.532	--
[13]	2.5 to 5	14.13sec	9.386e-2

V.CONCLUSION

The paper presents new topologies for 4-bit and 8-bit multipliers based on UT sutra of Vedic mathematics. The topologies are realized in 22 nm CMOS process technology in Tanner EDA tool and the performance analysis is performed using several test inputs with a power supply of 0.4 Volt. The multiplier designs proposed in this paper provides improvement in propagation speed and power consumption and the improvement in performance is achieved due to the new UT based architecture with fewer number of adder units. The designs provide less power consumption and high speed computing with the use of low power and high speed adder blocks.

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