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Design of Low Power Dual Dynamic Node Hybrid Flip-Flop with a Forced nMOS Circuit

Jyothi Jacob[1], Muhamad Salih[2]

PG Scholar [VLSI & ES], Dept. of ECE, Government Engineering College, Idukki, Kerala, India[1]

Assistant Professor, Dept. of ECE, Government Engineering College, Idukki, Kerala, India[2]

ABSTRACT: In this paper a new dual dynamic node hybrid flip-flopwith a forced nMOS circuit is introduced. In the proposed design inverters are replaced by forced nMOS inverters which help to reduce the leakage power and thus the total power consumption. This proposed design presents a power efficient method to incorporate logic functions to reduce pipeline overhead. This would be a good component to be included in VLSI standard cell library for low power applications. Flip-Flop topologies like Hybrid Latch Flip-Flop(HLFF), Semi-Dynamic Flip-Flop(SDFF), Cross Charge Control Flip-Flop(XCFF),Dual Dynamic Node Hybrid Flip-Flop(DDFF) and Proposed Flip-Flop were compared with Cadence tool in Generic Process Design Kit(GPDK) 180 nm CMOS technology. Comparisons show that the power consumption is reduced without degradation in delay compared to other topologies. The performance improvements shows the proposed design is suited for modern high performance applications where power consumption is a major concern.

KEYWORDS: Embedded logic, delay, leakage power, flip-flop, power consumption, forced nMOS

I.INTRODUCTION

Over the past decade, power consumption of VLSI chips has constantly been increasing. The trends in VLSI technology scaling in the last few years show that the number of on chip transistors is increasing every year. Operation frequency of VLSI systems is also increasing. Although capacitances and supply voltages are scaled down, meanwhile power consumption of the VLSI chips is increasing continuously. On the other hand, cooling systems cannot improve as fast as the power consumption increases. Therefore in the very close, future chips are expected to have limitations of cooling system and solving this problem will be expensive and inefficient. This necessitates the design of low power circuits.

A cell library includes a number of cells with different functionalities, where each cell may be available in several sizes and with different driving capability. Two central categories of cells included in cell libraries are flip-flops and latches. These are extremely important circuit elements in any synchronous VLSI chip. They are not only responsible for correct timing, functionality and performance of the chips but also their clocked devices consume a significant portion of the total active power. Based on the comparison of the power breakdown for different elements in VLSI chips,latches and flip-flops are the major source of the power consumption in synchronous systems.Latches and flip-flops have a direct impact on power consumption and speed of VLSI systems. Therefore study on low-power and high performance latches and flip-flops is inevitable.

Extensive works has been done to improve the performance of flip-flops in past few years [7-12]. In this paper a new low power dual dynamic node hybrid flip with a forced nMOS circuit is proposed. Forced nMOS circuit help to reduce the leakage power and thus the total power consumption. For the comparison purpose flip-flops like HLFF, SDFF, XCFF, DDFF and proposed flip-flop are designed and simulated in cadence 180 nm CMOS technology. Performance comparison of proposed flip-flop shows that there is 35% power reduction compared to DDFF which is a modern high performance circuit. This proposed flip-flop with embedded logic is a power efficient method to reduce pipeline overhead. It is possible to scale down the supplyvoltage of proposed flip-flop from 1.8 V to 1.2 V for further power reduction.

The rest of this paper is divided as follows.SectionII, describes existing high performance flip-flop topologies and discusses the disadvantages of the existing flip-flop topologies and challenges in achieving high performance. In Section III, architecture of proposed flip-flop and its operation are provided. Section IV, details the design and working

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principle of the proposed flip-flop while embedding logic functions. In Section V, results on various performancecomparison including power and delay are given. In thissection transient response and layout of the proposed circuit is also given. Finally Section VI, conclude with the improvements of the proposed flip-flop designs over the existing modern high performance designs.

II.RELATED WORKS

Many flip-flops have been reported in the past years.They can be grouped as static and dynamic structures. Static structures have high D-Q delay even though they low power consumption, so they remain as a low power solution when speed not a problem. These designs are not suited for modern high speed, low power applications. So dynamicstructures suited for modern high performance applications are analyzed. Dynamic flip-flop structures can be purely dynamic or pseudo dynamic. Pseudo dynamic structure has an internal precharge structure and static output deserves special consideration because of their distinctive performance improvements. They consist of dynamic front end and static output, thus called pseudo dynamic structures. HLFF and SDFF come under this category. They perform latching operation during the overlap period of clock. Their structures are shown in Figure 1, 2 and working is explained in [1] and [2] respectively. In these structures power consumption is high because of large clock load as well as large pre charge capacitance. SDFF is faster than HLFF which has low power consumption. Longer stack of nMOS transistors at the output makes HLFF slower. HLFF also has large hold time requirement which makes integration of HLFF to complex circuits difficult. This is also inefficient in embedding logic.

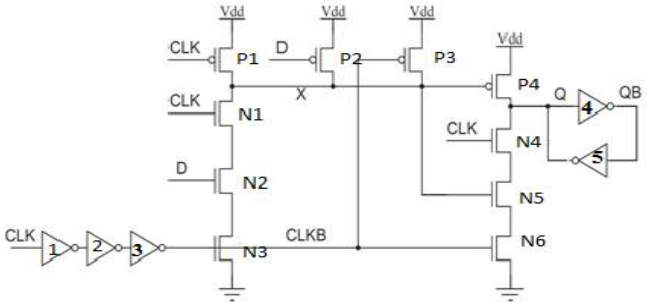

Figure 1: HLFF

The common drawback of conventional design is large precharge capacitance since both output pull-up and pull-down transistors are driven by same precharge node. In XCFF power dissipation is reduced by splitting the dynamic node into two, each separately driving output pull-up and pull-down transistors. Structure of XCFF is shown in Figure 3 and its working is explained in [3].Here only one of the two dynamic nodes is switched during one clock cycle which helps to reduce power consumption without degradation in speed. The clock driving load is also low in case of XCFF. The major drawback of XCFF is redundant precharge at node X1 and X2 for data patterns containing more 0s and 1s. Conditional shut off mechanism provided by inverters 3 and 4 increases hold time. A low to high transition in clock

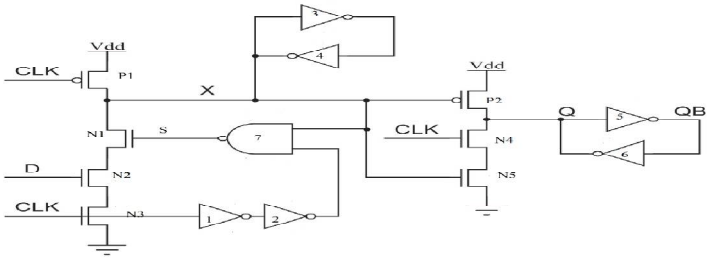

Figure 2: SDFF

when data is held low can cause charge sharing at node X1. This will cause errors in output if the inverter pair 1 and 2 is not properly skewed. This structure is not efficient in embedding logic because of charge sharing.

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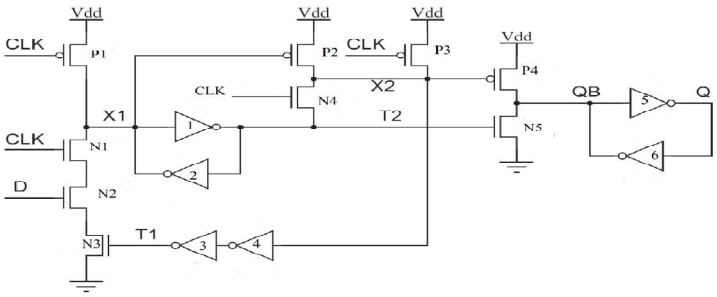

Figure 3: XCFF

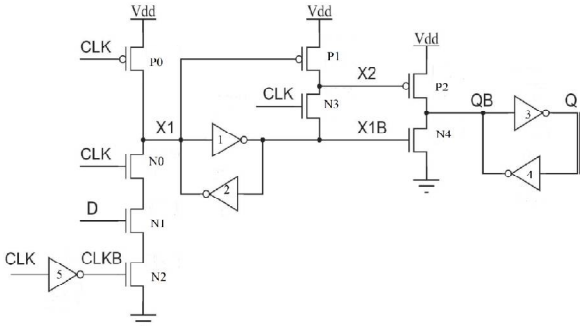

Figure 4: DDFF

Structure of DDFF is shown in Figure 4 and its working is explained in [4]. Node X1 is pseudo dynamic with inverter pair 1 and 2 acting as keeper. Node X2 is purely dynamic. In the front end an unconditional shut off mechanism is used while in case of XCFF it is conditional. Inverter pair 1 and 2 is carefully skewed to avoid charge sharing. DDFFis efficient in embedding logic.

III.ARCHITECTURE OF PROPOSED FLIP-FLOP

The proposed flip-flop is slight modification of DDFF and power consumption is lower than DDFF. In this the inverters are replaced by forced nMOS circuit which helps to reduce power consumption. Static inverter consists of a single nMOS and pMOS transistor while forced nMOS inverter consists of one pMOS and two nMOS transistors. The added nMOS increases the delay slightly but it help to reduce power consumption to a large extend. The structure of proposed flip-flop is shown in Figure 5.

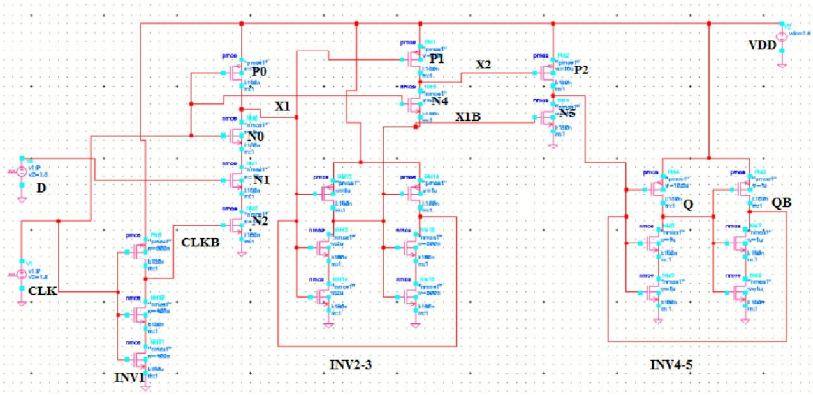

Figure 5: Proposed Flip-Flop

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The two phases of operation of flip-flops are precharge and evaluation phase. During the precharge phase clock(CLK) is low and in the evaluation phase CLK is high. Data (D) is latched during 1-1 overlap of clock during the evaluation phase. Working of the proposed circuit is explained by referring to Figure 5.

If D is high before the precharge phase node X1 will discharge through N0-2.This switches the state of the cross coupled inverter pair INV2-3 causing node X1B to go high and output QB to discharge through N5. The low level at the node X1 is retained by the inverter pair INV2-3 for the rest of the evaluation phase where no latching occurs. Thus, node X2 is held high throughout the evaluation period by the pMOS transistor P1. As the CLK falls low, the circuit enters the precharge phase and node X1 is pulled high through P0, switching the state of INV2-3. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV4-5.

If D is zero before the evaluation period, node X1 remains high and node X2 is pulled low through N4 as the CLK goes high. Thus, node QB is charged high through P2 and N4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high and X2 stores the charge dynamically. The architecture exhibits negative setup time because the short transparency period defined by the 1-1overlap CLK of and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low[5]. By proper sizing of INV1 hold time and setup time of proposed circuit can be maintained. Proper design is obtained by controlling the beta ratio[6] of inverters.

IV.EMBEDDING LOGIC TO PROPOSED FLIP-FLOP

By embedding logic functions N input logic function canbe realized by pull down network consisting of N transistors. Sequential circuit consists of combinational circuit and flip-flop. Compared to the discrete combination of N a static gate and a flip-flop, this embedded structure offers a very fast and small implementation. SDFF and DDFF are efficient in embedding logic. SDFF is not a good solution for embedding logic as far as power consumption is concerned. Proposed flip-flop is efficient in embedding logic and power consumption is also low compared to DDFF and SDFF.

Proposed flip-flop embedding NAND and NOR logic are shown in Figure 6 and 7 respectively. 2-input NAND logic consists of nMOS transistors in series and NOR logic consist of nMOS transistors in parallel. A, B are the inputs given to the circuit.

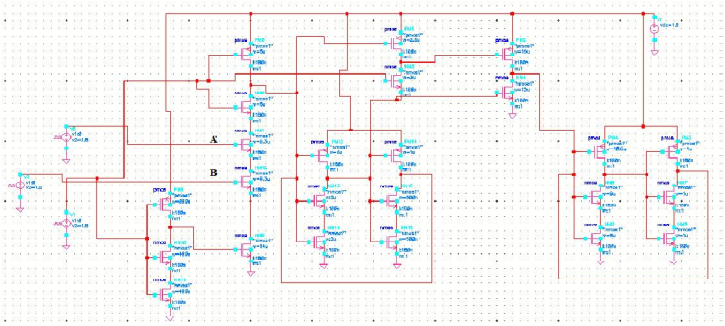

Figure 6: Proposed flip-flop embedding NAND

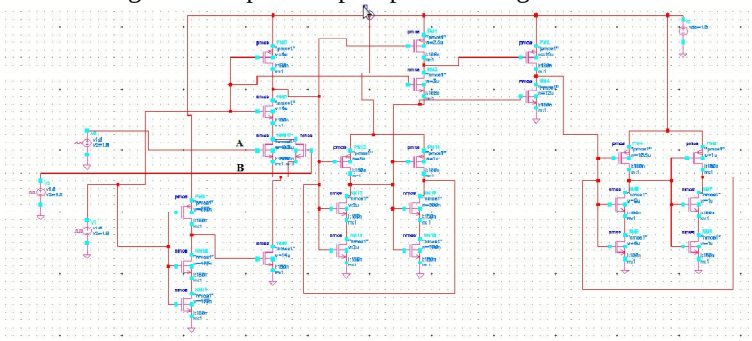

Figure 7: Proposed flip-flop embedding NOR

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V. PERFORMANCE ANALYSIS

To compare the performance of proposed flip-flop with existing topologies like HLFF, SDFF, XCFF and DDFF all the flip-flops were designed and simulated in cadence 180 nm technology. Simulations were carried out at a frequency of 2 GHz and supply voltage of 1.8 V. The transient response of proposed flip-flop, proposed flip-flop-NAND and proposed flip-flop-NOR are shown in Figure 8, 9 and 10 respectively.

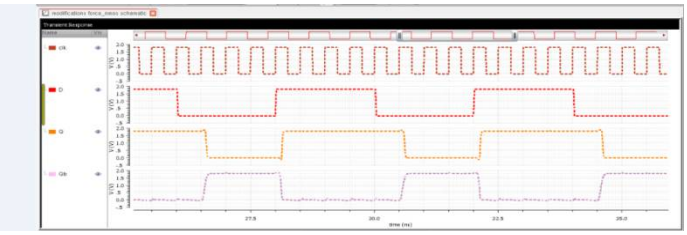

Figure 8: Transient response of proposed flip-flop

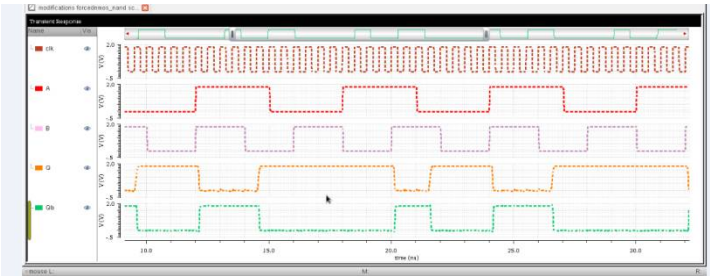

Figure 9: Transient response of proposed flip-flop-NAND

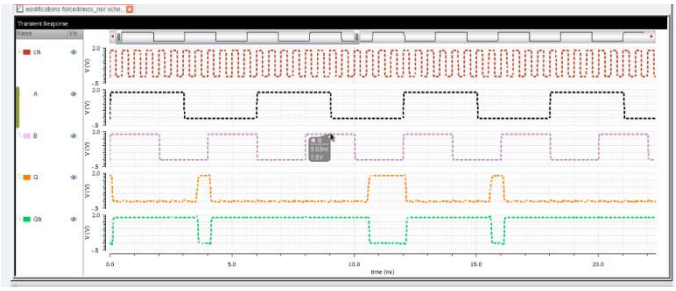

Figure 10: Transient response of proposed flip-flop-NOR

Power consumption and delay of various topologies are shown in Table I and II respectively. Here the clock frequency is 2 GHz and supply voltage is 1.8 V.

Table I: Power and delay comparisons of flip-flops

Type	Power(W)	Delay(s)
HLFF	2.4 μ	158 p
SDFF	2.7 μ	90 p
XCFF	1.3 μ	122 p
DDFF	1.17 μ	121 p
Proposed FF	866.5 n	121.3 p

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Table II: Power and delay comparisons of embedded logic flip-flops

Type	NAND		NOR	
	P(W)	D(s)	P(W)	D(s)
SDFF	2.3 μ	132 p	2.9 μ	103 p
DDFF	1 μ	123 p	1.6 μ	109 p
Pro FF	602.1 n	130 p	1μ	116 p

Power consumption for clock frequencies from .5 GHz to 5 GHz is shown in Figure 11. Here also supply voltage is 1.8 V. It is found that as clock frequency increases power consumption increases. The proposed flip-flop works efficiently at high frequencies. This indicates that it is suitable for modern high speed applications.

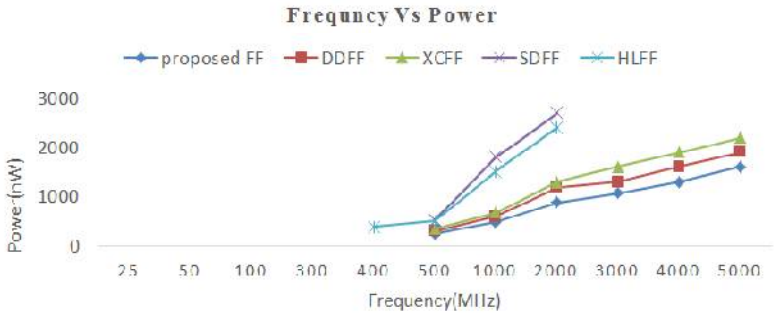

Figure 11: Frequency versus Power consumption graph

Power consumption for supply voltage from 1.8 V to 1.2 V is shown in Figure 12. Here the clock frequency used is 2 GHz. It is found that as supply voltage decreases power consumption decreases. In case of proposed flip-flop supply voltage can be scaled down to 1.2 V to reduce power consumption.Layout of proposed flip-flop is shown in Figure 13.

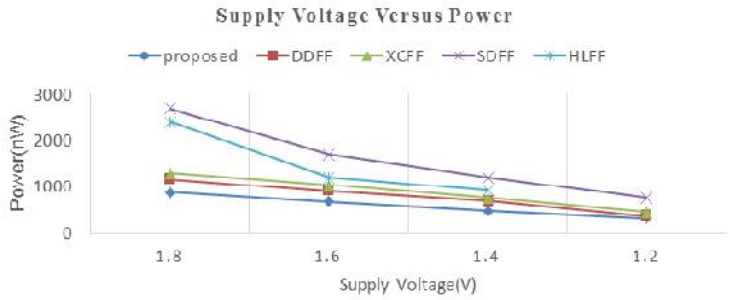

Figure 11: Supply Voltage versus Power consumption graph

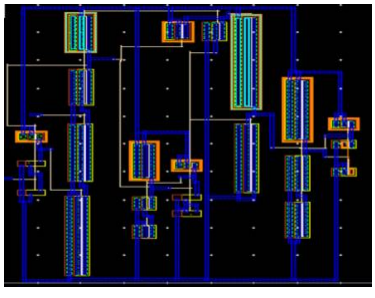

Figure 13: Layout of proposed flip-flop

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VI.CONCLUSION

A new dual dynamic node hybrid flip-flop with a forced nMOS circuit is proposed. This circuit is efficient in terms ofdelay and power consumption compared to other topologies. This is also good in embedding logic functions. The power consumption of proposed flip flop is 866.5 nW and delay is 121.3 ps at clock frequency of 2 GHz and supply voltage of 1.8 V. The proposed circuit works up to a frequency of 5 GHz and supply voltage can be scaled down to 1.2 V without affecting the functionality of circuit. While embedding logic function the power consumption is 602.1 nW for NAND and 1 µW for NOR logic, delay is 130 ps for NAND and 116 ps for NOR logic.This flip-flop can be added as a component in standard cell library and can be used for implementation of low power counters and shift registers.It is also possible to incorporate reset functionality to proposed flip-flop for further improvements.

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