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Switch Fault Diagnosis and Rectification in Buck Converter

Sneha Lal .A¹, Suraj Zachariah Manesh²

PG Student [Power Electronics], Dept. of EEE, Toc H Institute of Science and Technology, Ernakulam, Kerala, India¹

PG Student [Embedded Systems], Dept. of ECE, SRM University, Chennai, Tamil Nadu, India²

ABSTRACT: In this paper, a fault tolerant operation of a single switch dc-dc buck converter under switch failure is proposed. The fault tolerant operation of a power system can be performed in three steps: fault detection, identification and remedial action. In case of a switch failure, it is essential to identify the fault and rectify it as soon as possible to avoid its propagation through the system. This proposed paper can help to distinguish open and short circuit fault using a fault detection algorithm. The inductor current is taken as the reference. By comparing the PWM signal and the inductor current, the fault is detected. An auxiliary switch is needed for converter reconfiguration in post fault operation.

KEYWORDS: DC-DC converter, diagnosis, fault tolerance, PWM signal, fault detection algorithm.

I. INTRODUCTION

The dc-dc converters are widely used in many industrial applications such as aerospace, ships, electric vehicles and renewable energy power systems. From the application point of view, reliability is one of the important factor that has to be considered nowadays. Reliability is the ability of an item to perform the required function under stated conditions for a certain period of time, which is often measured by probability of survival and failure rate. Therefore reliability in these embedded systems and in safety critical applications has been improved with the integration of fault diagnosis and fault tolerant architectures. Fault tolerance in a power converter needs three steps: fault detection, fault identification and remedial actions. The first two steps are used to find the location and nature of fault. In remedial actions, first the faulty device is isolated if needed and then reconfigure the converter to guarantee the service continuity.

In most dc-dc converters, the critical elements are aluminum electrolytic capacitors and semiconductors. About 60% of the converter faults are due to electrolytic capacitors. Semi-converter faults and soldering joints failure contributes about 34%. The inductive elements constitute about 8% of the total converter faults and diodes constitute about 5%.

Working outside the safe operating area leads power semiconductors to damage. The main failure causes are, a)fault current either over current; b)short circuit current or earth fault current; c)over voltage; d)over temperature; e)cosmic radiations. Other problems may arise because of the driver of the power semiconductors: malfunctioning of the driver board, auxiliary power supply failure or large dv/dt disturbances. As a result, faults can be classified into five main types: 1) single switch short circuit 2) phase leg short circuit 3) single switch open circuit 4) single phase open circuit 5) intermittent gate mis firing. Several diagnostic methods are used to find out the faults. Once the fault is detected and isolated or online repair is implemented, the system can continue to operate safely and fault tolerant operation is implemented.

In a dc-dc converter system, open and short circuit faults are most common. This paper deals with the open and short circuit fault in a single switch dc-dc buck converter. Here the fault is first detected through a fault detection algorithm (FDA). After the detection, the circuit is reconfigured with another auxiliary switch and the operation is continued.

The main disadvantage of many fault tolerant systems is that, for fault detection, many additional sensors and auxiliary parts like tertiary winding (full bridge converters) [2] are used. And above all these, for fault rectification, many



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additional switches, legs(for H-bridge) are used [3]. All these will increase the losses, size, cost and complexity of the system. Thereby the performance of system is reduced.

The objective of this project is to:

1) Effectively find out the fault with reduced number of sensors

2) To rectify the fault within minimum time and with reduced number of switches

3) To ensure the continuous operation of the circuit by rectifying the fault.

II. PROPOSED TOPOLOGY

The Fig 1 shows the fault tolerant circuit of a buck converter. This circuit consists of two switches, one main switch and other an auxiliary switch. The auxiliary switch is connected in parallel with the main switch. A fuse unit is incorporated in the circuit to isolate the main switch during the faulty condition from the circuit. When a fault occurs in the circuit, the operation is shifted from the main switch to the auxiliary switch. There by the operation is continued.

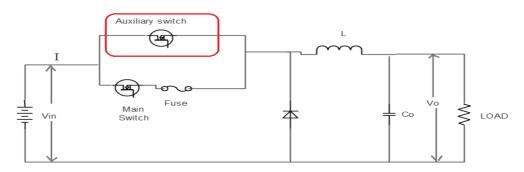


Fig. 1 Fault tolerant Buck Converter

III. SIMULATION DIAGRAM

The simulation parameters and values of buck converter are shown in the following table.

Table. 1 Simulation Parameters and Values of Buck Converter

SYMBOL	PARAMETER	VALUE
V_{in}	Input voltage	14V
Vout	Output voltage	6V
L_o	Inductor	$190\mu H$
C_o	Filter capacitor	$170\mu F$

Fig 2 shows the simulation diagram of the buck converter. A main switch and an auxiliary switch are shown in the diagram. These switches are connected in parallel, so that when the main switch become faulty, the operation is continued with the help of auxiliary switch. The fault is detected using a FDA(Fault Detection Algorithm), in which the slope of inductor current is taken as the reference. The slope is then compared with the PWM signal and fault is detected. After fault detection, the operation is changed from main switch to auxiliary switch. There by the operation is continued and the fault is rectified.



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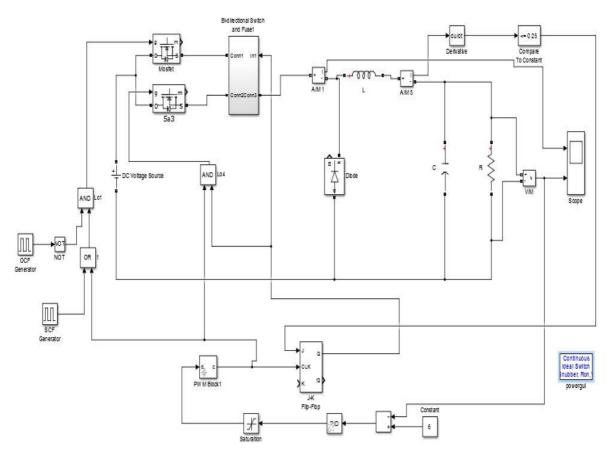


Fig. 2. Buck Converter Closed Circuit

Fig 3 shows the subsystem of the system. It contains two switches, connected in parallel. These together act as a fuse unit or a relay unit which is used to isolate the faulty switch from the main circuit and the auxiliary switch is introduced into the circuit instead of main switch.

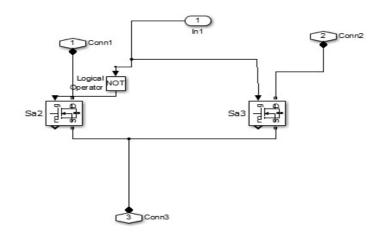


Fig. 3. Buck Converter-Sub System



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IV. SIMULATION RESULTS

Simulation results will discuss how the fault tolerant circuit works in open and short circuit fault condition. The fault is created using a signal generator. First the open circuit fault condition is discussed. In both open and short circuit condition, the operation mainly involves three steps: fault detection, fault identification and fault rectification.

OPEN CIRCUIT CONDITION:

Fault is generated using a pulse generator which is shown in Fig 4. To create an Open Circuit Fault, the gate signal is made to zero. So that, the switch is in zero state or non-conducting state. The fault created is based on the idea that either the open circuit fault or the short circuit fault switch can be found in any converter system.

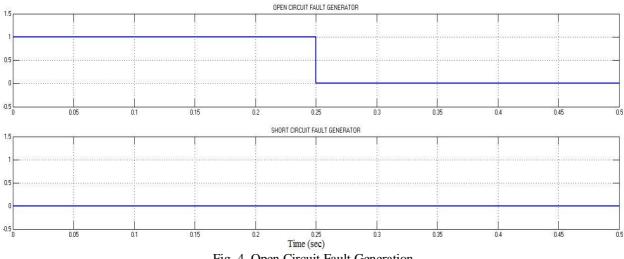


Fig. 4. Open Circuit Fault Generation

Fig 5 shows the condition of circuit during open circuit fault. In-order to create an open circuit condition, the gate signals to the switch is blocked. So it acts as an open circuit condition. In this state, the inductor current goes on decreasing, which is shown in the waveform. For obtaining the sign of inductor current it is compared with a threshold value (25000). When slope of inductor current becomes less than or equal to the threshold value (25000), the output from block becomes high. This high output is given as the input to the J-K flip-flop. The J-K flip-flop is used to produce a continuous high output. The PWM signal is given as the clock to the J-K flip-flop. During the faulty condition, both the J and clock becomes high. So the output Q becomes high, and thus the fault is detected, which is shown in the waveform. This high pulse is given to the subsystem, thereby the main switch is isolated and the auxiliary switch is introduced into the circuit.



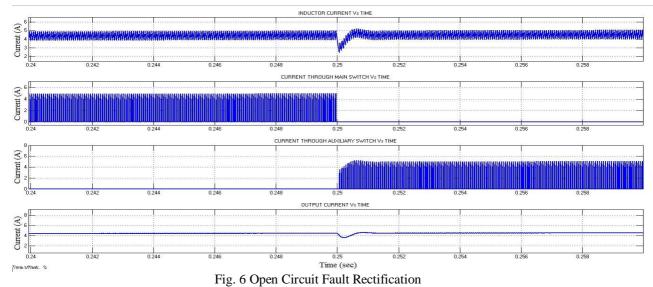
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering An ISO 3297: 2007 Certified Organization Vol. 5, Special Issue 3, March 2016 National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE'16) Organized by Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India On 17th & 18th March 2016 INDUCTOR CURRENT VS TIME (A) Current 2 lidt LESS THAN 2500 PWM SIGNAL Vs TIME MM 0.249



FAULT DETECTED

Fig. 5. Open Circuit Fault Detection

Fig 6 shows the rectification of fault in the converter. Open circuit fault is generated at time t=0.25 sec. The Fault Detection Algorithm detects the fault. After fault detection, the faulty switch is isolated from the circuit by blocking the control signals to the faulty switch. The fault is rectified through an auxiliary switch connected in parallel with the main switch. The operation is continued by giving gate signals to the auxiliary switch. The change of operation from main switch to the auxiliary switch is shown in the waveform.



SHORT CIRCUIT CONDITION:

Fig 7 shows the generation of Short Circuit Fault. In-order to create a Short Circuit Fault, a continuous high signal is given to the switch. So, the switch will always be in the conducting state. This high state of the switch represents the short circuit condition of the switch.



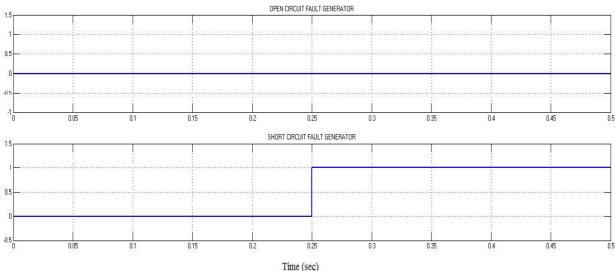
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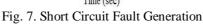


Fig 8 shows the condition of circuit during short circuit condition. In-order to create a short circuit condition we are giving a high gate signals to the switch. In this state, the inductor current goes on increasing and later the inductor current become constant, which is shown in the waveform. For obtaining the sign of inductor current, it is compared with a threshold value. When slope of inductor current becomes less than or equal to the threshold value(25000), the output from block becomes high. This high output is given as the input to the J-K flip-flop. The PWM signal is given as the clock to the J-K flip-flop. During the faulty condition, both the J and clock becomes high. So the output Q becomes high, and thus the fault is detected, which is shown in the waveform. This high pulse is given to the subsystem, thereby the main switch is isolated and the auxiliary switch is introduced into the circuit.

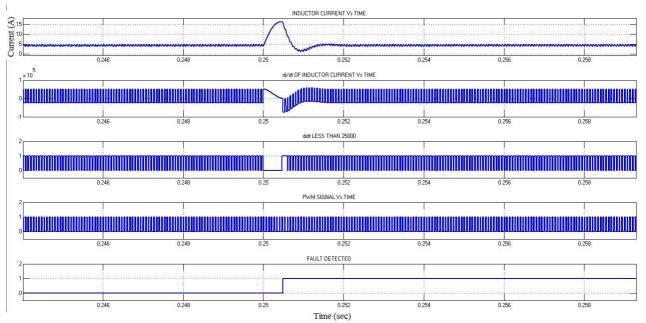


Fig. 8. Short Circuit Fault Detection



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The short circuit fault rectification of the buck converter is shown in the Fig 9. The fault is detected using Fault Detection Algorithm. After the fault detection, the faulty switch is isolated from the circuit and operation is continued using an auxiliary switch. At time t=0.25 sec, there is a disturbance in the output current and voltage. These disturbances are due to the change in operation from the main switch to the auxiliary switch.

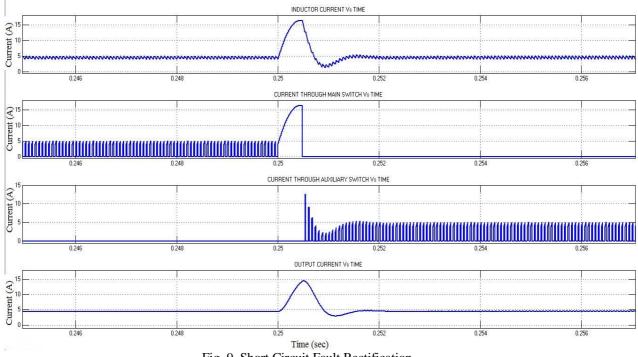


Fig. 9. Short Circuit Fault Rectification

V. CONCLUSION

This paper has proposed a FT operation of a single switch dc-dc buck converter for open and short circuit switch failures. The proposed FDA can identify and detect the type of fault very effectively. The inductor current and the PWM signal are the only parameters used to detect the fault. The simulation is also carried out. The open and short circuit faults are detected effectively. These faults are isolated and rectified as fast as possible. Operation is continued using an auxiliary switch connected in parallel with main switch.

REFERENCES

- [1] Ehsan Jamshidpour, Philippe Poure, Eskandar Gholipour, "Single-Switch DC-DC Converter With Fault-Tolerant Capability Under Open and Short- Circuit Switch Failures", IEEE transactions on power electronics, vol. 30, no. 5, May 2015
- [2] X. Pei, S. Nie, and Y. Kang, "Switch short-circuit fault diagnosis and remedial strategy for full-bridge dc-dc converters," IEEE Trans. Power Electron.
- [3] K. Ambusaidi, V. Pickert, and B. Zahawi, "New circuit topology for fault tolerant H-bridge dc-dc converter," IEEE Trans. Power Electron ., vol. 25, no. 6, pp. 1509-1516, Jun. 2010.
- [4] E. Jamshidpour, B. Nahid-Mobarakeh, P. Poure, S. Pierfederici, F. Meibody-Tabar, and S. S. Saadate, "Distributed active resonance suppression in hybrid dc power systems under unbalanced load conditions,"IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1833-1842, Apr. 2013.
- [5] H.Wang, M. Liserre, F. Blaabjerg, P. Rimmen, J. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," IEEE J. Emerging Select. Topics Power Electron., vol. 2, no. 1, pp. 97-114, Mar. 2014.
- [6] A. Amaral and A. Cardoso, "On-line fault detection of aluminium electrolytic capacitors, in step-down dc-dc converters, using input current and output voltage ripple," IET Power Electron., vol. 5, no. 3, pp. 315-322,2012.