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A Novel Technique for Leakage Power Reduction in CMOS VLSI Circuits by using Universal Gates

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ABSTRACT: In the nanometre range design technologies total power dissipation is very important issue in present peripheral devices. In CMOS based VLSI circuits scaling technology is gradually down towards in respect of size and achieving higher operating speeds. In this paper considering this parameter in such a way such that we can control the leakage power. Novel circuit techniques for reduction of current leakage in Universal gate inverter using based CMOS, LECTOR and LCPMOS properties are investigated. The proposed techniques are applied to base CMOS, NAND and NOR inverters and the result are compared with earlier inverter leakage minimization techniques and shows much better response. All low leakage models of inverter are designed and simulated in a tanner tool environment using 45 nm CMOS technology at 5 volt technologies.

KEYWORDS: Average power, sub threshold leakage current, LCPMOS voltage scaling **,** leakage control transistor.

I. INTRODUCTION

Today leakage power has become an increasingly important issue in processor hardware and software design [1]. With the main component of leakage, the sub threshold current, exponentially increasing with decreasing device dimensions [2]. Leakage current is an ever increasing share in the processor power consumption. In 45 nm and below technologies leakage current for 35 -45% is of processor power [3]. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this trend, transistor leakage power has increased exponentially [4]. Leakage Power of CMOS transistors depends on gate length and oxide thickness [5]. The rapid growth in semiconductor technology through the use of deep-submicron process has led the feature size to be shrinking, thereby integrating extremely complex functionally on a single chip [2]. Building low power VLSI system has a emerged as significant performance goal because the fast technology in mobile communication and computation. The advances in battery technology are not commensurate with advance in electronics device [6].

In this paper, a leakage power reduction technique called LCPMOS , a technique to tackle the leakage problem in CMOS circuits using a single additional leakage control transistor. Here a single leakage control within the logic gate for which the gate terminal of leakage control transistor (LCT) is controlled by the output of the circuit itself which increase the resistance of the path from pull down network to ground thereby increasing the resistance from V_{dd} to ground, loading to significant decrease in leakage current. Thereby limits the area and also power dissipation in active state [7]. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantage of each technique is limit the application . Our proposed technique thus providing a new choice to low leakage power VLSI designers. As compared to other techniques the main advantage is that LCPMOS technique does not require any additional control and monitoring circuitry. Another advantage with LCPMOS technique is that it reduces the leakage power to an extent of 91.54%,which is more efficient as compared to other technique . In this paper CMOS design, behind the speed and area of any chip, power dissipation or power consumption was Secondary consideration. But however we are increasing the total number of transistors and clock frequency in a single chip, then power consumption comes in very serious issue. Instantaneous power drawn by any

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chip from the power supply is directly proportional to the multiplication of supply voltage v(t) and supply current I_{dd} (t).[8]

$$\mathbf{P(t) = i_{dd}(t)*v(t)} \quad \mathbf{(1)}$$

Now, total energy consumed over some time interval T is,

$$\mathbf{E} = \int_0^t \boldsymbol{p}(\mathbf{t}).\ \mathbf{dt} \quad \mathbf{(2)}$$

$$\text{Or, } \mathbf{E} = \int_0^t \boldsymbol{i_{dd}(t).v(t)dt}$$

So the average power over this interval is,

$$\mathbf{P_{avg}} = \frac{E}{T} = \frac{1}{T}\int_0^t \boldsymbol{i_{dd}(t).v(t)dt} \quad \mathbf{(3)}$$

The Static power dissipation depends on due to sub-threshold conduction, tunnelling current through gate oxide and leakage through reverse biased diodes. Similarly, dynamic power dissipation depends on due to charging and discharging of load capacitances, "Short circuit" current while both PMOS and NMOS networks are partially "ON".

II. LITERATURE REVIEW

The increase in the transistor leakage current is one of the most important negative side effects of technology scaling. Leakage affects not only the standby and active power consumption, but also the circuit reliability, since it is strongly correlated to the process variations. Leakage current influences circuit performance differently depending on: operating conditions (e.g. standby, active, burn in test), circuit family (e.g. logic or memory), and environmental conditions (e.g. temperature, supply voltage). As the feature size becomes smaller, shorter channel lengths result in increased subthreshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub threshold leakage current because transistors cannot be turned off completely. Since the way designers control subthreshold and gate leakage can change from one technology to another, it is crucial for them to be aware of the impact of the total leakage on the operation of circuits and the techniques that mitigate it [1]

Sub threshold leakage current (I_{sub}) in MOS transistors, which occurs when the gate voltage is below the threshold voltage and mainly, consists of diffusion current. Off-state leakage in present-day devices is usually dominated by this type of leakage. An effect called drain-induced barrier lowering (DIBL) takes place when a high-drain voltage is applied to a short channel device. The source injects carriers into the channel surface (independent of gate voltage). Narrow width of the transistor can also modulate the threshold voltage and the sub threshold current.

$$I_{sub} = \mu_0\, C_{ox}\, \frac{W}{L}\, V^2\, e^{1.8}\, e^{\frac{Vgs - V_T}{nV}} \quad (4)$$

where, μ_0 is the zero bias mobility, Cox is the gate oxide capacitance, and (W/L) represents the width to the length ratio of the leaking MOS device. The variable V in equation 1.1 is the thermal voltage constant, and Vgs represents the gate to the source voltage. The parameter n in equation 1.1 is the sub-threshold swing coefficient given by 1 + (Cd/Cox) with Cd being the depletion layer capacitance of the source/drain junction. One important point about equation (4) is that the sub threshold leakage current is exponentially proportional to (Vgs -VT). Shorter channel length results in lower threshold voltages and increases subthreshold leakage. As temperature increases, subthreshold leakage is also increased. On the other hand, when the well-to-source junction of a MOSFET is reverse biased, there is a body effect that increases the threshold voltage and decreases subthreshold leakage.

Gate oxide tunneling current (Igate) in which tunneling of electrons that can result in leakage when there is a high electric field across a thin gate oxide layer. Electrons may tunnel into the conduction band of the oxide layer; this is called Fowler-Nordheim tunneling. In oxide layers less than 3-4 nm thick, there can also be direct tunneling through the silicon oxide layer. Mechanisms for direct tunneling include electron tunneling in the conduction band, electron tunneling in the valence band, and hole tunneling in the valence band.

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III. DIFFERENT TECHNIQUES

Leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique.

A. Base CMOS Technique:

During Complementary Metal oxide Semiconductor (CMOS) design the circuit topology is complementary push pull it means that both PMOS and NMOS network are contributed in the circuit.

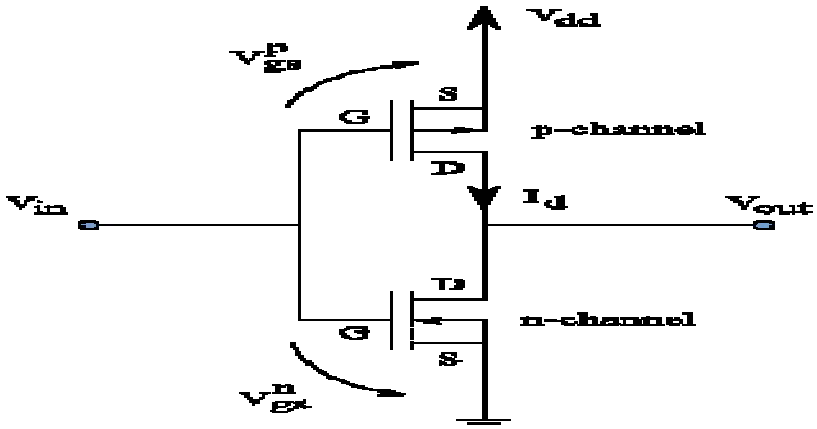

Fig.1: Based CMOS Technique

For static power dissipation we are considering the static CMOS inverter which is shown in figure1. If the input=0, the associated NMOS transistor is OFF and the PMOS transistor is ON. The output voltage is V_{dd} or logic 1.When the input =1 the associated NMOS transistor is ON and the PMOS transistor is OFF. The output voltage is 0 volt. It is seen that one transistor is always OFF when the gate is in either of these logic states. Ideally, no current flows through the off transistor so the power dissipation is zero when the circuit is quiescent. Zero quiescent power dissipation is a principal advantage of CMOS over competing transistor technologies. However, secondary effects including sub-threshold conduction, tunnelling and leakage lead to small amount of static current flowing through the "OFF" transistor. Assuming the leakage current is constant so instantaneous and average power are the same; the static power dissipation is the product of total leakage current and the supply voltage.

$$P_{static} = I_{static} * V_{dd} \quad (4)$$

There is some small static dissipation due to reverse bias leakage between diffusion region and the substrate in addition sub-threshold conduction can contribute to the static dissipation. Now we are introduced a model where we shows that the parasitic diode is shown between n well and substrate. Since parasitic diodes are reverse biased then only leakage current contributes to static power dissipation. The leakage current is described by the diode equation[8].

$$I_o = i_s \left(e^{\frac{qv}{kt}} - 1\right) \quad (5)$$

B. MTCMOS

Multiple threshold voltage CMOS (MTCMOS) is a high –threshold NMOS gating transistor connected between the pull-down network and the ground, and low threshold voltage transistors are used in the gate. The reverse conduction paths exist, which tends the noise margin to reduce or may result complete failure of the gate. [1] The logical function of a gating transistor is similar to that of a sleep transistor. [9]

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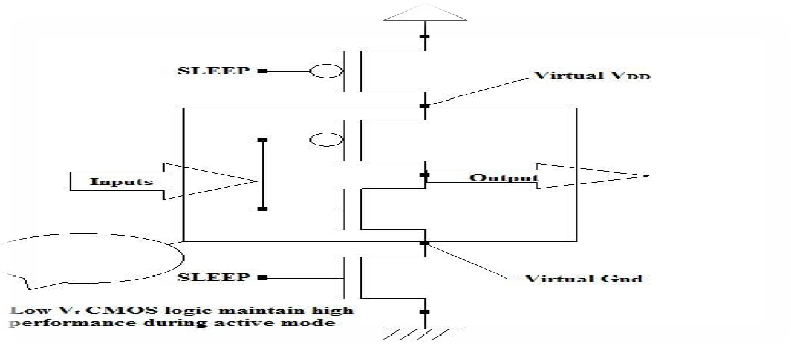

Fig.2: MTCMOS Technique

B. SLEEP Transistor Technique:

This technique is a state-destructive technique which cut off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high sleep transistors between pull-up networks and V_{dd} and pull-down networks and ground while for fast switching speeds, low V_{th} transistors are used in logic circuits [10]. This technique dramatically reduces leakage power during sleep mode. [3]

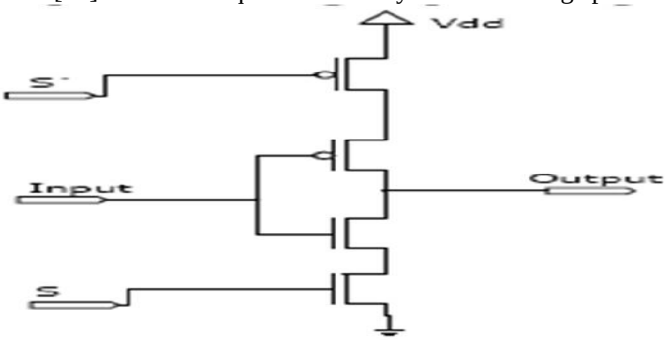

Fig 3: Sleep Transistors Technique

C. LECTOR Technique:

This technique is used for reduction in the leakage power; the assembling of transistors from V_{dd} to ground is the notion behind the LECTOR Technique. In this method, two leakage control transistors are positioned in between the a PMOS (LCT1) added to the pull-up network and a NMOS (LCT2) added to the pull-down network, this implies either one of the LCTs will continuously drives in its near cut-off region. And this effective technique in both idle and active stage of the circuit better leakage reduction in this technique increase the resistance in the path from source to ground, which increase the area of the circuit, one of the most important constraint in the design of VLSI circuits.[8]

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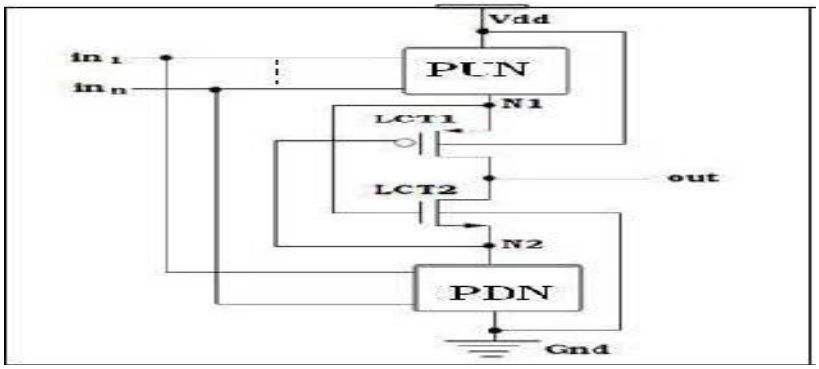

Fig. 4: LECTOR Technique

IV. PROPOSED TECHNIQUE

In this proposed technique, we introduced a single leakage control transistor within the logic gate for which the logic gate terminal of leakage control transistor (LCT) is controlled by the output of circuit itself**.** Which increases the resistance of the path from pull down network to ground thereby impressing the resistance from V_{ddn} to ground, leading to significant decrease in leakage currents? The main advantage as compared to other techniques is that LCPMOS technique does not require additional control and monitoring circuitry, thereby limits the area and also the power dissipation in active state. Leakage control (PMOS) technique is illnstrated in detail with the area the case of an inverter LCPMOS INVERTER shown in figure 5. A PMOS is introduced as LCT between N1 and Gnd node of inverter.

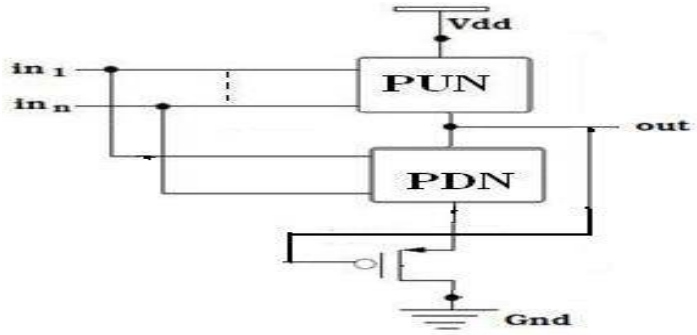

Fig.5: LCPMOS Technique

When V_{dd}=1v, input A=0, the output is high. As the output drives the LCT goes to OFF state hence provides high resistance path between V_{dd} and Gnd. When A=1 the output is low, hence LCT will be in ON state hence output is low. LCPMOS inverters for all possible inputs are shown in table 1.

TABLE1: Possible Inputs of LPCMOS Inverters

Transistor Reference	Input vector A	
	O	1
M1	ON State	OFF State
M2	OFF State	ON State
LCT	Near cut-off state	ON State

In the sleep related technique, the sleep transistors have to be able to isolate the power supply and Gnd from the rest of the transistors of the gate. Hence they need to be made bulkier dissipating more dynamic power. This offsets the saving

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yielded when the circuit is idle. Sleep transistors technique depends on input vector and it needs additional circuitry to monitor and control the switch in sleep transistors, consuming power in both active and idle states. In comparison, LCPMOS generates the required control signals within the gate and is also vector independent. Single transistor is added in LCPMOS technique in every path from V_{dd} to GND irrespective of number of transistors in pull-up and pull-down network. The loading requirement with LCT is a constant which is lower.

V. EXPERIMENTAL RESULTS

The CMOS INVERTER is shown in figure 6 with the one LCT added between pull-down network and Gnd. The simulations waveforms of LCPMOS NOT from figure 7 shows that basic characteristic of NOT are retained by LCPMOS NOT gate.

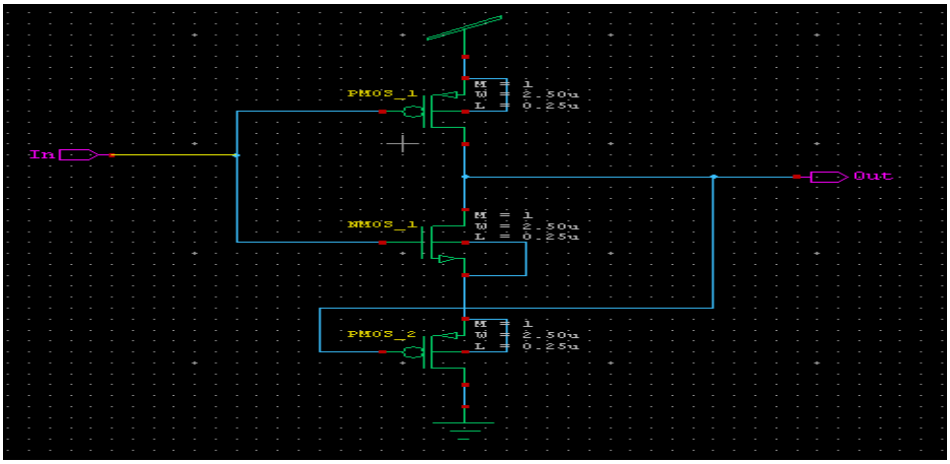

Fig.6: LCPMOS based NOT Gate

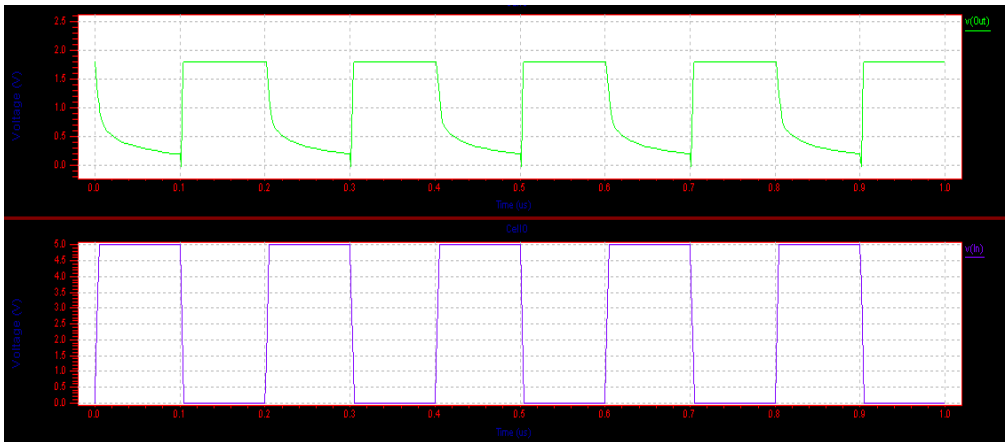

Fig.7: Waveform of LCPMOS based NOT Gate

The 2-inputs CMOS NAND Gate is shown figure 8 with the one LCT added between pull-down network and ground. The simulation wave forms of LCPMOS NAND form figure 9 show that the basic characteristics of NAND are retained by LCPMOS NAND.

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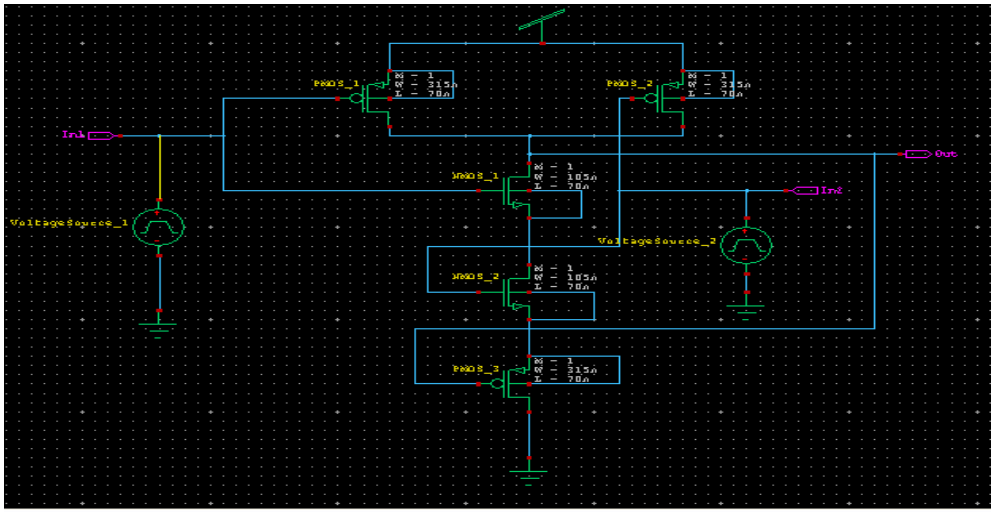

Fig.8: LCPMOS based NAND Gate

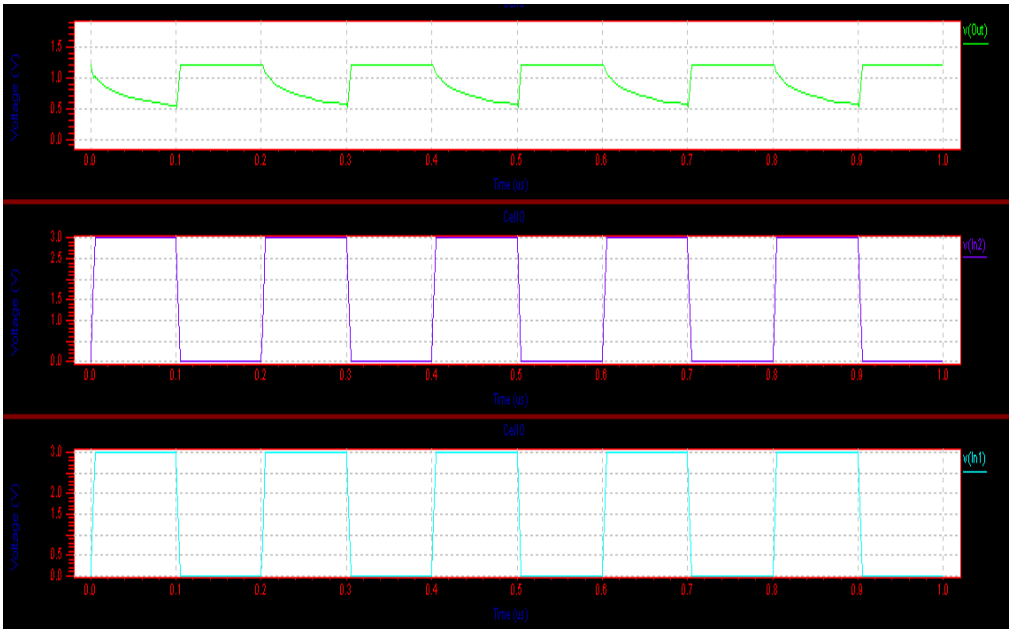

Fig.9: Waveform of LCPMOS based NAND Gate

Similarly the 2-input CMOS NOR gate is shown in figure10 with the one LCT added between pull-down network and gnd. The simulation waveforms of LCPMOS NOR from figure8 show that the basic characteristics of NOR are retained by LCPMOS NOR.

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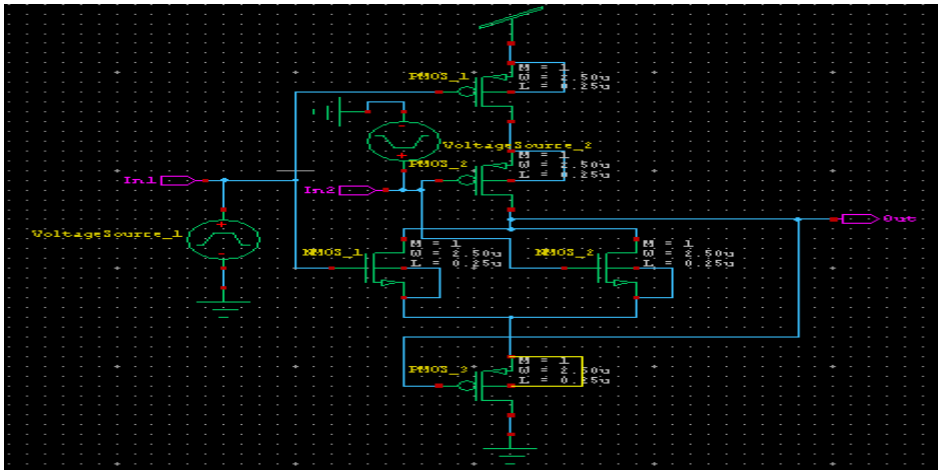

Fig.10: LCPMOS based NOR Gate

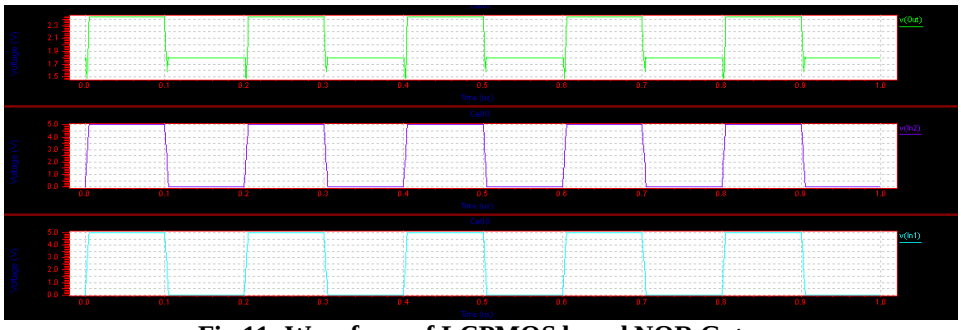

Fig.11: Waveform of LCPMOS based NOR Gate

The leakage power is calculated using the S-EDIT simulator of TANNER TOOLS. The results obtained through the different techniques for NOT gate, NAND gate and NOR gate is shown in Table 2 to Table 7. Simulations are performed by taking two different process parameters Viz., 65nm, 45nm. From these table it is seen that average power of LCPMOS technique is much lower as comparable to Base CMOS and LECTOR techniques for both 65nm and 45 nm technologies. However if we compare both the technology, it is seen that as the technology decreases reduces the power dissipation. So we conclude that novel LCPMOS is the efficient technique for leakage power reduction in CMOS VLSI circuits.

TABLE 2: NOT GATE at 65 nm

Techniques	Average power (nw)	Delay (ns)
Base CMOS	99	-1.04
LECTOR	90	-1.8
LCPMOS	35	-1.9

TABLE 3: NOT GATE at 45 nm

Techniques	Average Power (nw)	Delay (ns)
Base CMOS	72	-1.05
LECTOR	63	-3.2
LCPMOS	15	-3.7

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(An ISO 3297: 2007 Certified Organization)

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TABLE 4: NAND GATE at 65 nm

Techniques	Average Power (nw)	Delay (ns)
Base CMOS	86	-3.6
LECTOR	57	-3.7
LCPMOS	51	-4.1

TABLE 5: NAND GATE at 45 nm

Techniques	Average Power (nw)	Delay (ns)
Base CMOS	59	-2.9
LECTOR	48	-3.2
LCPMOS	35	-3.8

TABLE 6: NOR GATE at 65 nm

Techniques	Average Power (nw)	Delay (ns)
Base CMOS	70	-9.4
LECTOR	35	-9.6
LCPMOS	28	-9.7

TABLE 7: NOR GATE at 45 nm

Techniques	Average Power (nw)	Delay (ns)
Base CMOS	36	-9.6
LECTOR	28	-9.8
LCPMOS	24	-9.9

VI. CONCLUSION

The increase in leakage power because of the scaling down of device dimensions, supply and threshold voltages in order to achieve high performance and low dynamic power dissipation, becomes more with the deep-submicron and nanometre technologies and thus it becomes a great challenge to tackle the problem of leakage power. LCPMOS uses one LCT which is controlled by the output of circuit itself. LCPMOS achieves the reduction in leakage power compared to other leakage reduction techniques, such as LECTOR, sleepy stack, sleepy keeper, etc, along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained. The LCPMOS technique when applied to generic logic circuits achieves up to 80-92% leakage reduction over the respective conventional circuits without affecting the dynamic power. For that, this novel technique will be new era in low power VLSI design. The results are simulated using Tanner tool in 45nm and 65 nm technology.

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