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Variation Effect of Frequency Modulation Index on Harmonic Behaviour of Cascaded H-Bridge Multilevel Inverter

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ABSTRACT: The fast growth of the solar energy applications requires improvement of the different technology of the PV systems such as the transport technology of the electrical power and connection to the network. The major demerit of the PV electric energy is that, required conversion of the PV output from DC to AC, which led the inverter to play an important role in the PV conversion chain. However, conventional inverters reach the limit of efficiency conversion expressing a higher total harmonic distortion. The multilevel inverter topology introduced as a better replacement in case of cost efficiency and harmonic distortion. In this paper, the third major topology of multilevel inverter, known as cascaded H-bridge topology was studied and simulated comparing the variation effect of the carrier frequency on the cost efficiency for different output voltage level.

KEYWORDS: Inverter, multilevel, cascaded H-bridge, cost efficiency.

I.INTRODUCTION

In recent years, a higher demand on the PV system applications begun to demand higher power equipment reaching the level of megawatt [1]. The conversion chain of the photovoltaic systems included the solar cells as electrical power generator. However the obtained electric energy is in a form of DC which cannot be connected directly to the network grid. A power electronics known as the inverter is necessary for the conversion of DC to AC to feed the network with a higher performance efficiency, and low cost power [2]. However the conventional inverters already reach their limits due to a controversial issue which is the current harmonic level [3]. A new inverter structure was introduced as a solution for the total harmonic distortion (THD) known as the multilevel inverter (MLI). This structure have received more attention due to its capability of higher voltage operation with higher efficiency and lower THD [4]. MLI topology is focused on medium and high power conversion, power increasing and harmonic quality improvement [5].MLI structure is classified in three main topologies, the neutral-clamped-diode, the floating capacitor and the cascaded structure. The MLI cascaded have the possibility of conversion from fixed DC voltage to variable AC output with constant or variable frequency [6]. The output voltage waveform of the MLI approaches the sinusoidal waveform using different control techniques and can be classified according to the switching frequency. Methods working with high switching frequency which mean dealing with many switches in one period of the fundamental output voltage such as the sinusoidal pulse width modulation method (SPWM) [7]. And the space vector modulation (SVM) [8]. In the other hand the methods that work with low switching frequencies modulation such as the space vector control (SVC)[9].However, the control optimization of the cascaded H-bridges topology in term of total harmonic distortion factor and efficiency factor is required to improve the output voltage of the inverter.

In this paper, the SPWM modulation technique was used to control the cascaded H-bridges topology of the MLI inverter. We discussed the optimization of the SPWM technique with a comparison simulation study in term of output voltage quality defined as the total harmonic distortion factor dependency on the variation of the frequency modulation index defining the relation between the carriers modulation frequency by the fundamental modulation frequency.

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II.SYSTEM MODEL AND DESCRIPTION

In this work, cascaded H-bridge traditional topology of the multilevel inverter with different output voltage level is reviewed. This topology required several number of separated sources and components depending on the desired levels of voltage. For the control method, SPWM was chosen based on its simplicity and efficiency to deal with more than 3 level output voltage. The electronic simulation circuit and control technique will be discussed in the next sub sections.

II-1- Schematic electronic circuit

In Fig. 1 the seven level MLI cascaded H-bridges schematic is given as an example circuit to show the structure of this topology. It consists of H-bridges cells powered by separate power supplies and contain in each cell four switches controlled in complementary (Sa1, S'a1) to (Sa6, S'a6) mode and a total of three cells in each leg with a variation of the control frequency.

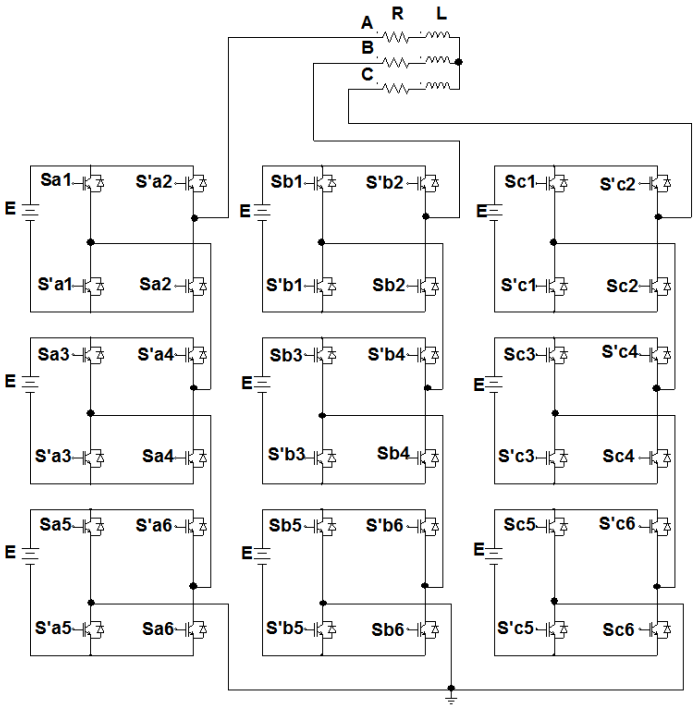

Fig. 1 Three phase seven-level cascaded topology inverter

The simulation was performed at 4 different output voltage level including the seven, eleven, fifteen and thirty one level and the circuit components of each level is shown in table 1.

Table 1 Components number of the cascaded multilevel inverter topology

	Topology
	Cascade
Power Source	3/2(m-1)
Principal dispositifs of commutation	6(m-1)
Diodes	6(m-1)
Capacitors	0
Total number of components	13.5(m-1)

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II-2- Control technique SPWM

The SPWM is based on a carrier modulation strategies, it consists of a comparison between two signals one is sinusoidal and the other is high frequency carrier waveform. The comparison results will generates the control of the different switches in a complementary way. This technique has the advantage of achieving low THD on the line-to-line voltage and high efficiency control [10] and it is based on the PD control which command all the carrier to be in phase as shown in Fig. 2.

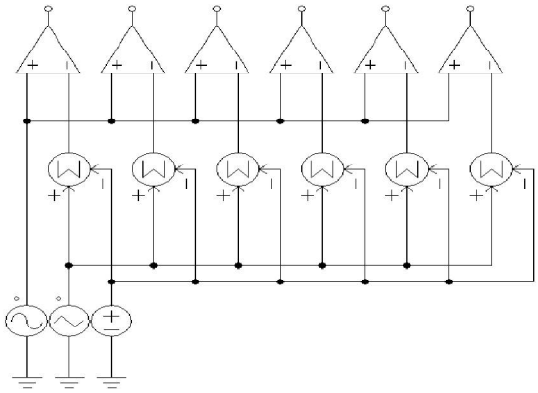

Fig. 2 Logical Diagram of the SPWM

The output voltage level (k) is given by a comparison (k-1) high-frequency carrier signal with a sinusoidal waveform. The main control signals G1 to G6 are generated by a direct comparison of 6 triangular carrier signals with a sinusoidal modulation signals as shown in Fig. 3.

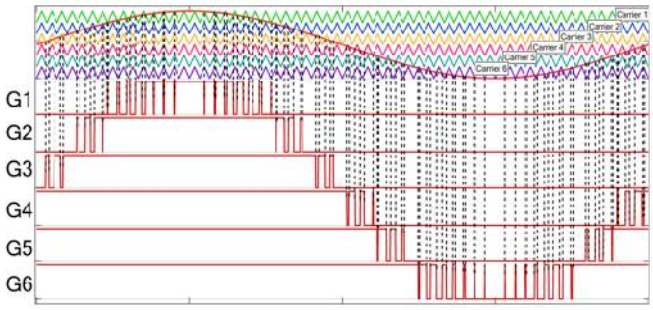

Fig. 3 Switching signals comparison

The switches control is operated by a logical process based on Fig. 2 logical diagram and the results are shown in table 2.

Table 2Different Switching Stages of the used MLI for 7 Level multilevel inverter (1=ON, 0=OFF)

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S'_{a1}	S'_{a2}	S'_{a3}	S'_{a4}	S'_{a5}	S'_{a6}	V_{ao}
1	1	1	1	1	1	0	0	0	0	0	0	**3E**
0	1	1	1	1	1	1	0	0	0	0	0	**2E**
0	0	1	1	1	1	1	1	0	0	0	0	**E**
0	0	0	1	1	1	1	1	1	0	0	0	**0**
0	0	0	0	1	1	1	1	1	1	0	0	**-E**
0	0	0	0	0	1	1	1	1	1	1	0	**-2E**
0	0	0	0	0	0	1	1	1	1	1	1	**-3E**

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The frequency modulation index [6], which describe the frequency relation between the fundamental sinusoidal signal and the carrier signal is given by Eqs. (1).

$$m_f = \frac{f_c}{f_m} \qquad (1)$$

III- SIMULATION AND RESULTS DISCUSSION

The variations of the modulation frequency index are illustrated in table 3. This variation is simulating the inverter control with different switching frequencies from the lowest to the highest.

Table 3Total Harmonic Distortion factor dependency on the output voltage level

Frequency index	1	2	20	200
Level				
7	12.15	16.97	17.92	18.41
11	7.59	10.76	10.65	11.15
15	5.52	7.85	8.28	7.99
31	2.64	3.72	3.71	3.74

This results prove that each level has a specific optimum frequency for the control carrier waveform of the SPWM technique. The seven-level inverter shown a lower THD for a lower frequency control of the switches comparably to the thirty-one-level which can be explained by the dependency on the number of components.

Figure 4 shows the output line-to-line voltages V_{AB}, $V_{BC,}$ and V_{CA}, deduced as shown in Eqs. (2).

$$V_{AB} = V_{A0} - V_{B0}$$
$$V_{BC} = V_{B0} - V_{C0} \qquad (2)$$
$$V_{CA} = V_{C0} - V_{A0}$$

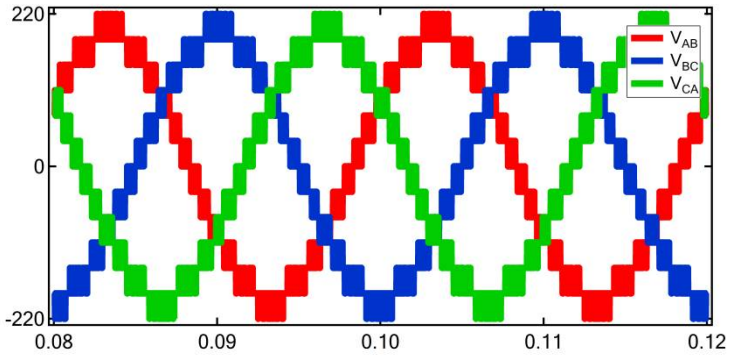

Fig. 4 Seven-level output line-to-line voltages V_{AB}, V_{BC}, V_{CA}

Seven-level in the line-to-line voltage V_{AB}, V_{BC}, V_{CA}, where each one of them is shifted by a phase angle equal to 120° (3E, 2E, E, 0, -E, -2E, -3E),is produced from five-level pole voltages. Nine-level pole voltages produced eleven-level line to line voltages (5E, 4E, 3E, 2E, E, 0, -E, -2E, -3E, -4E, -5E). Thriteen-level pole voltages produced fifteen-level line to line voltages (7E, 6E, 5E, 5E, 4E, 3E, 2E, E, 0, -E, -2E, -3E, -4E, -5E, -6E, -7E).

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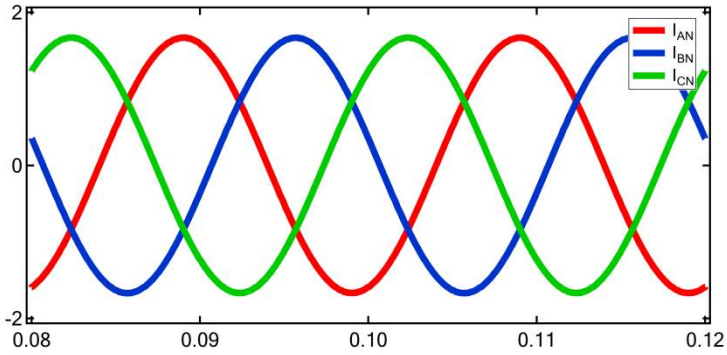

Fig. 5 Seven-level output phase current I_{AN}, I_{BN}, I_{CN}

Figure 5 shows the simulation results of the phase current shape and indicates that the phase current in case of R-L charges shows a stable and smoother output current signal due to the automatic filtering of the harmonic components by the inductance. The THD is found to be 12.15% in case using the fundamental frequency for the triangular carriers. Increasing the number of level will lead to decrease the total harmonic distortion factor.

IV-CONCLUSION

The direct variation effect of the frequency modulation index of the MLI cascaded topology is discussed. The point of comparison included the total harmonic distortion relation to the increase of the inverter voltage levels. The SPWM was applied for controlling the different MLI topology and shown a simplified control and higher stability of the inverter.The THD results indicates that each output voltage level requires specific control frequency, and it's depend on the number of components of the cascaded structure. And we demonstrate that increasing the output voltage level will be an essential key to improve the efficiency of the inverter by decreasing the total harmonic effect by reducing the control stress on the switches.

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