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Renewable Energy Based Diode Clamped Multilevel Inverter with Reduced number of switches for Drives Application

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ABSTRACT: In this paper PV based diode clamped multilevel inverter (DC-MLI) with the reduced number of switches are presented. Reduced number of switches are employed in DC-MLI for generating seven levels of AC output. The proposed Converter (Buck Boost) voltage polarity is positive also voltage gain is squared times of the traditional Buck Boost converter. So it is used for wide range of positive output. In this proposed system Buck Boost converter's two switches are operating synchronously. In continuous conduction mode switch turn-on & turn-off periods are available. At the time of Switch-on period, two inductors are magnetized and two capacitors are discharged, during the switch- off period two capacitors are charged and two inductors are demagnetized.The switching losses and the voltage stress of power devices can be reduced in proposed multi-level inverter. The operating principles of proposed inverter and voltage balancing method of input capacitors are presented using MATLAB software and simulation results are presented.

KEYWORDS: PV system, Buck Boost converter, Diode clamped multilevel inverter, Single phase induction motor.

I.INTRODUCTION

In the current scenario, because of the environmental problems and restricted fossil resources, the demand for renewable energy is increasing. to fulfill this growing demand, Solar (PV), fuel cell and Wind energy (WT) systems became the necessary integral a part of grid connected renewable energy systems (RES). Harnessing of power from the PV systems contributes to clean power generation. This contribution make it wide spread in the current international atmospheric condition. Long lasting, high efficiency and pollution free power generation are the benefits of PV systems. In section II and III discussed about the diode clamped multi-level inverter and buck boost converter design and operation. In section V discussed about the simulation and its results.

II.DIODE CLAMPED MULTI LEVEL INVERTER

Figure 1 shows the planned novel topology utilized in the seven level inverter, input resistor consists of 3series capacitors C1, C2, and C3. The divided voltage istransmitted to H-bridge by four MOSFET, and 4 diodes.The voltage is send to output terminal by H-bridge that isformed by four MOSFET. The planned structure electrical convertergenerates seven levels AC output voltage with the suitablegate signals style.

The required seven voltage output levels (+/-1/3Vdc, +/-2/3Vdc, +/-Vdc, 0) square measure generated as follows:
1) To get a voltage level Vo = 1/3Vdc, S1 is turned on atthe positive 0.5 cycle. Energy is provided by thecapacitor C1 and also the voltage across H-bridge is 1/3Vdc. S5and S8 is turned on and also the voltage applied to the loadterminals is 1/3Vdc.
2) To get a voltage level Vo = 2/3Vdc, S1 and S4 square measureturned on. Energy is provided by the electrical device C1 and C2.The voltage across H-bridge is 2/3Vdc. S5 and S8 is turnedon and also the voltage applied to the load terminals is 2/3Vdc.

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3) To get a voltage level Vo = Vdc, S1 and S2 square measure turnedon. Energy is provided by the electrical device C1, C2, and C3.The voltage across H-bridge is Vdc. S5 and S8 is turned onand the voltage applied to the load terminals is Vdc.
4) To get a voltage level Vo = -1/3Vdc, S2 is turned on atthe negative 0.5 cycle. Energy is provided by thecapacitor C3 and also the voltage across H-bridge is 1/3Vdc. S6and S7 is turned on and therefore the voltage applied to the load terminals is -1/3Vdc. Fig. half dozen shows this path at thismode.
5) To come up with a voltage level Vo = -2/3Vdc, S2 and S3 square measureturned on. Energy is provided by the condenser C2 and C3.The voltage across H-bridge is 2/3Vdc. S6 and S7 is turnedon, the voltage applied to the load terminals is -2/3Vdc.
6) To come up with a voltage level Vo = -Vdc, S1 and S2 square measure turnedon. Energy is provided by the condenser C1, C2, and C3,the voltage across H-bridge is Vdc. S6 and S7 is turned on,the voltage applied to the load terminals is -Vdc.
7) To come up with a voltage level Vo = zero, S5 and S7 square measure turned on.The voltage applied to the load terminals is zero.
Table I& II shows the components comparison of seven level inverters and the voltage stress of different inverters, Table III lists the shift mixtures at totally different outputlevels.

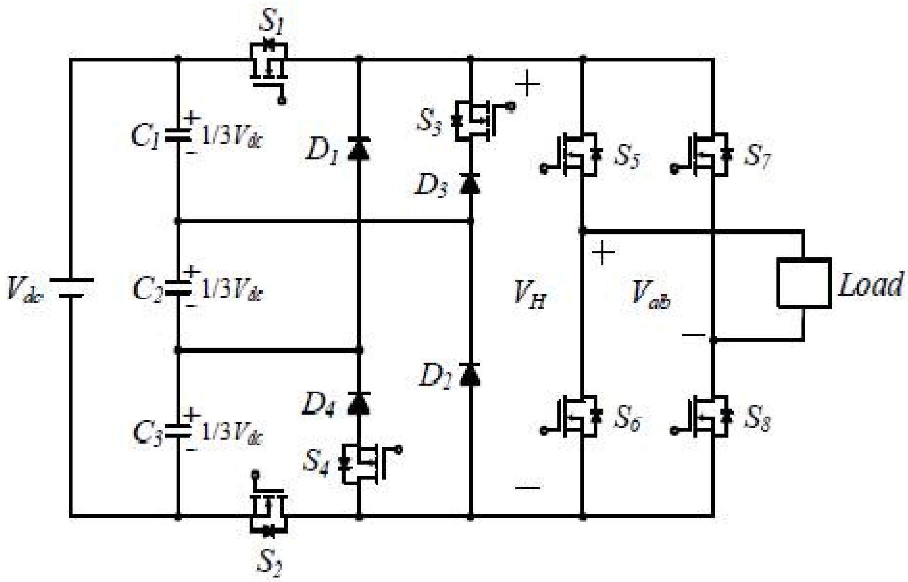

Fig. 1DC MLI topology

TABLE I
COMPONENTS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

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TABLE II
VOLTAGE STRESS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	V_o	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	V_o	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

TABLE III
SWITCHING COMBINATIONS REQUIRED TO GENERATE THE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

	Switching combinations							
Output voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3\,V_{dc}$	on	off	off	off	on	off	off	on
$2/3\,V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3\,V_{dc}$	off	on	off	off	off	on	on	off
$-2/3\,V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

The carriers compare with a reference sine waveform $v_{sin}$to get signal of switches. The frequency of carrier is switching frequency of inverter. The method to determine switch signals in Fig. 2are as follow,

(a) $v_{sin}<0$and $v_{sin}>v_{tri2}\rightarrow S_2$is turnedon
(b) $v_{sin}>v_{tri4}\rightarrow S_4$is turnedon
(c) $v_{sin}<v_{tri8}\rightarrow S_7$is turnedon
(d) $v_{sin}>v_{tri8}\rightarrow S_8$is turnedon
(e) $v_{sin}>0$ and$v_{sin}<v_{tri1}\rightarrow S_1$is turnedon
(f)$v_{sin}<v_{tri3}\rightarrow S_3$is turnedon
(g) $v_{sin}>v_{tri6}\rightarrow S_5$is turnedon
(h) $v_{sin}<v_{tri6}\rightarrow S_6$is turnedon

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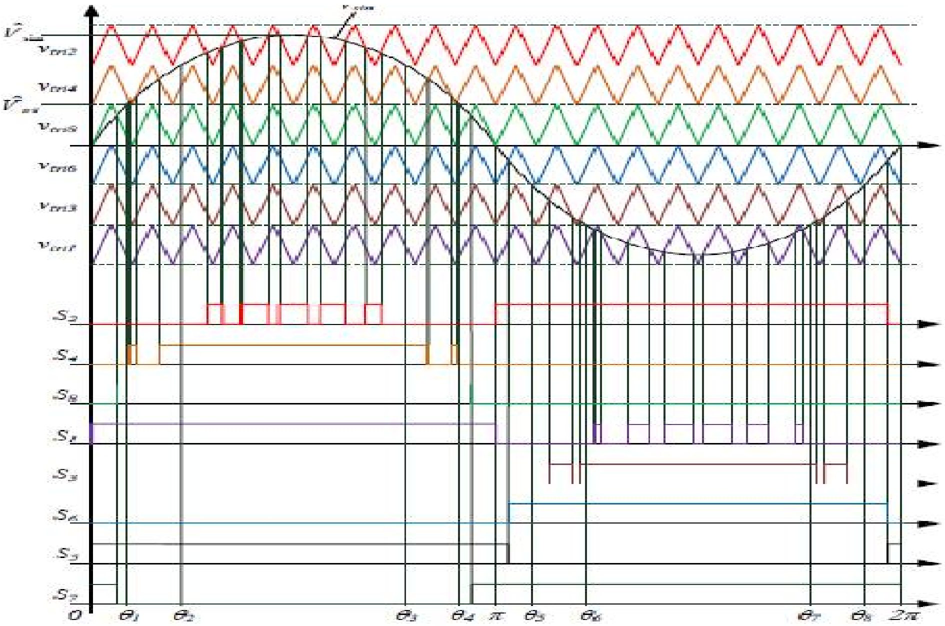

Fig. 2 SPWM

III.BUCK BOOST CONVERTER

The circuit configuration of the new transformerlessbuck–boost convertor, that consists of 2 powerswitches (S1 and S2), 2 diodes (D1 and D0), 2 inductors(L1 and L2), 2 capacitors (C1 and C0), and one resistiveload R. Power switches S1 and S2 area unit controlled synchronously.According to the state of the facility switches and diodes, sometypical time-domain waveforms for this new transformerlessbuck–boost convertor in operation in CCM. area unit displayed in Fig. 3,and the attainable operation states for the planned buck–boostconverter area unit shown in Fig. 3. For mode1 it denotes that thepower switches S1 and S2 area unit turned on, whereas the diodesD1 and D0 don't conduct. Consequently, each the electrical device L1and the electrical device L2 area unit magnetic, and each the charge pumpCapacitor C1 and also the output condenser C0 area unit discharged. Formode2 it describes that the facility switches S1 and S2 area unitturned off whereas the diodes D1 and D0 conduct for its forwardbiased voltage. Hence, each the electrical device L1 and also the electrical device L2are demagnetized, and each the charge pump condenser C1 andthe output condenser C0 square measure charged.Here, so as to change the circuit analyses and deduction,we assumed that the convertor operates in steady state, all elementsare ideal, and every one capacitors square measure giant enough to staythe voltage across them constant. Fig 4 shows the switching configuration of buck boost converter.

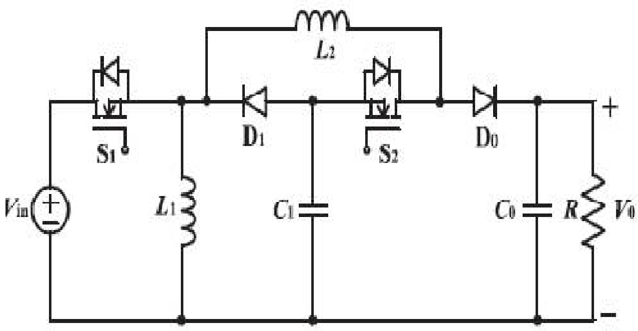

Fig. 3 Proposed Buck Boost converter topology

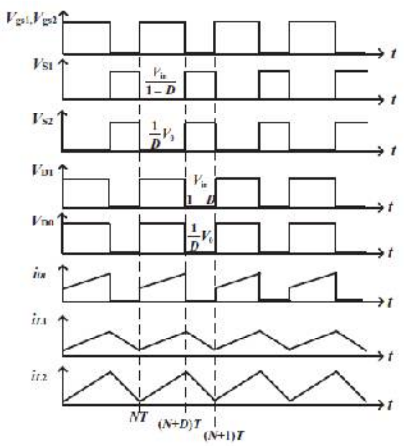

Fig. 4switching pulse of buck boost converter

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IV. SIMULATION RESULTS AND DISCUSSION

In the fig 5, it shows the simulation diagram of proposed system. In this system pv panels are connected in series to achieve the required output voltage. PV panel output voltage depends on the solar irradiation and temperature. By changing irradiance and temperature, the output voltage is varied. Buck Boost converter is used to increase or decrease the voltage. If the generated voltage is less means, boost operation performed to step up the output voltage otherwise generated voltage is high means, to step down using buck operation also it get positive output. Diode clamped multilevel inverter is used to get staircase waveform. Diode Clamped –Multi Level Inverter havereduced number of switches for getting seven levels output waveform. Filters are used to get pure sinusoidal wave form & without any distortion. Simulation results shows the output voltage of PV panel and boost converter. System output voltage and current wave form can be shown in fig .9.

The filter circuit consist of capacitor of range 200µF and inductor of range 5mH which used to eliminate the ripple content present in the output waveforms. The output of the buck-boost converter is depends on the inductors L1 and L2 of range 1mH and 3mH respectively. The dc link capacitor of 20µF is supplied to the multi-level inverter and it can gives the output for the ac load which can be fed to the drives or lamp as the consumer wish. The dc link is divided into three parts and the range will be 100mF which eliminate the ripple content present in the dc supply voltage also these capacitors are used to increase the levels of the multi-level inverter. The proposed system generated the maximum of seven levels in the generated waveforms. The output is fed to the single phase capacitor start induction motor.

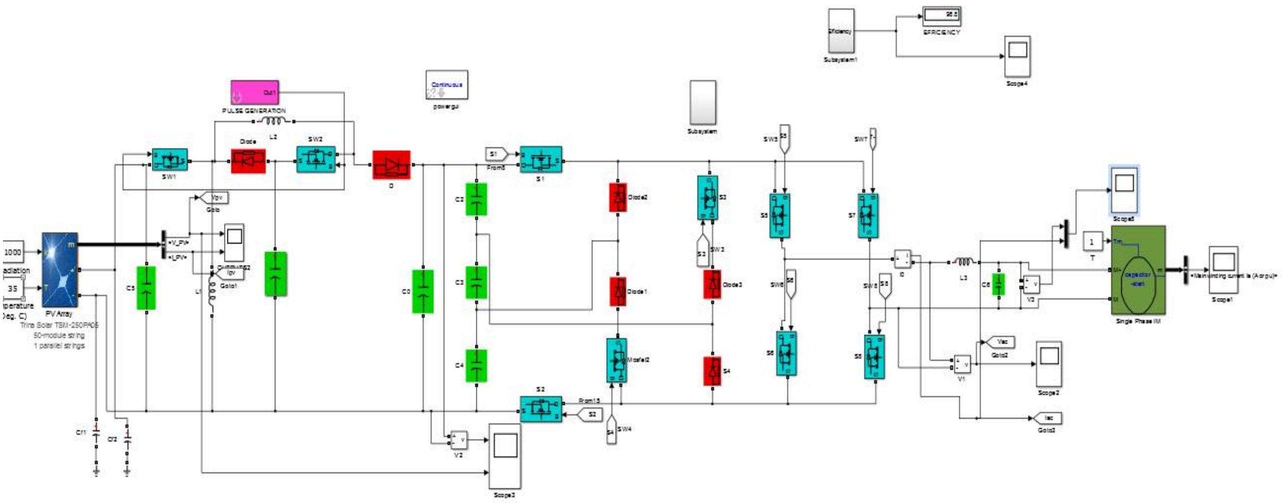

Fig. 5 Simulation of proposed system

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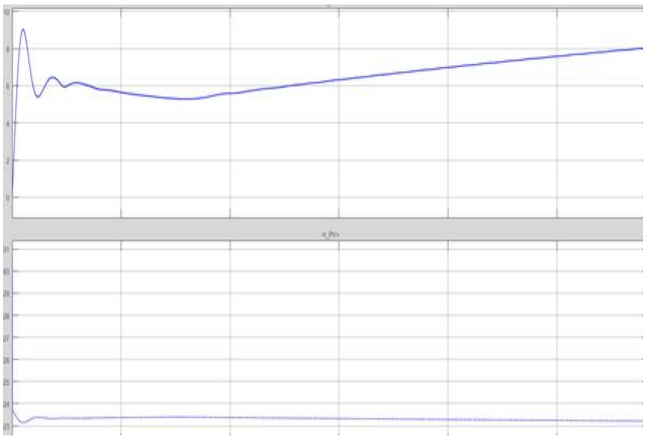

Fig. 6 output waveform of PV voltage and current

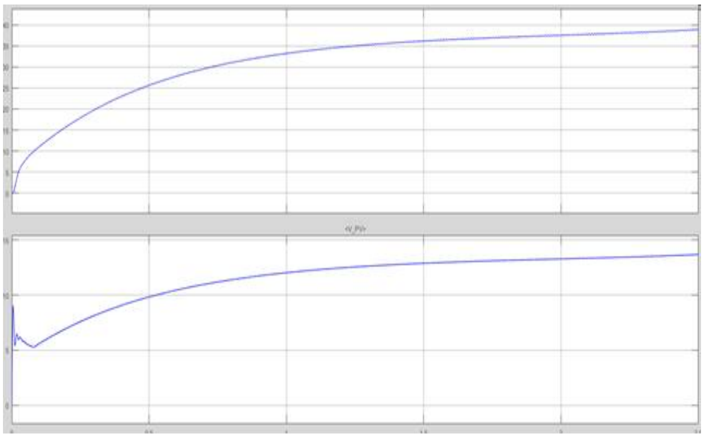

Fig. 7 Output waveform of Boost converter and PV panel

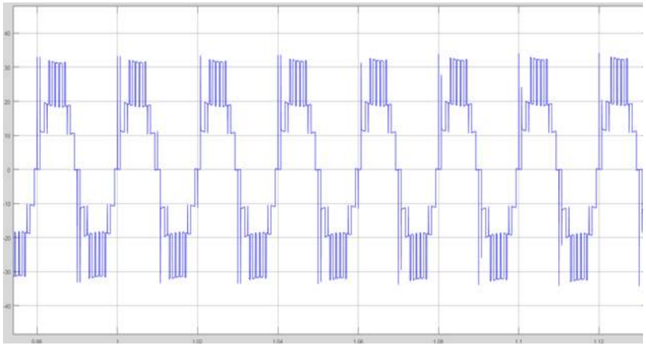

Fig. 8 Seven level output voltage waveform

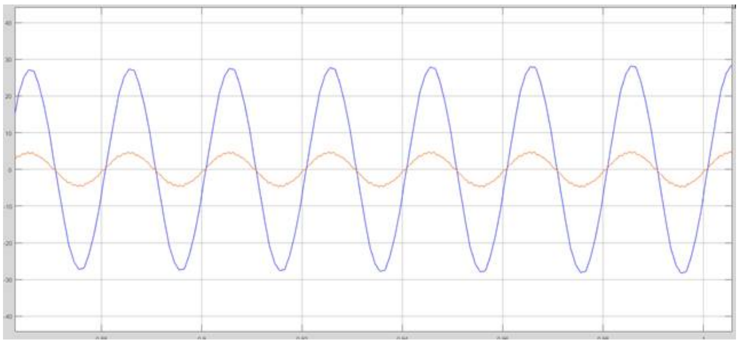

Fig. 9 Filtered output voltage waveform

V.CONCLUSION

A seven level diode clamped multilevel inverter is designed with reduced number of switches and implemented in this paper. The main part of this proposed configuration is to reduce the number of power electronic switches. The reduction of power device is proved by compare with traditional structures. Buck boost converter is normally generate negative output but hear simulated positive output. Also reduced number of switches will reduce system cost and harmonics. Experimental results shows the full load efficiency is 96.8%.

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