ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 7, April 2016

MSPWM and MTPWM Techniques for Harmonic Elimination in Modified Cascaded Inverter

P. Ram Prakash[1], Dr S.Titus[2]

Assistant Professor, Dept. of EEE, Ramco Institute of Technology, Rajapalayam, Tamilnadu, India[1]

Professor & Head, Dept. of EEE, M.A.M College of Engineering, Trichy, Tamilnadu, India[2]

ABSTRACT: Cascaded Multilevel inverters are nowadays popular in the field of high power applications for their high quality output. Cascaded Multilevel inverters are highly capable of handling more power in the output side hence they are preferred for larger power industries. This work mainly concentrates on Modified Cascaded Multilevel inverter with reduced switches. The objective of this work is to reduce switches with increase in multilevel outputs which inherently reduces the cost and harmonics. Simulations of Seven level inverter with reducednumber of switches is carried out using MATLAB/Simulink. Total Harmonic Distortion (THD) is analyzed for Modified Cascaded multilevel inverter in MATLAB. The hardware implementation is done using Power Mosfet Switches and the THD is analyzed using Power Quality Analyzer and the hardware results were validated with simulation.

KEYWORDS: Cascaded Multilevel Inverter, Total harmonic distortion (THD), Modified Cascaded Multilevel Inverter, MSPWM, MTPWM

I.INTRODUCTION

Multilevel inverter is used commonly in the field of Power electronic industries due to its high efficiency and sinusoidal like output [1]. Multilevel inverters are highly reliable, highly flexible, high conversion efficiency, flexible to enhance, low output switching frequency, low cost and the Switching losses is very less in semiconductor switches due to this advantages the multilevel inverters are well emerged trends in the area of high power industries.

The various topologies of multilevel inverters are diode-clamped MLI, capacitor-clamped MLI and Cascaded MLI [3-4] type. In the above types Cascaded MLI is more efficient than diode-clamped MLI, capacitor-clamped MLI because in diode-clamped MLI, diodes are very larger in numbers so automatically switching losses are more in diode-clamped MLI then in capacitor-clamped MLI, capacitors are more which cause charging and discharging problems. The Cascaded MLI inverter does not need any capacitor for the operation hence this cascaded type MLI is very efficient in Industries side .The General cascaded MLI is shown in Fig and thus from fig we inferred the General Cascaded MLI needed 12 semiconductor switches for a seven level output .The same seven level output can be obtained with only 7 switches & 3 diodes in the Modified Cascaded MLI circuit shown in fig .The modulation techniques used in this projects are Multiple Sinusoidal & Multiple Trapezoidal Pulse with modulation with Triangular wave as carrier wave.

The Modified Cascaded MLI topology offer strong advantages such as improved output waveforms, no filters are required and lower total harmonics distortion (THD). In this proposed topology 7 switches and 7-level MLI is proposed and a prototype is constructed for verifying the effectiveness of the topology.

II.CASCADED MULTILEVEL INVERTER

The Cascaded Multilevel inverter is nothing but two or more normal full converter with 4 switches are seriously cascaded then the semiconductor switches are triggered in a way that the multilevel output is obtained. The general cascaded MLI consist of 12 semiconductor Switches and 3 Separate DC sources .The general circuit of Cascaded Multilevel inverter is shown in fig.1.

The general circuit shows that $V_{DC1}, V_{DC2} and\ V_{DC3}$ are the 3 separate DC sources and the switches $S_{11}, S_{12}, S_{13}\ and\ S_{14}$ are the Power semiconductor Switches for 1^{st} bridge and the next $S_{21}, S_{22}, S_{23}\ and\ S_{24}$ are the

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 7, April 2016

Power semiconductor switches for 2^{nd} bridge and the next S_{31}, S_{32}, S_{33} *and* S_{34} are the Power semiconductor switches for the 3^{rd} bridge. The output voltage V_o is measured across the first and the last bridge.

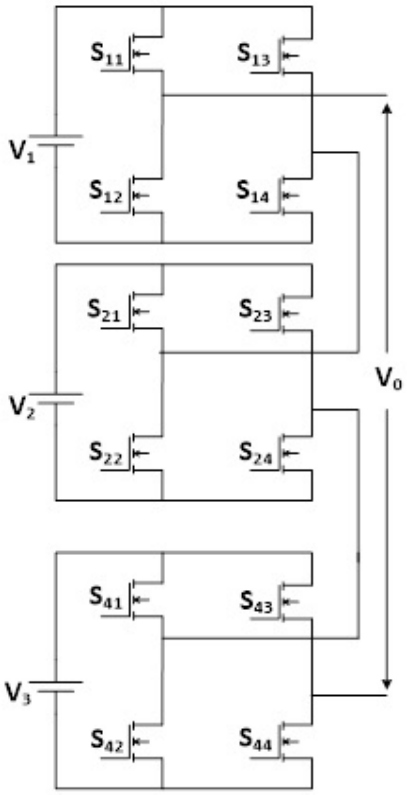

Figure 1: General Cascaded MLI Circuit

III.MODIFIED CASCADED MULTILEVEL INVERTER

The Modified Cascaded Multilevel inverter consists of only 7 Power Mosfet switches and 3 Power Diodes thus by using this Modified Cascaded Multilevel inverter the switching losses are reduced because the power semiconductor switches are reduced and the complicity of circuit minimized thus the circuit having 12 power semiconductor switches having more complex network then the modified circuit having only 7 switches. The cost of the inverter is reduced due to switches are reduced and the simulation time reduced due to less number of switches. The Modified cascaded multilevel inverter circuit is shown in fig.2.

In this circuit, the switches $S_{11}S_{21}S_{31}$ are the main Power switches and the switches $S_1S_2S_3S_4$ are the power semiconductor switches for inverter operation i.e, H-bridge switches. V_{DC1},V_{DC2}andV_{DC3} are the 3 separate DC sources for 3 separate main power switches.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 7, April 2016

Table1: switching table for modified cascaded multilevel inverter

Duration	ON Switches	ON Diodes	Voltage Levels
Positive Half Cycle	-	D_1, D_2, D_3	0
	S_{11}	D_2, D_3	+ V_{DC}
	S_{11}, S_{21}	D_3	+2 V_{DC}
	S_{11}, S_{21}, S_{31}	-	+3 V_{DC}
Negative Half Cycle	-	D_1, D_2, D_3	0
	S_{11}	D_2, D_3	-V_{DC}
	S_{11}, S_{21}	D_3	-2 V_{DC}
	S_{11}, S_{21}, S_{31}	-	-3 V_{DC}

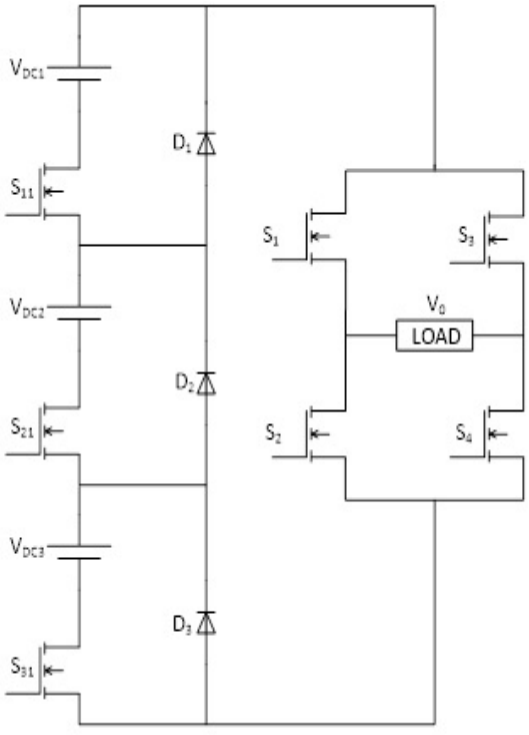

Figure 2:Modified Cascaded MLI with Reduced Switches

A. OPERATION OF MODIFIED CASCADED MLI

This type of inverter consists of a conversion unit with a switching device connected in series with a Voltage source and a diode. The number of conversion units is equal to the number of output levels. By triggering S_{11}, V_{DC1} is obtained at output which is equal to V_{dc}. Similarly, by triggering S_{11} and S_{12}, we can obtain the output voltage as the addition of V_{DC1} and V_{DC2} equal to $+2V_{dc}$. If all the switches (S_{11}, S_{12} and S_{13}) are ON, the +3Vdc level is obtained.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 7, April 2016

The output levels are unidirectional. By using H-Bridge the output is converted into bidirectional. At positive half cycle, Switches S_1 and S_4 are on and during negative half cycle S_2 and S_3 are on in the H-Bridge inverter. The switching table for Modified 7-Level inverter topology is shown in Table.1.

The number of levels (N) = (2*Number of DC Sources) + 1.

To reduce the harmonics in the multilevel inverter, the firing angles of various stages can be selected accordingly. For a 7-level inverter, three firing angles α_1, α_2 and α_3 can be selected at different values in order to reduce the lower order harmonics [7] .The conditions to select the firing angles are given by the following

$\alpha_1 < \alpha_2 < \alpha_3 < 90^o$
$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) = (m-1) * M/2$

where M - modulation index and
(m-1)/2 – Number of Separate DC Sources

IV.MODULATION STRATEGIES

A. MSPWM STRATEGY

This technique involves comparing several absolute sinusoidal [2] modulation signals with single triangular carrier. For a seven level output, three sinusoidal signals are compared to a single triangular carrier signal which is shown in fig.3. The modulation index M is
M= 2Vcr / (m-1)Vdc
Vcr – Peak Carrier Voltage, m – Number of output levels

B. MTPWM STRATEGY

In this scheme, a single triangular carrier and multiple trapezoid [2] modulating signals are used. The intersections between the trapezoid signals and carrier signal define the switching instants of the PWM [5-6] pulse. These signals can then be used to drive the actual gating signals for the power devices in the inverter module. For a seven level output, three trapezoidal signals are compared to a single triangular carrier signal which is shown in fig.4.

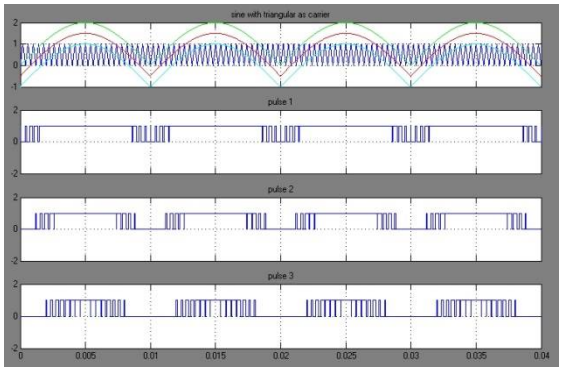

Figure 3: Switching pulse generation using MSPWM

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 7, April 2016

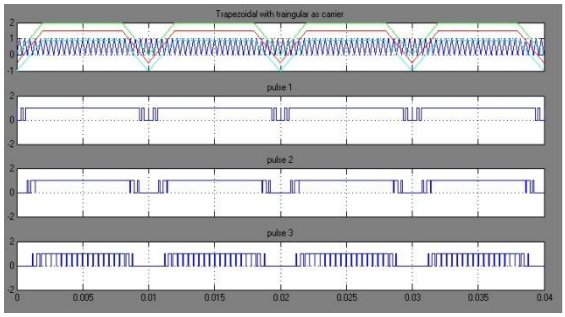

Figure 4:Switching pulse generation using MTPWM

V. SIMULATION RESULTS

In this paper MATLAB is used to implement before performing hardware. In MATLAB the seven level inverter circuit is simulated and results of output voltage and THD are shown from fig.5 to fig.10and table-2.

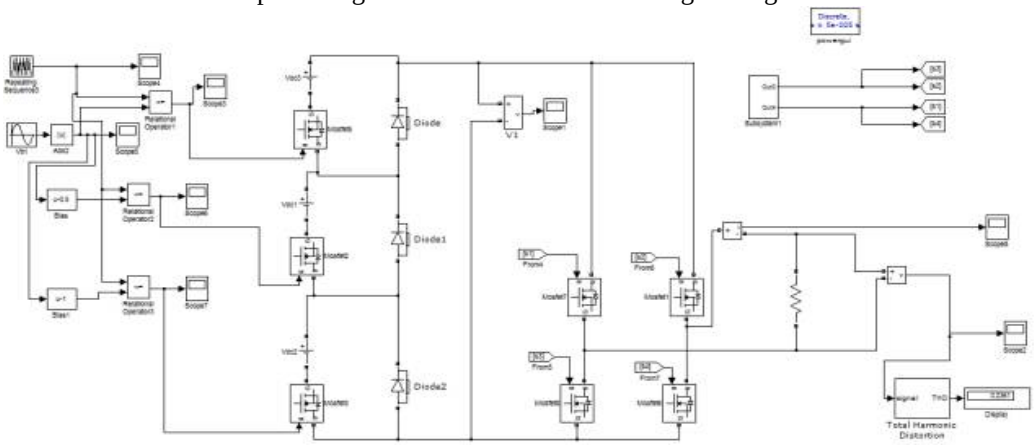

Figure 5.MATLAB/Simulink Model of Modified Cascaded 7-Level Inverter (MSPWM)

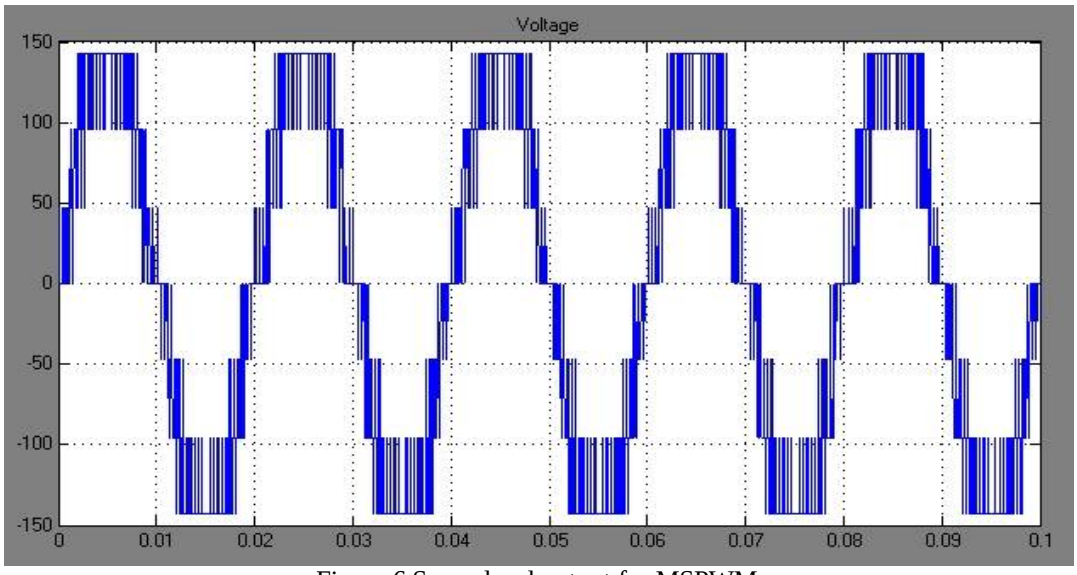

Figure 6.Seven level output for MSPWM

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 7, April 2016

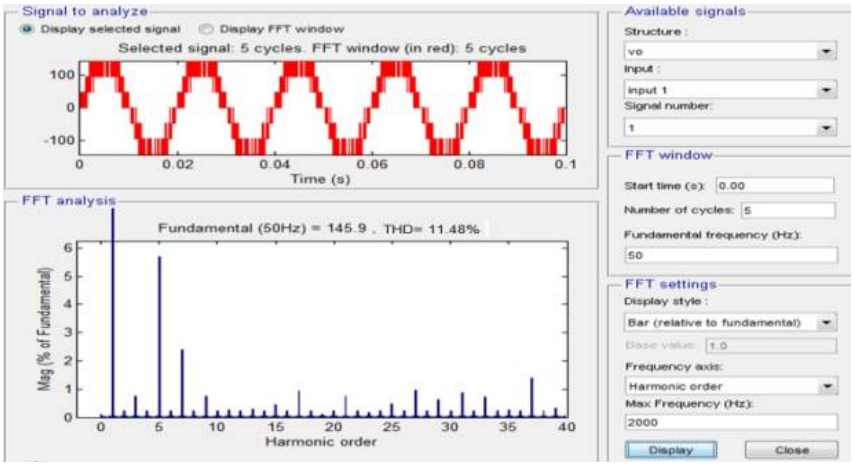

Figure 7.FFT Analysis for MSPWM

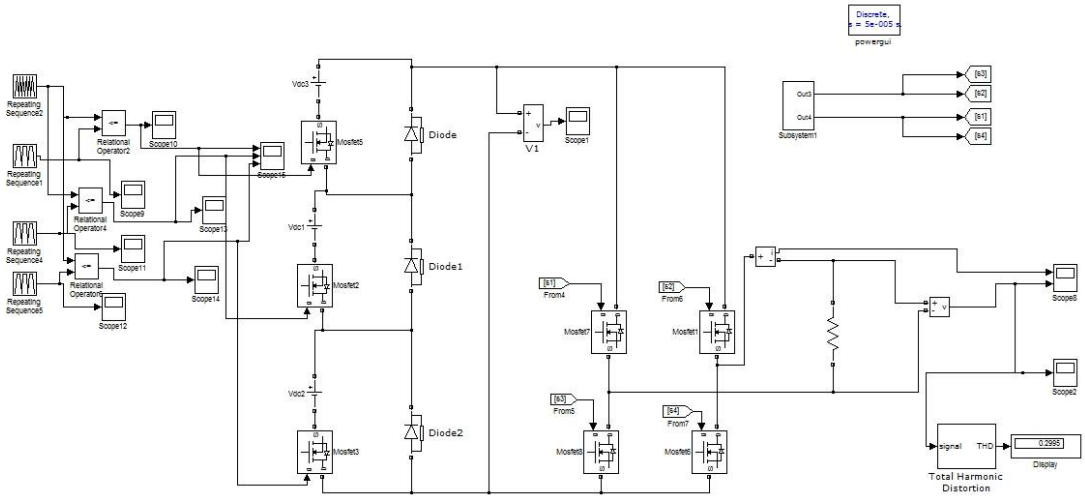

Figure 8.MATLAB/Simulink Model of Modified Cascaded 7-Level Inverter (MTPWM)

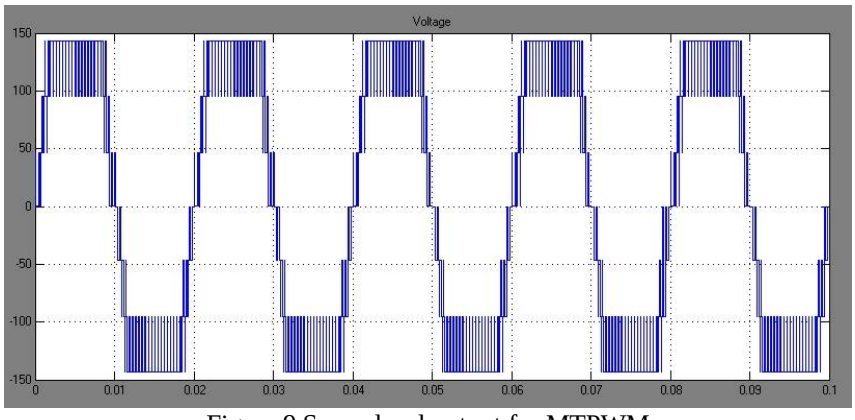

Figure 9.Seven level output for MTPWM

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 7, April 2016

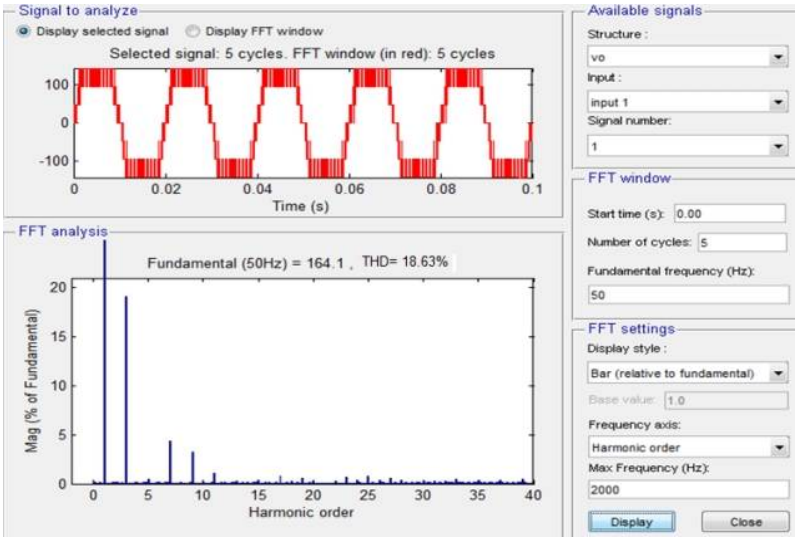

Figure 10.FFT Analysis for MTPWM

Table 2: Comparison Chart

Triangular Reference fc	THD (%
MSPWM	11.43
MTPWM	18.63

VI.HARDWARE IMPLEMENTATION

The hardware is implemented for seven level inverter, using IRF460 – MOSFET which has high voltage and current carrying capability. Gate Driver circuits are used for boosting the pulses which we get from a microcontroller. PIC16F877A is used for generating required pulses. The hardware Setup for MSPWM based Seven Level Inverter is shown in fig.11. and the output waveform for MSPWM based Seven Level Inverter is shown in fig.12.

Figure 11: Hardware Setup for MSPWM based Seven Level Inverter

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 7, April 2016

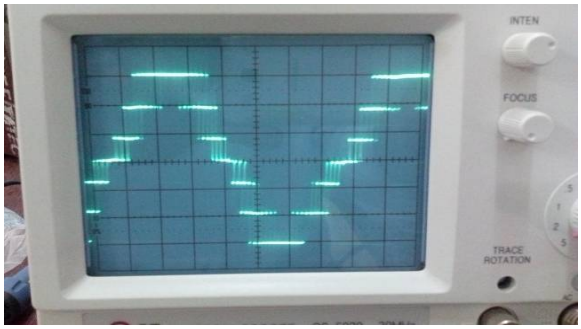

Figure 12.Output waveform for MSPWM based Seven Level Inverter

VII. CONCLUSION

This paper has dealt with pulse width modulation technique for a seven level inverter with two different multiple reference signals like Sine and Trapezoidal. The main achievement of this control techniques are the reduction in their total harmonic distortion (THD), closer to sinusoidal waveform without the usage of an output filter. Modified multilevel inverter reduces the switching losses by reducing number of switches and provides improved output voltage capability. It can be observed that MSPWM produces a better fundamental output voltage and minimized total harmonic distortion (THD). By increasing the number of levels in this method, the harmonics can be further reduced.

REFERENCES

[1] Babaei.E," Optimal topologies for cascaded sub-multilevel converters", Journal of Power Electronics, 10(3), pp-251-261,2010
[2] P.Jamuna, C.ChristoberAsirRajan "MSPWM&MTPWM Techniques for Asymmetric H-Bridge Multilevel Inverter" IEEE, International Conference On Advances In Engineering, Science And Management (ICAESM -2012) March 30, 31, 2012
[3] Mariusz Malinowski, Senior Member, IEEE, K. Gopakumar, Senior Member, IEEE, Jose Rodriguez, Senior Member, IEEE, and Marcelo A. Pérez, Member, IEEE. A Survey on Cascaded Multilevel Inverters -IEEE Transactions on Industrial Electronics, VOL. 57, NO. 7, July 2010.
[4] ZhongDu1, Leon M. Tolbert, John N. Chiasson, and BurakÖzpineci. "A Cascade Multilevel Inverter Using a Single DC Source".
[5] D. Holmes, and T. Lipo, Pulse Width Modulation for Power Converters Principles and Practice, 2003.
[6] N . A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," IEEE Trans. Power Electron., vol. 57, no. 6, pp. 2111–2123, Jun. 2010.
[7] M.H.Rashid, "Power Electronics: Circuits, Devices, and Applications", 3rd edition, Pearson education.