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Effective Use of Cache Memory in Multi-Core Processor

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ABSTRACT: Generally the CPU has fetch, decode, and execute operation. Most of today's multi-core processors feature shared caches. In shared caches the caches are splitted into blocks and are used randomly by each core in a multi-core processor. Because of this there is severe delay experienced by each core and the processing speed is also reduced. This happens due to more time taken for read operation of memory and CPU. The problem faced by such architectures is cache contention. So far the time required for fetching is more when compared to the execution process. The fetching time must be reduced. Hence to address this problem, we have implemented a program that allows the usage of cache memory for each core of a processor at same time. In our concept, we execute all jobs of each core by parallel processing. It is observed that the delay, power consumption and the memory usage is also reduced effectively, when cache memory is used parallely used by all cores.

KEYWORDS: Multi-core processor, cache memory, parallel processing, cache hit, cache miss, multi-core threading

I.INTRODUCTION

A multi-core processor has two or more cores. Each cores of the processor executes instructions like an individual computer. The real processors are still on one chip. On this chip every core looks mostly similar like others. There are variety of cores which work in parallel manner. A dual-core processor uses two independent . A quad-core processor uses four different microprocessors. It is clear from the content that, the processor name is based on how many microprocessors are being used on the chip. We use central processing unit, main memory, caches in this method. Our main aim is to minimize the delay and power consumption. And due to this the memory is utilized in an efficient manner.

II.RELATED WORKS

Author [1] N. Ramasubramanian one of the important factors that influence execution time of a program is the cache access time. Cache memory uses two sides in which one is rapid memory and another is lagging memory unit. Cache memory helps in rapid process of data, there is interest to understand the result of cache processing execution .The advancement in cache has included many cache levels and size increase. Ancient single-core systems had a improved cache model where the present multicore systems uses sharing process for cache memory. Hence due to this sharing and increase in the cache level, the cache execution time increases and tries to absorb a greater percentage of memory execution time.

Author [2] Praveena Chauhan This paper has a set associative cache memory with 4 way and observing the cache hit and cache miss process. A cache controller has been implemented with a small size of 2K byte and with 16 bytes of

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block size. Main memory has 4K byte and it is been noted. The simulation has been completed using Xilinx Synthesis Tool (XST) with spartan3 FPGA device. The simulator has functional verification of the implemented code. The maximum output execution time is which is pause-time after clock is 0.78ns and minimum input access time before clock arrival, which is initial-time for implemented module is 1.69ns. The clock frequency is 259.209MHz.The implementation has also been simulated in Cadence RTL Compiler tool. Hence, output of the implemented cache controller is completed in Cadence Encounter Digital Implementation tool and the file has been produced. The designed cache controller absorbs 5.576mW of power.

III.PROPOSED SYSTEM

In this work, we propose a simulation based technique to reduce the fetching time. This is done by using multicore processor with cache memory which is shared by all cores at different time for each application. By doing this the execution speed is increased and makes the application more efficient thereby cache contention is also reduced. To make use of the cache memory for efficient use of the multi-core processor. To parallely execute all the operations of each core in a processor by using cache memory and hence to reduce the delay and power consumption. The another objective is to reduce the memory usage effectively by parallel processing of all cores. To decrease the fetching time and increase the speed of execution for better usage of multi-core architecture.

IV.CACHE MEMORY

A cache is device that exploits both spatial and temporal locality. It simultaneously keeps a copy of updated relevent objects in a greater process storage place than the objects that are stored by themselves. The module functions on copies that present in the cache in place of functioning straightly on the objects, with a result increase in performance. The cache has duty for producing changes to the copies to send back to the objects stored. During the ancient years caches have caches have a similar place across a world wide of computer systems. This was implemented to help many engineers and scientists. Here we consider only a basic knowledge of cache and computer system implementation.

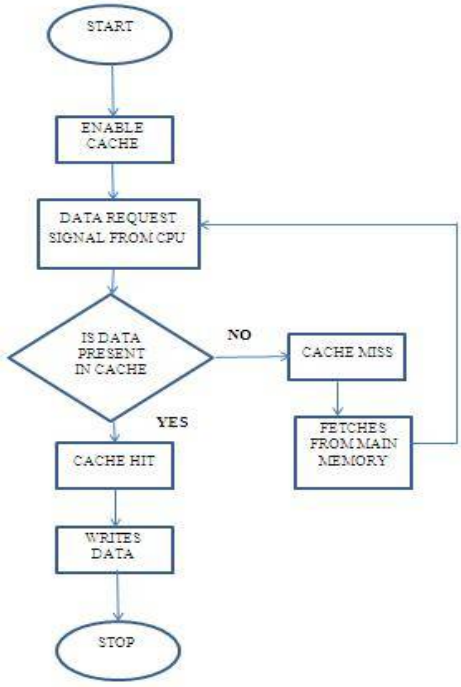

Figure 1: Cache Execution Steps

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But, this is a developed method on implementation of cache that take the user through a implementation of separate major memory variables and their dependencies. It not only provides the data on the process of machines, and it also provides complete computations of data. In previous period, cache implementation has randomly taken a last place to CPU implementation, the cache system is implemented to match the condition given by the CPU design. The execution time is most importantly minimized when the cache design influence the design of CPU.

A.Cache miss

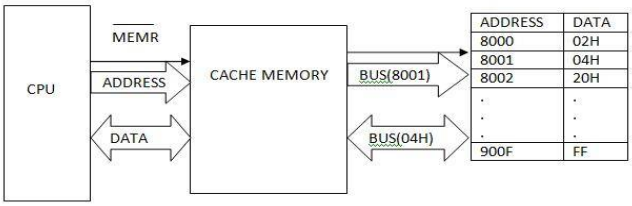

Figure 2: Cache Miss

B.Cache hit

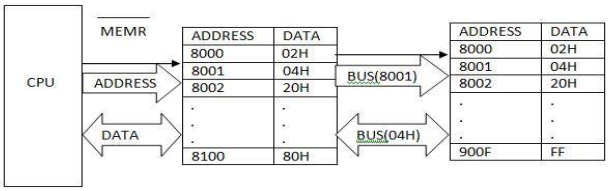

Figure 3: Cache Miss

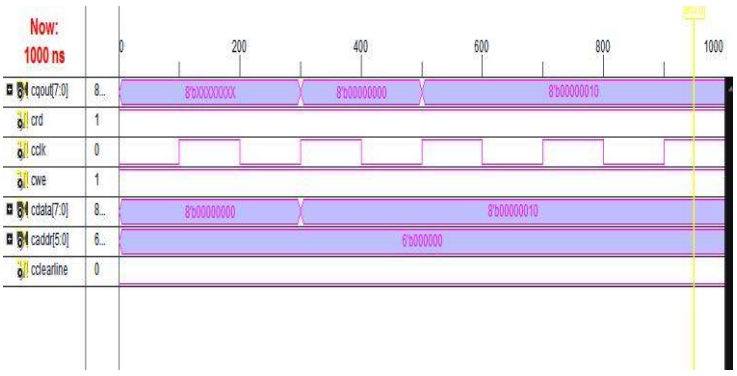

Figure 4: Simulation of Cache Memory

V. MAIN MEMORY

It is the memory where the data or instruction is actually present. It has lowest level in the memory hierarchy. The data has to be brought into the cache from the main memory as and when required by the processor. The main memory of 4K byte i.e. 4096 bytes have been designed to check the functionality of cache controller. Each location of main memory consists of 1byte i.e. 8 bits. Hence, there are total 4096 locations in the main memory in each location of

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memory is accessed by a 12 bit address line. There are two separate data lines for input and output. The input data line is of 8 bits whereas the output data line is of 128 bits. The requirement of 128 bit data line for output will be described in the operation.

The architecture of main memory is simple as compared to cache memory. Whenever there is a miss in the cache during read operation the address coming from the processor will be forwarded to the main memory with the help of cache controller. After the address arrives, the whole block of data consisting of 128 bits will be forwarded to the cache. This 128 bits data not only consists of the required data by the processor, but the neighboring data is also provided to the cache keeping in view the property of locality of the cache. In case of write operation, if there is a hit in cache, the data will be written to the cache as well as main memory by write through policy. If there is a miss, the data will be written directly to the main memory.

Figure 6: Simulation of Main Memory

VI.MULTI-CORE

A multi-core processor has more than two seperate real processing units (called "cores"), which is the units that are used for fetching and writing module. While a processor has more than single core to access all the required functions of a system, its processor is need to be multi core processor. In other lines ,a chip with more than a single CPU's (Central Processing Unit). The instructions are usual CPU instructions such as read, write data, and fetch, but more cores can execute several instructions at the simultaneous time, increasing all speed for modules that is to parallel processing. Producers usually joins the cores into a one integrated circuit (known as a chip multiprocessor), or into multiple core in a chip package. Processors were usually produced with only single core. In the 1980s Rockwell International manufactured with two cores on single chip as sharing the chip's pin on various clock cycles. Multi-core processors were produced in the early 2000s by Intel, AMD . It implements multiprocessing in one single package. Designers may dual cores in a multi-core device tightly or elastically.

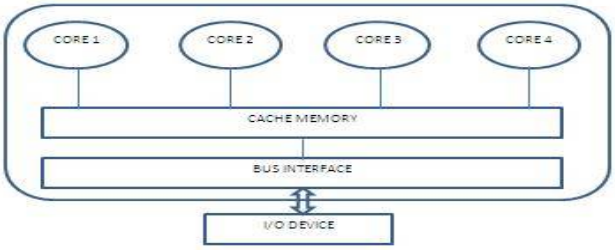

Figure 7: Multi-core Architecture

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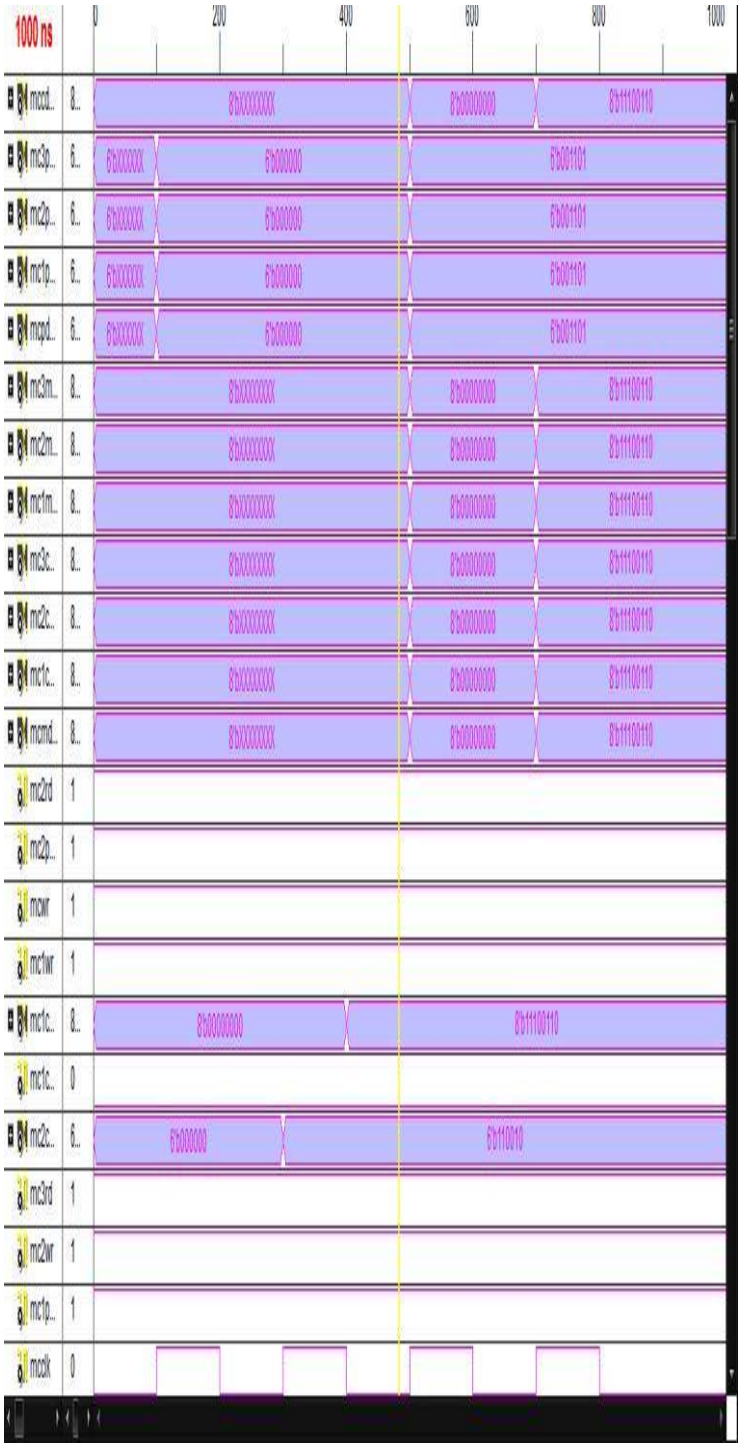

Figure 8: Simulation of Multi-Core Processor

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VII.SYNTHESIS REPORT

The design has been synthesized using Xilinx Synthesis Tool (XST). Table 1 shows the device utilization summary of cache controller designed. The development board that has been targeted is SPARTAN 3 evaluation board.

LOGIC UTILIZATION	USED	AVAILABLE	UTILIZATION
Number of Slices	1117	3584	31%
Number of 4 input LUTs	1236	7168	17%
Number of GCLKs	1	8	12%
Number of bonded IOBs	181	141	128% (*)
Number used as RAMs	15	384	3%

Table 1: Device utilization summary of the designed cache controller

Speed Grade	-4
Minimum period	5.765ns
Maximum Frequency	173.461MHz
Minimum input arrival time before clock:	10.342ns
Maximum output required time after clock:	7.165ns

Table 2: Timing summary of the designed multi-core

Speed Grade	-4
Minimum period	4.971ns
Maximum Frequency	201.155MHz
Minimum input arrival time before clock:	8.929ns
Maximum output required time after clock:	6.216ns

Table 3: Timing summary of the designed single-core

The main memory has been enabled to read data from it as memories 0 and memories 1. Also has to be kept 1 in order to perform any read or write operation in main memory.

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The main memory will be referred for read only when there is a miss in the cache. So, not only the data required by the processor will be read but the whole block will be sent to the cache keeping in view the property of spatial locality.

VIII.POWER REPORT

(total power consumption=351mW)

	I(ma)	P(mW)	V(volts)
Vccint	12	18	1.50
Vccaux	100	330	3.30
Vcco33	1	3	3.30
Inputs:	0	0	-
Logic:	0	0	-
Outputs:	0	0	-
Vcco33	0	0	-
Signals:	0	0	-
Quiescent Vccint	12	18	1.50
Quiescent Vccaux	100	330	3.30
Quiescent Vcco33	1	3	3.30

Table 4: Power report of Multi-core Processor

(total power consumption = 404mW)

	I(ma)	P(mW)	V(volts)
Vccint	45	68	1.50
Vccaux	100	330	3.30
Vcco33	2	7	3.30
Inputs:	0	0	-
Logic:	0	0	-
Outputs:	0	0	-
Vcco33	0	0	-
Signals:	0	0	-
Quiescent Vccint	45	68	1.50
Quiescent Vccaux	100	330	3.30
Quiescent Vcco33	2	7	3.30

Table 5: Power report of Sinle core Processor

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IX. CONCLUSION

Design Suite in Verilog HDL and it has been found to work successfully with given inputs. In this design, the main memory has been considered. Along with this cache memory of has been designed to check the functionality of the designed. A test module has also been designed which consists of some instructions to be fetched from the instruction cache. The cache memory is made use in an efficient manner. All the operations of each core in a processor is parallely executed using cache memory and hence the delay, memory usage and power consumption is reduced. The design has been implemented on SPARTAN 3 evaluation board. From the synthesis report, it could be seen that the maximum output required time i.e. hold-time after clock is 7.165ns and minimum input time before clock arrival i.e. setup-time for designed module is10.342ns. The maximum clock frequency is 173.461MHz.The device utilization summary showed that minimum resources were consumed. The designed cache controller consumes 351mW of total power.

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