ISSN (Print) : 2320 – 3765
ISSN (Online) : 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

Design of Cascaded CMOS LNA for Ultra Low Power Application Using Positive Feedback Technique

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ABSTRACT: A novel circuit topology for a CMOS low-noise amplifier (LNA) is presented in this paper. By employing a positive feedback technique at the common-source transistor of the cascade stage, the voltage gain can be enhanced.

In addition, with the MOS transistors biased in the moderate inversion region, the proposed LNA circuit is well suited to operate at reduced power consumption and supply voltage conditions. Utilizing a standard CMOS process, the CMOS LNA has been demonstrated for 5-GHz frequency band applications. Operated at a supply voltage of 0.6 V, the LNA with the gain-boosting technique achieves a gain of 17 dB and a noise figure of 2.1dB. This CMOS LNA will be planned to work for military applications.

KEYWORDS:CMOS, low-noise amplifier (LNA), positive feedback, ultra-low power, ultra-low voltage.

I.INTRODUCTION

Wireless communication systems are commonly used in our daily life. The emerging of the new wireless communication standards would further push the development of multifunction mobile devices into the market. However, different mobile communication standards are using different modulation methods and different operation frequencies. For a multifunctional device which could work with applications that supports various wireless communication standards, the RF systems have to be designed. In RF receiver, low-noise amplifier (LNA) is one of the most critical components. It is the first amplifier which amplifies the received signal from the antenna with low noise and moderate gain, because the signal received is usually very weak and sensitive to noise or distortion.

The low-noise amplifier is a key component, which is placed at the front-end of a radio receiver circuit whose noise performance decides the noise of entire receiver. Using an LNA, the noise of all subsequent stages reduces by the gain of LNA, while noise of LNA itself is injected into the received signal. So, it is necessary to boost the signal power while adding as little noise and distortion. Wireless applications are also defined as battery powered devices. Power consumption is therefore a more important concern for the LNA.

Receiver receives the radio waves and converts their information to a suitable form. It consists of major blocks as switch, band pass filter, low noise amplifier, mixer. The information carried by the radio waves is affected by the noise. Noise which acts as an unwanted signal degrades the quality of information. So the noise parameter is of prime importance [1]. The low noise amplifier needs to have low noise figure, high gain and good stability to avoid oscillations.

In the present technology the transistors are used for amplification purpose. All the signal parameters are improved due to the use of transistors. In this design of low noise amplifier low noise figure, high gain, good stability and input output matching all these parameters should work together hand in hand [2].

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To overcome the stringent limitations imposed by ultra-low supply voltage and ultra-low power dissipation, a cascade LNA topology is presented in this paper. By operating the transistors in moderate inversion, the LNA circuit can operate at microwatt power consumption. By incorporating a positive feedback technique in the proposed topology, enhanced gain can be achieved at the frequency band of interest. The aspect ratio and gate bias of M3 are optimized for optimum voltage gain, noise figure, linearity, and stability for the proposed LNA. Using a standard 0.13-µm CMOS process, the proposed CMOS LNA is implemented for the 5-GHz band applications.

II.LITERATURE SURVEY

There are several existing solutions for CMOS-based LNAs.

The diverse range of modern wireless applications necessitates communication systems with more bandwidth and flexibility. Dual-band transceivers have been introduced to increase the functionality of such communication systems by switching between two different bands to receive one band at a time. While switching between bands improves the receiver's versatility (e.g., in multiband cellular phones). But, it is not sufficient in the case of a multifunctionality transceiver where more than one band needs to be received simultaneously (e.g., a multiband cellular phone with a global positioning system, global position system (GPS), receiver and a Bluetooth interface).

A two-stage common-source configuration was employed. This LNA was designed for 5 GHz application with 0.4 V supply voltage. By using forward-body-biased MOSFETs, the LNA can operate at 0.4 V supply voltage, demonstrating the application potential of dynamic threshold voltage technology in the radio frequency region. [3]

A 0.35-µm CMOS technology is used to design the LNA. Researcher designed new concurrent dual-band receiver architecture. It is capable of simultaneous operation at two different frequencies without dissipating twice as much power or a significant increase in cost and footprint. [8]

With the cascode amplifier topology, high gain can be achieved with relatively low current consumption. This method enhances the effective gm of the LNA by a factor that is inversely proportional to a MOSFET's input resistance. Also, this method does not degrade the NF of the LNA if the device sizes and bias conditions are chosen properly. But, there are some drawbacks with this cascode topology. The cascode LNA is not suitable for low voltage application due to its stacking configuration. [9]

In the case of multiband receiver, a fully integrated CMOS receiver front-end based on direct conversion architecture for UMTS/802.11b-g and a low-IF architecture at 100 kHz for DCS1800 was designed. [10]

There is an explicit trade-off between linearity, gain, and power consumption. To overcome the stringent limitations imposed by ultra-low supply voltage and ultra-low power dissipation, a two stage cascade LNA topology is presented in this implemented paper.

By using source degeneration technique, good input impedance matching is achieved in the first stage of an amplifier. By applying the positive feedback technique at the input of the second stage of amplifier, gain of the second stage of the designed amplifier can be enhanced.

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III.DESIGNED BLOCK DIAGRAM

The designed two stage cascaded CMOS LNA is designed by using the following blocks.

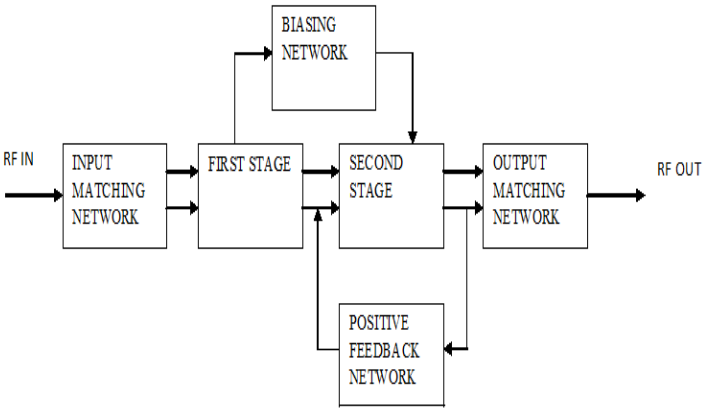

Fig. 1 Block Diagram

Since the LNA is the first component in the receiver chain, the input must be matched to be driven by 50Ω. Many methods for matching the input using passive circuit elements are possible with varying bandwidths and degrees of complexity.

Combinations of transformers, resistors, inductors, capacitors and transmission lines are used to match electrical impedances. Designed LNA requires an inductor to provide the power and noise match. It is simple and in series with the input of the transistor. It achieves simultaneous noise and power matching of the transistor.

For CMOS circuit implementations, the most widely used circuit schematic is a common-source amplifier with source degeneration for ultra-low-supply voltage. In order to effectively enhance the voltage gain at ultra-low-supply voltage, positive feedback can be incorporated in the common-source amplifier with source degeneration.

Based on a simple concept, it can be accomplished by inserting a transconductance stage. With the designed technique, the voltage gain of the source-degenerated common-source amplifier can be determined by the second stage. For better understanding of the gain-enhancement technique, the loop gain of the positive feedback is derived.

Here, fixed biasing technique is used everywhere to bias the transistors M1, M2, M3. The DC voltage depends on the transistor's voltage requirement being used for the amplifier design. By employing a positive feedback technique at the common-source transistor of the cascade stage, the voltage gain can be enhanced.

IV.CIRCUIT IMPLEMENTATION

The circuit simulation is done in the ADS (Advance Design System) software by the Agilent Company.The design using the lumped components and the TSMC RF CMOS components is done.

A. First Stage of Amplifier:

The first stage of typical CMOS low-noise amplifier uses an inductive degeneration approach for narrow-band input matching to the 50 Ω antennas. The transistor M1 is the main amplifying device of this stage and transistor M2 is cascaded with M1. An inductor L3 of a large value is connected between the drain of M1 and Vdd. This inductor which

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opposes the change in current and the cascaded transistor is to prevent large flow of drain current through M1 which can damage the transistor. The transistor M1 is biased with VG1 through the resistor R1.

As mentioned in the block diagram an input matching network is connected to the first stage i.e. the input stage for input impedance matching. Inductor L1 is used as input matching network. The gate length of the transistors is fixed at 130nm and the width of gate is varied. Bulk of both the transistors is connected to ground. In this design, the selected frequency is 5 GHz. Here in the implemented design, first stage of LNA is a common-source amplifier with source degeneration technique. This first stage of LNA is designed mainly to dominate the noise figure of the amplifier. Biasing voltage for the amplifier is 0.55V and current is 834 µA. The input impedance and output impedance matching to the amplifier circuit is provided through the inductor.

B. Second Stage of Amplifier:

For the design of the second stage of low noise amplifier, the NMOS transistor in common-source topology with source degeneration technique is used, same as in the first stage. The second stage is connected to the first stage through the coupling capacitor. The transistor M2 is biased with VG2 through the resistor R2. The maximum current that this stage should consume is 867µA. This second stage of LNA is designed mainly to achieve the high gain. Biasing voltage for this NMOS transistor is 0.55V and current is 867 µA.

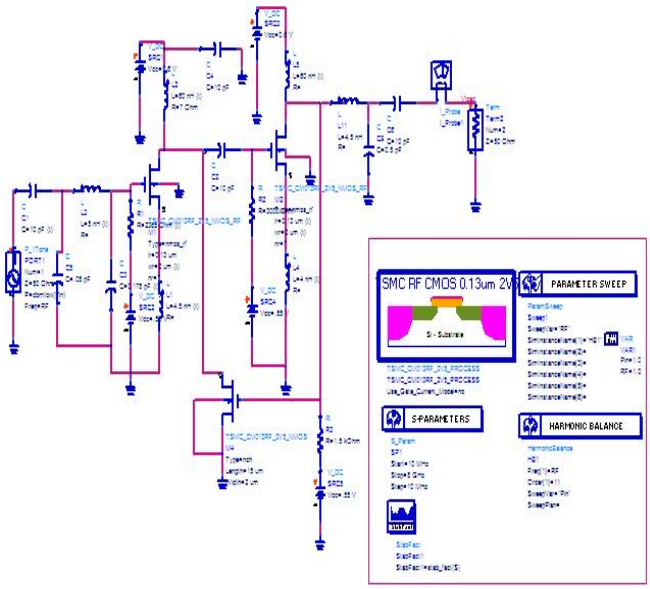

Fig. 2Schematic of an Amplifier Design

The above design, fig. 2 is implemented in the ADS. The S11 (input return loss), S12 (Isolation), S22 (output return loss) and S21 (gain) are plotted. The stability is checked of the overall circuit which is 1.5 i.e. above 1, and the noise figure is 2.1.

C. Positive Feedback Stage:

Positive feedback technique helps to enhance the overall gain of the two stage amplifier. Active device is used for the feedback. DC biasing is used to bias this active device. This feedback is applied from the output of the second stage of the amplifier to the input of the second stage of the amplifier.

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V.LAYOUT OF DESIGN

The layout process allows designers to have their circuits manufactured. Layout is an important step in RFIC design for several reasons. Layout determines the physical area that the LNA will occupy which is important as there are chip size specifications for wireless LAN transceivers. As well, the area the LNA should be minimized since the chip area for wireless LAN transceivers is limited.

More importantly, the physical layout of the LNA will have a direct impact on its performance. The performance is affected as the physical layout introduces parasitic, coupling. Layout was performed using the ADS tool.

The process that was used, CMOS 0.13µm, allows for 4 levels of metal to be used; the first level of metal is the most resistive while the top level of metal, the analog metal, is the least resistive. The metals are separated by a polysilicon layer. A connection between the metal layers is achieved using Vias. Vias provide a path from one metal to another, however they introduce resistance. To minimize the resistance, an array of Vias can be implemented.

The inductors used in the design of the LNA were built using the analog metal, while the Metal-Insulator-Metal (MIM) capacitors were built using two metal layers separated by polysilicon. The layout of the transistors was performed by ADS tool with connections to the base, emitter and collector through the first and second levels of metal. The resistors used in the LNA design were built in layout using polysilicon with connections at its terminals through metal 1.

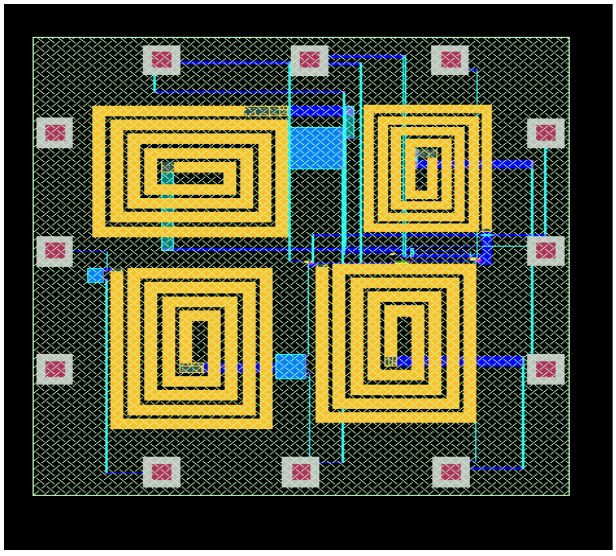

Fig. 3Layout of an Amplifier Design

Above figure 3 shows the layout of designed amplifier.

VI.BONDING DIAGRAM

Flat no-leads packages such as quad-flat no-leads (QFN) and dual-flat no-leads (DFN) physically and electrically connect integrated circuits to printed circuit boards. Flat no-leads, also known as micro lead frame (MLF) and SON (small-outline no leads), is a surface-mount technology, one of several package technologies that connect integrated circuits to the surfaces of PCBs without through-holes.
Here, QFN12 3mmx3mm package is used as shown in following figure 4.

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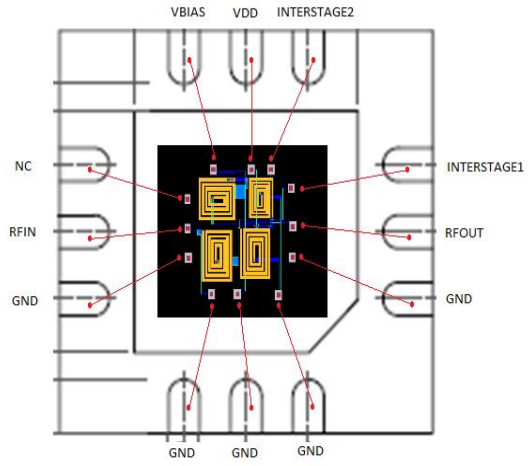

Fig. 4Bonding Diagram of Designed LNA

VII.RESULTS

ADS (Advance Design System) software is used for the simulation of the circuit. It is software developed by the Agilent Company. The parameters such as S11, S12, S21, S22, noise figure and stability are plotted for the designed circuit.

The noise figure is defined by amount of noise contributed by the circuit. For any LNA design, it is ideal to have noise figure as low as possible.

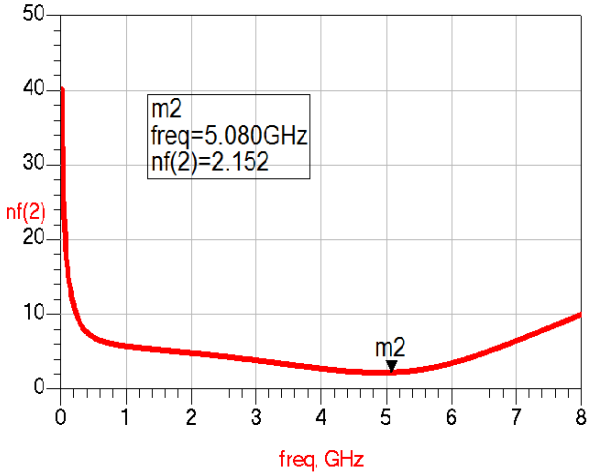

Fig. 5Noise Figure Vs Frequency

The targeted noise figure for this project is less than 3 dB for the frequency band which is 5 GHz. The noise figure was simulated using the ADS simulator.Noise figure is required to be very less. In the implemented design, the overall noise figure is 2.1dB as shown in Figure 5.

While designing any amplifier, it is important to check the stability of the device chosen, or the amplifier may function as an oscillator. Unconditional stability means that with any load present to the input or output of the device, the circuit will not become unstable – will not oscillate. Instabilities are primarily caused by three phenomena: internal feedback

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of the transistor, external feedback around the transistor caused by external circuit, or excess gain at frequencies outside of the band of operation.

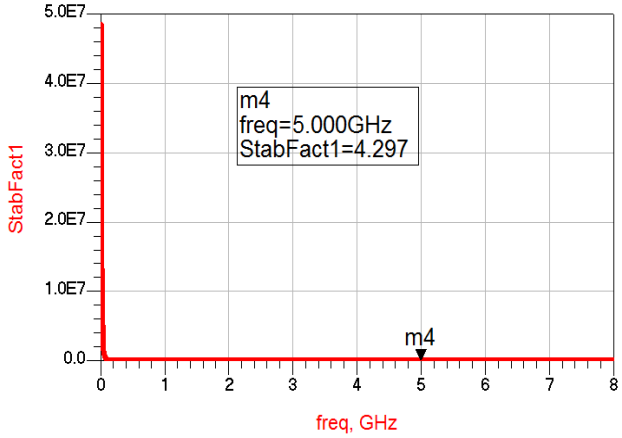

Fig. 6 Stability Vs Frequency

Stability of the designed circuit is 4.2 which is greater than 1. It means the amplifier is having good stability and there are not any oscillations. Also, the circuit is unconditionally stable.

When signal passed through input port, complete signal will not passed to the output port. Some amount of signal will return from input port, this is nothing but the input return loss.Inputreturn loss (S11) is measured at the same port to calculate loss due to incident and the reflected signal. The ideal value of S11 should be below -10 dB. It shows signal reflected at port 1 for the incident signal at port 1.

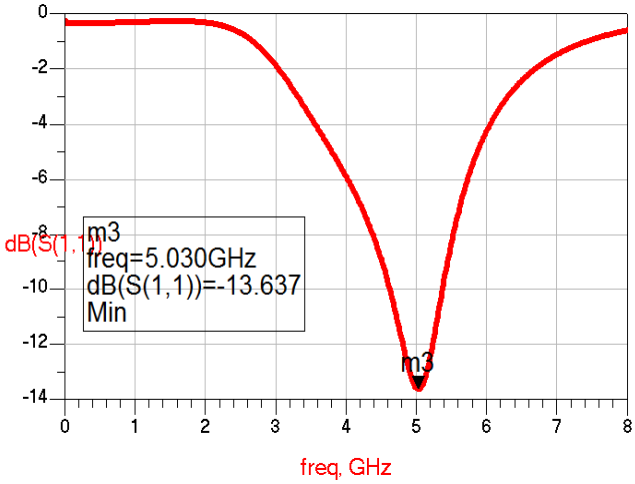

Fig. 7 Input Return Loss Vs Frequency

Figure 7 shows the input return loss S (1, 1) measured at the input port 1. The S11 value is -13 dB at 5GHz.

When signal came back from the other block connected to low noise amplifier i.e. mixer, complete signal will not passed to the input port. Some amount of signal will return from output port, this is nothing but the output return loss.Similarly the S22 at the output port also should be below -10 dB.

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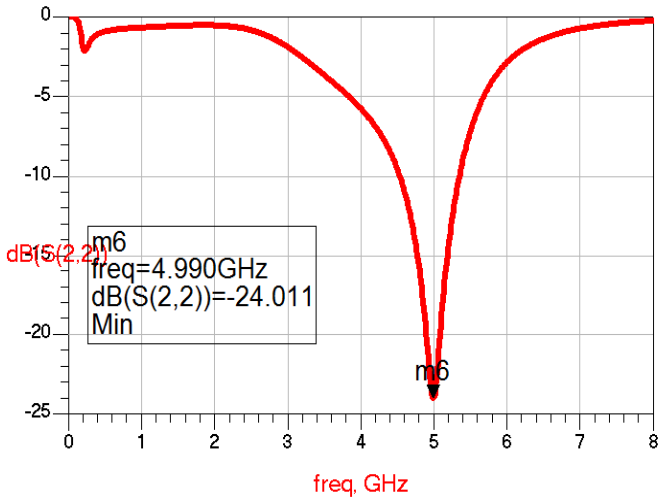

Fig. 8 Output Return Loss Vs Frequency

Figure 8 shows the output return loss S (2, 2) measured at the output port 2. The S22 value is -24 dB at 5GHz.

When the signal receives by antenna is weak transfer to the low noise amplifier which increases the signal strength. This increase signal strength is nothing but the gain of the amplifier.

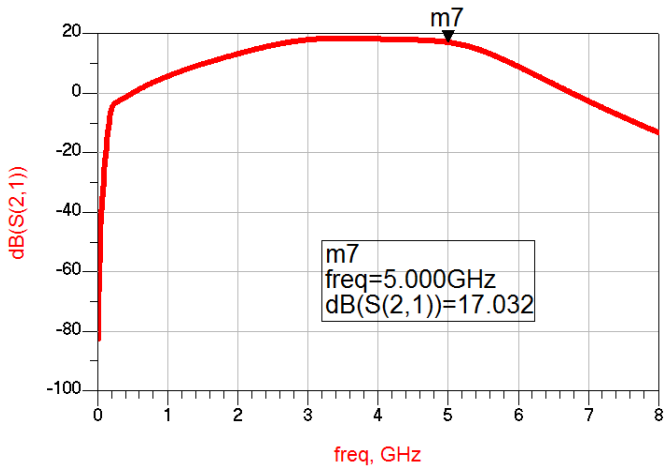

Fig. 9 Gain Vs Frequency

Figure 9 shows the gain S (2, 1) of the overall circuit. Gain is 17 dB at 5 GHz.

Isolation prevent low noise amplifier from the signal which is connected second to the LNA.

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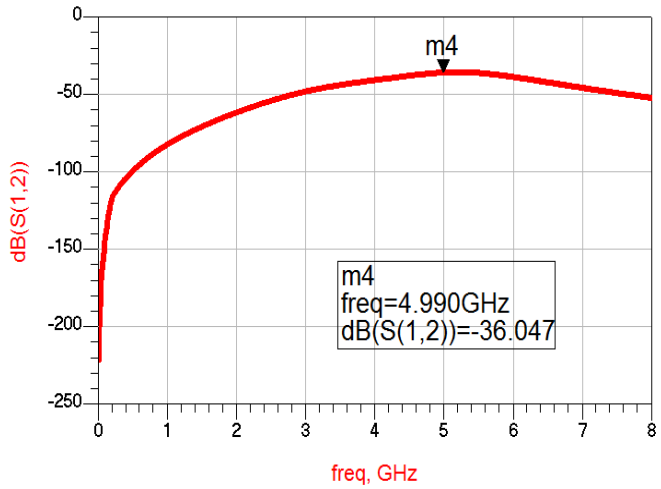

Fig. 10 Isolation Vs Frequency

Figure 10 shows the isolation S (1, 2) of the overall circuit which is -36 dB.

VIII.CONCLUSION

The amplifier is showing excellent gain, stability, noise figure, and input/output return loss. The simulation results show that the designed integrated circuit can meet the requirements of LNA. Complete LNA schematic is simulated in Agilent's ADS through 0.13µm CMOS technology generates 17 dB voltage gain (S21), 2.1 dB noise figure (NF), -13 dB input return loss (S11) and output return loss(S22) is -24 dB. Also, the stability factor is 4.2 at 5 GHz frequency with voltage supply of 0.6V.

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