



Three Level Boost PFC Converter for High Voltage AC-DC Applications

Aswathi P¹, Manjusha V A²

PG Scholar (Power Electronics and Power Systems), Dept. of EEE, Amal Jyothi College of Engineering, Koovapally, Kerala, India¹

Assistant Professor, Dept. of EEE, Amal Jyothi College of Engineering, Koovapally, Kerala, India²

ABSTRACT: In the present situation, the evolution of growing in of computers, laptops, uninterrupted power supplies, telecom and biomedical equipment has become overpowering. Hence the utilization of such equipment results high power consumption and small power density which provided a large market to Distributed Power System (DPS). Power conditioning, typically rectification is essential usually for electronics equipment. Rectifier behaves as nonlinear load producing non sinusoidal line current due to the non-linear input characteristic. The steady growth of use of electronics equipment is become a significant problem as per the line current harmonic is concerned. Their adverse effects on the power system are many. Hence in three-phase systems, the neutral current magnitude increase and becomes the cause of overheating of transformers and induction motors, as well as the dreadful conditions of system voltage waveforms. A reduction in line current harmonics or Power Factor Correction (PFC) is vital. Boost converter when used in high voltage applications makes the system bulky. Three Level Boost PFC Converter was designed for high voltage applications for improving PF and reduce THD. A controller was tested using MATLAB/SIMULINK for the voltage balancing across the capacitors and PFC of the three level Boost PFC converter. An experimental prototype has been made for low voltage applications. A comparison of the conventional and new converter is done for low and high voltages.

KEYWORDS: Three level Boost Converter, Power Factor Correction, SMR, Multiloop Interleaved control, Capacitor voltage balancing.

I. INTRODUCTION

In industry most of the load is inductive in nature which results in lagging power factor that is why there is loss and wastage of energy which results in high power bills and heavy penalties from electricity boards. If the load is uneven it is very difficult to maintain unity power factor. The devices generally used in industrial, commercial and residential applications need to undergo rectification for their proper functioning and operation. They are connected to the grid comprising of non-linear loads and thus have non-linear input characteristics which results in production of non-sinusoidal line current. Also current comprising of frequency components at multiples of line frequency is observed which lead to line harmonics. Due to the increasing demand of these devices, the line current harmonics pose a major problem by degrading the power factor of the system thus affecting the performance of the devices. Hence there is a need to reduce the line current harmonics so as to improve the power factor of the system. This has led to designing of Power Factor Correction circuits which maintains unity Power Factor. PFC is done in order to reduce the power transmission losses and increase the system stability. PFC circuits needs to shape the input current waveform and regulate output voltage simultaneously. Different methods like active and passive PFC topologies are thereto obtain PFC functions.

II. LITERATURE REVIEW

There are mainly two types of power factor correction methods are used. Active PFC topologies are advantageous over the passive topologies in PFC applications.



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

A. Passive PFC

The easier way to control the harmonic current is to use a passive filter which passes current only at line frequency. This can be done by adding an inductor in series at the AC side of the nonlinear load (rectifier), placing inductor at the dc side, using combinations of low-pass input and output filters or using harmonic trap filter etc. Passive filter reduces the harmonic current, in a non-linear device by exhibiting linear characteristics. But these filters are large, expensive and bulky which requires high current inductors [1]. Passive methods of PFC have certain advantages. They are simple and reliable. The generation of high frequency electromagnetic interference (EMI) and switching losses due to high frequency are getting reduced. But, they are also well known for their drawbacks. Passive filters are heavy and bulky. Its dynamic response is very weak, voltage regulation is very poor and the shape of its input current depends on the load. The fundamental component may show an excessive phase shift, even if the line current harmonics are reduced and it will reduce the power factor.

B. Active PFC

An active power factor corrector improves the power factor by using different types of dc-dc converters the main aim is to make the load circuitry purely resistive. The active power factor correction circuits can be selected as single-stage or multi-stage [2]. They are mainly of three types i.e. buck converter, boost converter and buck-boost converter topology having a self PFC capability which helps in improving the PF. Power factor correction using Buck converter topology and its advantages are presented in [3] and [4].

Boost converter topology used for PFC is outlined in [4]. In ac-dc Bridgeless Boost topology the output diodes operated in high voltage have severe reverse recovery problems due to high diode forward current and high output voltage. As the switching frequency increases the large reverse recovery currents of the output diodes affect the switches in the form of additional turn on losses and also produce electromagnetic interference (EMI) noises. Interleaved, half and full bridge Boost topologies are outlined in [4]. The main problem with operation of dc-dc converters are unregulated power supply, which leads to improper function of dc-dc converters. So various types of control schemes are used to enhance the efficiency of dc-dc converters [5].

The idea of having circuits that generate three-level (TL) voltage waveforms can be traced back to two U.S. patents in the early 1960s. These TL circuits were invented for computer applications with the intention of transforming conventional computation methodology from binary logic form to ternary form. Later, Nabae *et al.* and Baker reported a different form of TL circuits specific to power conversion application in 1980 and 1981, respectively named the neutral-point-clamped (NPC) inverter the phase leg of this inverter can output not only the positive and negative bus voltages but also the neutral-point voltage. As a result, the output voltage of the NPC inverter has lower harmonics as compared to that of traditional inverters. Since the phase leg provides three levels of voltages, the NPC inverter is also called TL inverter. An additional advantage of the TL inverter is that the voltage stress of the switches is reduced to half of the input voltage, which makes it suitable for high input voltage power conversions the technique has application to dc-dc converters by Pinheiro and Barbi to reduce the voltage stress of the switches the application of which does not create a TL voltage state. Since the phase leg of this dc-dc converter is similar to that of the TL inverter it was named TL converter. The concept was applied to the Multilevel DC-DC converters.

The control methods for the three-level SMR (ac/dc application) can be found in [6] where gate signals $GT1$ and $GT2$ are generated from the lookup table with inputs $H1$, $H2$, and $H3$. It can be found that sensing capacitor voltage is required for the generation of inputs $H2$ and $H3$. Therefore for the control of the three-level SMR, it is necessary to sense individual capacitor voltage and to add voltage balancing loop in [8]. Similar voltage balancing loops can be also found in the dc/dc applications [8], [9].

III. THREE LEVEL BOOST PFC CONVERTER

Three level boost PFC converter consists of diode bridge rectifier, three level boost dc-dc converter supplying load and appropriate controller. Block diagram of the system is shown in Figure 3.1.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

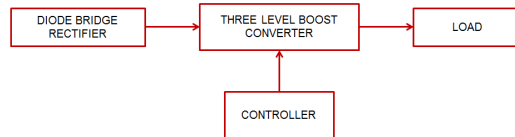


Figure 3.1 Block diagram of Three level Boost PFC Converter

The input ac voltage $V_s = V_m \sin(\omega t)$ is a sinusoidal function with peak amplitude V_s . Through the diode rectifier, the input voltage of the three level boosting converters can be expressed with the rectified voltage V_s . By assuming that the switching frequency f_s is much larger than the line frequency f , the control signals v_{cont1} and v_{cont2} can be regarded as two constants within the switching period $T_s = 1/f_s$. The ideal inductor and the ideal capacitors are assumed. They are the inductor resistance and the capacitor resistances are assumed zero.

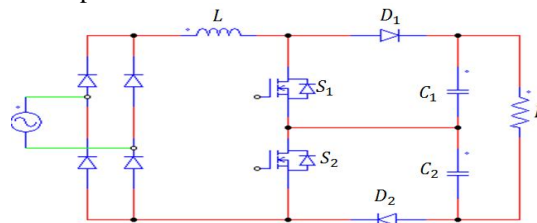


Figure 3.2 Three level Boost PFC Converter

In two level boost converter only one active switch is used and this leads to 2 (2 number of active switches=2) operating modes (0 or 1). In the Three Level Boost (TLB) converter two active switches (S_1 and S_2) are used and consequently 4 (2 number of active switches=4) modes are available (00, 01, 10, 11). The output has a capacitor voltage divider. The increase in the operating modes and thus switching states will lead to n additional control freedom to charge and discharge the dc link capacitors independently. The circuit diagram is shown in Figure 3.2.

The voltage of the centre point is $V_d/2$, which is obtained by choosing C_1, C_2 and the symmetrical operation of the two boost switches. Due to the input inductor L and two diodes D_1 and D_2 in the three level boosting PFC converter, both switches can be conducting at the same time without the concern of the short circuit damage. As shown in Figure there are four switching states in the three level boosting PFC converters.

Mode 1: As shown in Figure 3.3 both switches turn on in the switching state 1. Thus the inductor voltage V_L in the three level boosting PFC converters equals the rectified input voltage $V_L = v_s$ and both capacitors supply energy to the load $i_{C1} = i_{C2} = -i_d < 0$. In this mode the inductor is always in charging mode and charged capacitors supply the current to the load.

$$V_L = v_s \quad (3.1)$$

$$i_{C1} = i_{C2} = -i_d \quad (3.2)$$

$$= v_{C1} + v_{C2} \quad (3.3)$$

Mode 2: In the switching state 2 in Figure 3.4, the top switch turns on and the bottom switch turns off. The resulting inductor voltage V_L equals the rectified input voltage minus the bottom capacitor voltage. The capacitor C_1 supplies energy to the load. But the capacitor C_2 stores the energy from the input voltage i.e. is in charging mode. Similarly the resulting inductor voltage in equals the rectified input voltage minus the top capacitor voltage. In this mode inductor may be in charging mode or discharging mode.

$$V_L = v_s + v_{C2} \quad (3.4)$$

$$i_{C1} = -i_d \quad (3.5)$$

$$i_{C2} = i_L - i_d \quad (3.6)$$

$$v_d = v_{C1} + v_{C2} \quad (3.7)$$

Mode 3: In the switching state 3, the top capacitor C_1 is in charging mode but the bottom capacitor C_2 is in discharging mode i.e. it supplies the load current. In this mode inductor may be in charging mode or discharging mode

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

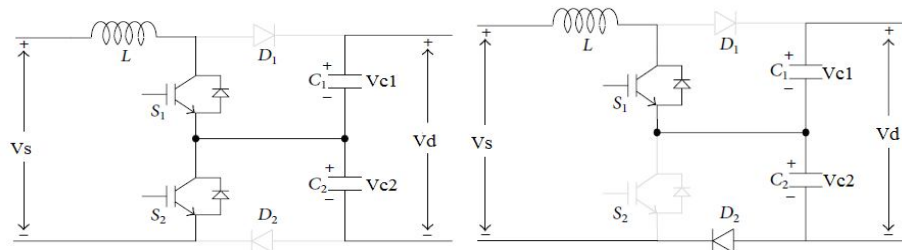


Figure3.3Mode 1

Figure3.4Mode 2

$$v_L = v_s + v_{C1} \quad (3.8)$$

$$i_{C1} = i_L - i_d \quad (3.9)$$

$$i_{C2} = -i_d \quad (3.10)$$

$$v_d = v_{C1} + v_{C2} \quad (3.11)$$

Mode 4: When both switches turn off in Figure 3.5, the resulting inductor voltage equals the rectified input voltage minus the output voltage. The rectified input voltage supplies the load current and charges both capacitors simultaneously. Due to boosting operation $v_{C1} + v_{C2} > V_s$, so in this mode inductor always is in discharging mode and both capacitors are in charging mode and input supplies the current to the load.

$$v_L = v_s - v_{C1} - v_{C2} \quad (3.12)$$

$$i_{C1} = i_{C2} = i_L - i_d \quad (3.13)$$

$$v_d = v_{C1} + v_{C2} \quad (3.14)$$

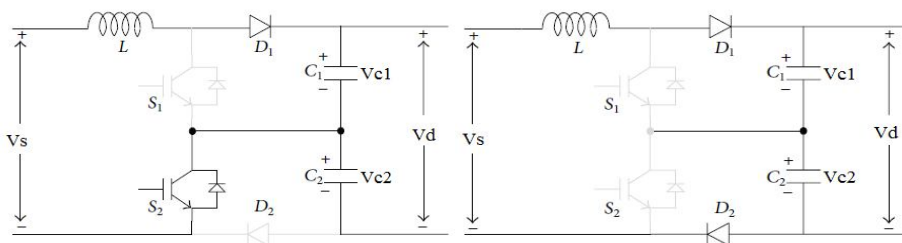


Figure3.5Mode 3

Figure3.6Mode 4

Two gate signals of switches GT1 and GT2 are generated from the comparisons of control signal and two unit sawtooth signals v_{tri1} and v_{tri2} . Two sawtooth signals have unit amplitude and identical period T_s and there is a 180deg phase difference between them. Both duty ratios of switches are equal to the control signal. As the two carrier triangular signals intersect at duty ratio 0.5 there are two regions where this converter can operate depending on whether the input voltage is lower or higher than half of the output voltage.

In region 1, $V_s > V_d/2$; hence $V_L = V_s - V_d/2 > 0$ so inductor current raising polarity is positive in modes 3 and 2 as shown in Figure. This will occur only when duty ratios of upper switch SW2 and of lower switch SW1 are less than 0.5. In this region both switches must not be ON at the same time.

In region 2, $D1 = D2 > 0.5$, input voltage is $V_s < V_d/2$ then, inductor current raising polarity is negative $V_L = V_s - V_d/2 < 0$ in modes 2 and 3 as shown in Figure. In this region both switches must not be OFF at the same time. The operating modes in two regions are as shown in Figure 3.7 and 3.8.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

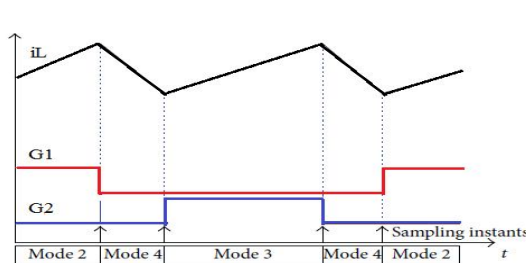


Figure 3.7 Region 1

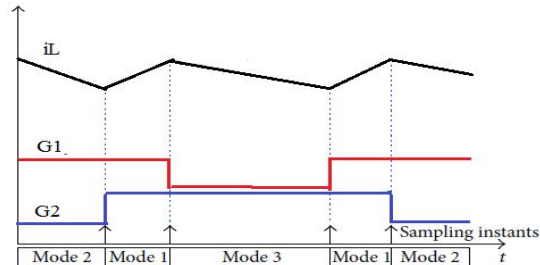


Figure 3.8 Region 2

DESIGN EQUATIONS

Inductor value capacitor values and ripple in inductor current is obtained as shown in equations.

$$L = \frac{V_d}{4f_s} \Delta I \quad (3.15)$$

$$C_1 = C_2 = \frac{I_d}{2\omega \Delta v_{c1}} \quad (3.16)$$

$$I_d = \frac{P}{V_d} \quad (3.17)$$

$$\text{For } V_s < \frac{V_d}{2}, \Delta I_{max1} = V_{in} T_s D / 2L$$

$$\text{For } V_s > \frac{V_d}{2}, \Delta I_{max2} = V_s - 0.5V_d T_s D / 2L$$

$$\Delta I_{max} = V_s T_s / 16L$$

The voltage equation of three level boost converters is shown below.

$$V_d / V_s = 2 / (1 - D) \quad (3.18)$$

CONTROL STRATEGY

Control combines the conventional multi loop control, the feed forward loop, and the interleaved PWM scheme. Both the voltage controller and the current controller are proportional integral type controllers (PI). Two gate signals GT1 and GT2 are generated from the comparisons of control signals v_{cont1} and v_{cont2} (v_{cont}) and two unit sawtooth signals v_{tri1} and v_{tri2} , respectively. The two sawtooth signals have unit amplitude and identical period T_s . There is a 180 phase difference between them. Both duty ratios of switches $SW1$ and $SW2$ are equal to the MIC control signal v_{cont} .

Both current and voltage controllers are PI controllers. Inner current controller is used for current shaping. Outer voltage controller is used for voltage regulation. In the outer voltage loop, the current amplitude is obtained by the voltage controller and the error voltage is the difference between the output voltage command V_d^* and the output voltage V_d . Then the peak value of the input current multiply with the rectified signal to ensure the inductor current command is in phase with the rectified input voltage. In the inner current loop, the inductor current command minus sensed inductor current to obtain the current error. The multi loop interleaved control with conventional capacitor voltage balancing control (CVBC) shown in Figure 3.8. One control signal is generated by the multi loop control, and the other control signal is yielded by CVBC with sensing the capacitor voltages. The average value current I_L is input to the multi loop control to yield the desired PFC function and obtain the control signal v_{cont1} . The difference I_{vC} between two values I_{vC1} and I_{vC2} is calculated and the compensating signal v_{cont} is obtained by the P controller.

$$\Delta v_{cont} = k_p (I_{vC2} - I_{vC1}) \quad (3.19)$$

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

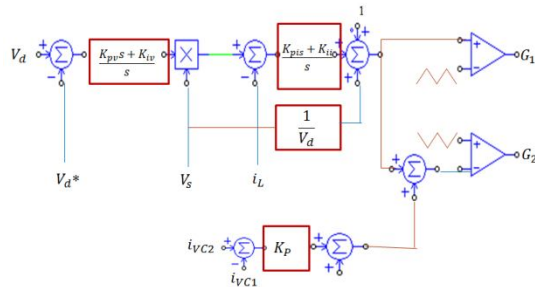


Figure 3.7 Multiloop interleaved control

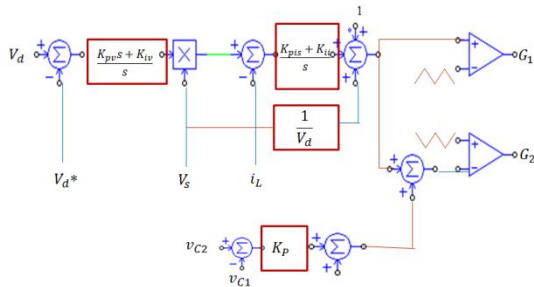


Figure 3.8 Sampling and control strategy

Current sampling technique is required for sampling the inductor current. There is no capacitor voltage sensing and balancing is done by sensing the input voltage, inductor current and output voltage. So a signal is saved. It reduces cost, complexity. The figure shows the sampling of inductor current. The multi loop interleaved control and the SCVBC with the sampling and hold strategy is shown above where only the input voltage, the output voltage v_d and the inductor current i_L are sensed. Then, the other control signal v_{cont2} is generated by adding the compensating signal to the control signal v_{cont1} .

$$v_{cont2} = v_{cont1} + \Delta v_{cont} v_{cont1} + k_p (i_{vC2} - i_{vC1}) \quad (3.20)$$

The sampling/hold strategy samples the inductor current thrice per switching period T_s and obtains the average value i_L and the other two values i_{vC1} and i_{vC2} . Proportional controller value is obtained by equation below.

$$0 < k_p < 2L/T_s i_{vC2 \max} \quad (3.21)$$

IV. SIMULATION ANALYSIS

Software simulation of the power factor correction circuit with single phase diode bridge rectifier is done in MATLAB/Simulink. In the sample circuit of the considered system, a single phase diode bridge rectifier having four diodes connected in two arms is taken as the non-linear load. The input supply is 110V and the switching frequency is set to 20 kHz. The inductor and capacitor values taken are 0.5mH, 2240 μ F and 1410 μ F respectively.

A. Simulink Model of open loop PFC Three Level Boost PFC Converter

Open loop operation of Three level Boost PFC Converter is as shown in figure. The converter operates with input of 110V. The power factor obtained is 0.98. The output voltage remains regulated at 330V but with the presence of voltage transients. The waveforms are shown below at 300W.

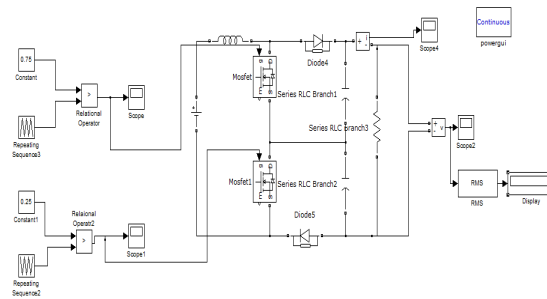


Figure 4.1 Simulink model of Open loop Three level Boost

The output voltage waveform is as

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

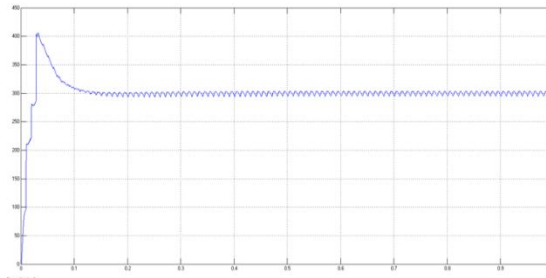


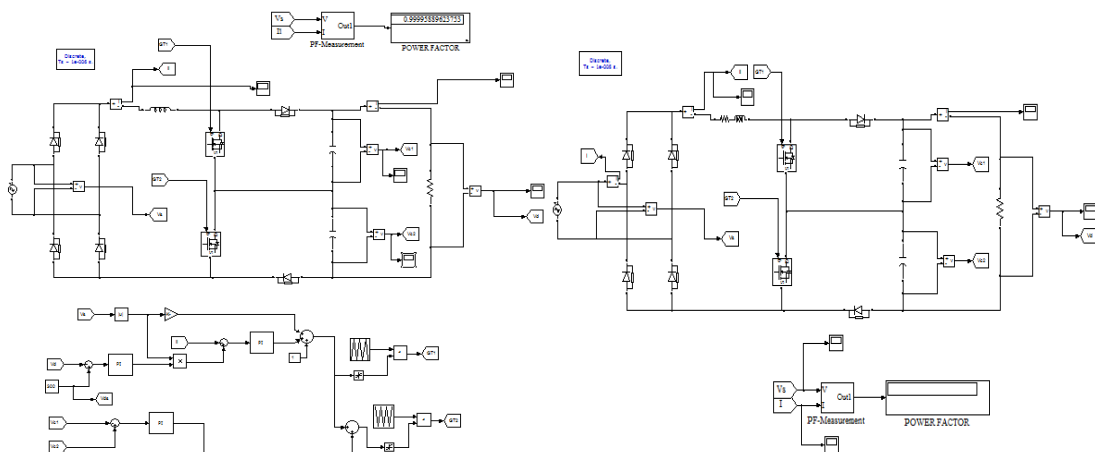
Figure 4.2 Output Voltage Waveform of Open loop Three level Boost Converter

B. Simulink Model of Closed loop PFC Three Level Boost PFC Converter

The Simulink model of the Three level Boost PFC Converter with Multiloop Interleaved control and the control with the help of sampling and control strategy is shown Figure 4.4 . The input voltage and current obtained are sinusoidal with power factor of 0.99995 and 0.99997 respectively. Output voltage remains regulated at 300V with fewer transients. The three level Boost PFC Converter with SCVBC designed for high voltage has high PF of 0.99997 and low THD of 9% compared with that of low voltage design with PF of 0.9997 and high current harmonics. The comparison table of different parameters is as shown. Three level Boost converter also obtained better PF and low current harmonics compared to the conventional Boost converter.

Table 4.1 Comparison of different parameters

Duty cycle (%)	Load (ohm)	Power rating (W)	Power Factor	THD
10	1500	60	0.999	9.54
20	750	120	0.9999	9.51
50	300	300	0.9998	9.41
100	150	600	0.9984	9.25

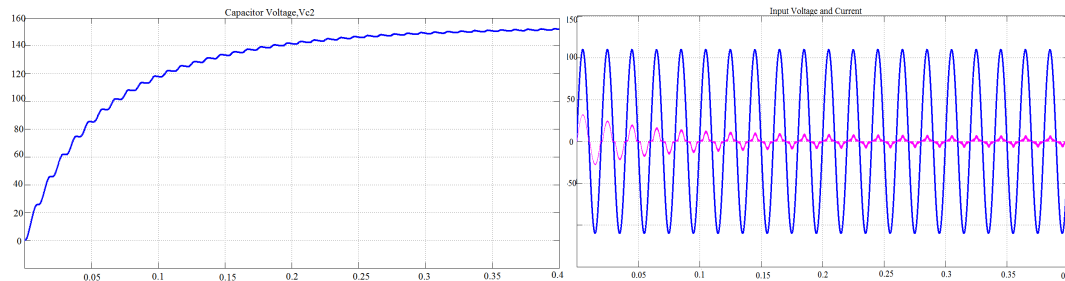


The capacitor voltages obtained remains regulated at 160V.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

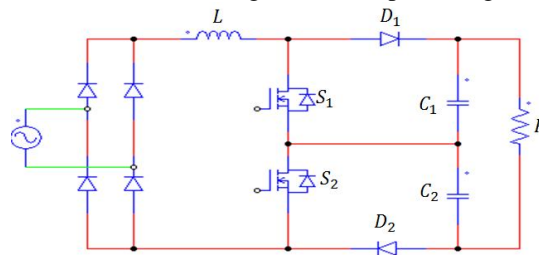
(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

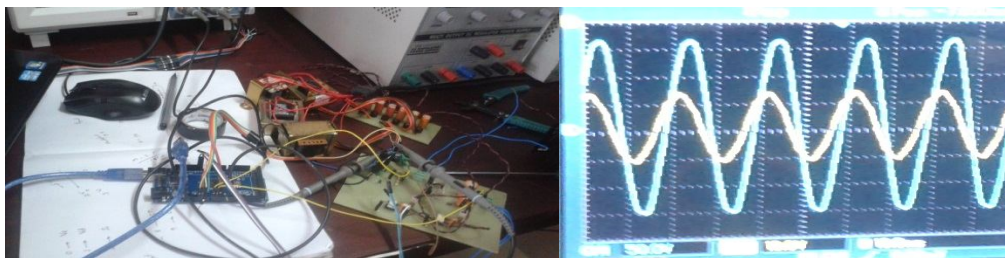


V. HARDWARE RESULTS

A prototype of single phase closed loop Three Level Boost converter topology, for PFC is modelled at 1kHz switching frequency. The components includes MOSFET (IRF640) used as the switch, Diodes (IN4007), Capacitors (220 μ F, 300 μ F), Inductor (60mH) and Resistor (300K) as load. Power supply unit is used to generate regulated power supply. The output 12V of the transformer is rectified with the help of diode bridge rectifier and fed to the driver circuit as input. The driver output of 12V is used to drive the Power switches. The varying gate pulse to the switch is generated with the help of Arduino Mega. The circuit of three level boost converters is used in PFC high voltage applications. Here a prototype model of the converter is designed for low voltages with input of 15V. The hardware circuit diagram of the prototype model is as shown in Figure 5.1. Output voltage remained regulated at 50V.



Improved power factor was obtained. Input voltage and current waveforms obtained in DSO are as shown in Figure 5.3.



VI. CONCLUSION

Traditional diode rectifiers are commonly used for AC to DC power conversion. These electrical equipments generate harmonic waves and suffer low power factor. Now converters with power factor correction have received greater attention due to improved power factor and low harmonics. The Three Level Boost PFC topology has the ability to regulate the output voltage to a desired value by varying the duty ratio. Three Level Boost PFC circuit with open loop control and closed loop Sampling and Control strategy is simulated in MATLAB/Simulink. In closed loop control the input power factor is better than the open loop control. The power factor is improved to a value 0.9998 and the input voltage and current waveforms are in phase to each other. A prototype is also designed in low voltages and implemented using PCB, the converter shows an excellent ability to improve the input power factor of the system.



ISSN (Print) : 2320 – 3765
ISSN (Online) : 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

REFERENCES

- [1] B. Singh, N. Singh, A. Chandra, K. Al-Haddad, A. Pandey and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," ACTA ELECTROTECHNICA, vol. 48, no. 1, pp. 962-981, October 2007.
- [2] Damodhar Reddy K. Pavan Kumar Goud, "Analysis of different topologies for active power factor correction using DC-DC converters," International Journal of Advanced Technology & Engineering Research", vol. 4, no. 1, pp. 1045-1053, January 2014.
- [3] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up DC-DC converter with coupled-inductor and voltage-doubler circuits", IEEE Transactions on Industrial Electronics, vol. 58, no. 9, pp. 4196-4206, September 2011.
- [4] A. Shahin, M. Hinaje, J. P. Martin, S. Erfederici, S. Rael and B. Davat, "Novel high step-up DC-DC converter with coupled-inductor and voltage-doubler circuits", IEEE Transactions on Industrial Electronics, vol. 58, no. 9, pp. 4196-4206, September 2011.
- [5] Xinbo Ruan, Qianhong Chen, "Fundamental Considerations of Three-Level DC-DC Converters: Topologies, Analyses and Control," Control, IEEE Transactions on Circuits and Systems, vol. 55, no. 11, pp. 3733-3743, December 2008.
- [6] Xinbo Ruan, Qianhong Chen, "Fundamental Considerations of Three-Level DC-DC Converters: Topologies, Analyses, and Control," Control, IEEE Transactions on Circuits and Systems, vol. 55, no. 11, pp. 3733-3743, December 2008.
- [7] V.I. Meleshin, D.V. Zhiklenkov, "Efficient Three-Level Boost Converter for Various Applications", Control Conference, EPE-PEMC 2012 ECCE Europe, pp. 91-98, April 2012.
- [8] B. R. Lin, H. Lu, "A novel PWM scheme for single-phase three-level power-factor-correction circuit", Transactions on Energy Conversions, vol. 47, no. 2, pp. 245-252, April 2000.
- [9] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter", IEEE App. Power Electron. Conf., pp. 434-439, 1995.
- [10] Hung-Chi Chen, Jhen-Yu Liao, "Design and implementation of sensorless capacitor voltage balancing control", IEEE Transactions on Power Electronics, vol. 29, no. 7, pp. 2319-2327, July 2014.