ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2015

DC Capacitor Voltage Equalization in Multi-level Neutral Clamped Inverters for DSTATCOM Application

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ABSTRACT: Multilevel neutral point clamped (NPC) inverter systems are increasingly used in load compensation applications. However, the most significant problem associated with these compensators is the capacitor voltage imbalances and drift due to dc components in the zero sequence current, resulting in degradation of tracking performance of the voltage source inverter. This paper proposes a carrier-based pulse width modulation control for an inverter-chopper circuit in order to regulate the capacitor voltages to their reference values. To demonstrate the simplicity and effectiveness of the aforementioned control scheme, a three-phase four-wire five-level NPC compensator system is taken as an example.

KEYWORDS: Distribution Static Compensator (DSTATCOM), hysteresis band current control, instantaneous symmetrical component theory, voltage source inverter (VSI).

I.INTRODUCTION

Multilevel neutral point clamped (NPC)inverters are becoming increasingly popular in widespread applications [1], [2].In order to achieve different voltage levels, the inverters rely on split-capacitor configurations. Due to various reasons like unequal capacitance leakage currents, asymmetrical tracking of current, unequal delays in semiconductor devices, the presence of dc components in the neutral current, etc., the capacitor voltages drift away from the reference values, degrading the performance of the inverter. A number of techniques have been suggested in literature to overcome this dc voltage imbalance problem in the capacitors. A carrier based pulse width modulation method is attempted for voltage balancing in flying-capacitor inverters, as suggested in [3].However, voltage balancing is easier in flying-capacitor configuration than in diode clamped inverters because of the absence of leg-voltage redundancies in diode clamped inverters. The advantage of redundant switching states is exploited in [4]–[6] to counter the drift in capacitor voltages. Some techniques require the switching of appropriate space vectors for balancing [7]–[10]. However, low modulation index and power factors limit the voltage control. Most of the aforementioned methods can correct only minor imbalances in the voltages and are not suitable for load compensation applications. This is due to the requirement that the compensator currents tracked by the compensator have to closely follow the reference instantaneously .Hence, the switching states of the inverter operated in the current controlled mode are exclusively governed by the current controller, and it may not be possible to command the switching state, which can counter the voltage imbalance. An elegant way of paralleling the capacitor cells to balance the charges has also been attempted [11]. However, this technique, when applied to a load compensation application, requires a combination of eight switches for paralleling using an auxiliary capacitor, to enable bidirectional transfer of energy.

A method of achieving both voltage balance as well as power factor correction capacity is presented in[12]. However, this capability is obtained only with a back-to-back connection of a multilevel rectifier with the multilevel inverter. Balancing issue in a diode clamped multilevel inverter has been approached by the use of one leg in a conventional two-level mode, which compromises on the utilization of multilevel modulation potential [13].Ensuring that the active power absorptions equal to the losses in each H-bridge inverter so that voltage drift is prevented is discussed in [14].However, balancing in H-Bridge inverters, using a single dc storage capacitor for each inverter bridge ,is much easier than in split capacitors used in diode clamped inverters. The split capacitors involve the problem of maintaining the total, as well as individual voltages, constant. An inverter-chopper circuit has also been suggested for a load compensation application to achieve equalization of capacitor voltages [15].Common mode voltage elimination with dc link balancing is discussed in [16],which uses a balancing circuit

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2015

similar to the one discussed in[15]. This circuit is the simplest topology requiring only two switches and an inductor for charge balancing. This inverter chopper configuration extended to higher levels is discussed in [17].

An essential requirement for a high band width current controlled voltage source inverter (VSI) is that the capacitor voltages must be regulated to the same reference voltage V_{dcref}. However, the voltage imbalance is of minor nature whenever the zero sequence current in the neutral wire contains only ac components. However, the imbalance problem is compounded when the neutral current contains dc components. The injection of a dc component of current through the capacitors has the effect of charging one of the capacitors above its reference value and discharging the other below the reference value. The polarity of the dc current determines which one of the capacitors would charge and the other discharge. Hence, apart from resulting in dangerously high voltages across some of the switches ,the performance of the compensator also suffers degradation, due to the loss of its tracking ability. The two- quadrant chopper used to maintain equalized voltage across the capacitors is shown in Fig. 1 and consists of two switches, each with an anti parallel diode and an inductor connected between the midpoint of the capacitors and the chopper leg. The fundamental principle governing the working of chopper is the transfer of energy from one capacitor to another, whenever the voltage of one is greater than the other.

The chopper inductor aids in the transfer of this energy. As an example, if it is assumed that there is a positive dc component in the neutral current, it is evident that Vdc2 will become greater thanVdc1 over time. Hence, in order to equalize the voltages, the switch S_n is operated so that energy is transferred from the bottom capacitor to L_{ch}. Once the switch S_n is turned off, the energy in the inductor is transferred to the top capacitor through the anti parallel diode D_p. Similarly, for a negative dc component, Vdc1 will become greater thanVdc2, requiring the operation of switch S_p and diode D_n. various control strategies like single pulse control, multi-pulse control, and proportional–integral (PI) duty cycle control schemes are suggested to control the chopper [15]. However, all these strategies require the state model of the chopper circuit. The time for which each of these chopper switches must be on and off requires solution to the state equations and inversion of the state transition matrix. These complex computations have to be executed repeatedly in order to regulate the capacitor voltages to the desired reference values. Therefore, there is a need to evolve a simple control strategy to automatically regulate these voltages, without complex computations. This paper focuses on a simple carrier-based error control of the chopper, resulting in a constant frequency operation. Other issues, such as the carrier frequency used and derivation of the average neutral current magnitude responsible for the voltage drift in diode clamped inverters, are also discussed.

An example of a three-phase four-wire compensated system is taken for a load compensation application. The compensator is realized using a three-level three-leg NPC VSI, as shown in Fig. 1. Each leg consists of four switches and two clamping diodes. Each of the switches consists of an anti parallel diode connected

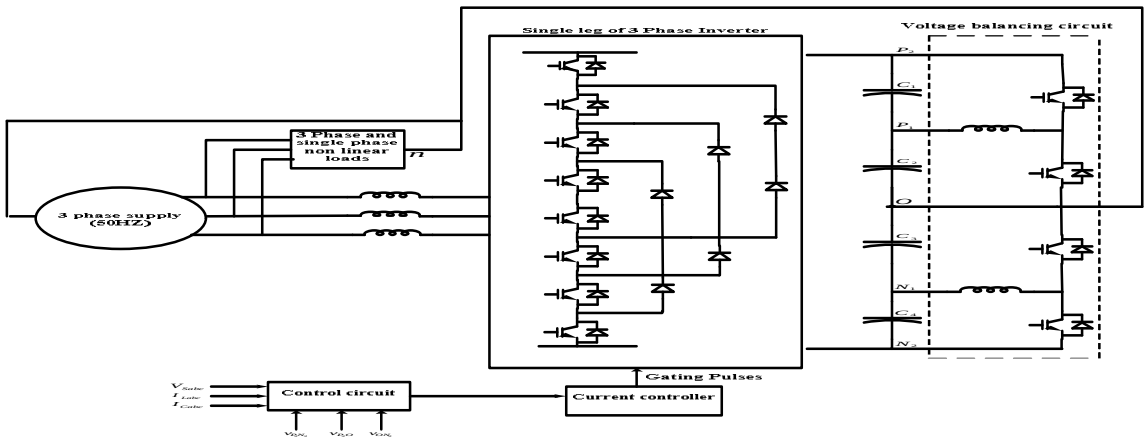

Fig.1: Circuit Configuration of the SAPF

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 4, Issue 10, October 2015

Table 1: Five Level Inverter Output Voltage, Corresponding Switching Combination and function

Output voltage	S_1 (1=close 0=open)	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output function, u
$2V_{dc}$	1	1	1	1	0	0	0	0	2
V_{dc}	0	1	1	1	1	0	0	0	1
0	0	0	1	1	1	1	0	0	0
$-V_{dc}$	0	0	0	1	1	1	1	0	-1
$-2V_{dc}$	0	0	0	0	1	1	1	1	-2

The four-wire system requires four identical capacitors C_{dc} be connected in series. The five levels achievable through this inverter are Vdc,2Vdc,-Vdc,-2Vdc and zero, referred as states+1,+2,-1,-2 0, respectively. Table I gives the output voltage across the points i(i = a, b,c) and n' for different switch combinations. As a consequence of the split-capacitor topology, balancing the voltages becomes significant to result in the proper compensation of harmonics, reactive power, and unbalances in the load. Hence, the compensator includes a chopper circuit, as shown in Fig. 1, to counter the voltage imbalances in the capacitors.

II. COMPENSATION CONTROL ALGORITHM

The reference currents (i^*_{fa}, i^*_{fb}, and i^*_{fc}) for the compensator are generated using the instantaneous symmetrical component theory [18]. When these currents are injected using the VSI into the point of common coupling (PCC), the source currents become balanced and sinusoidal. The reference currents are given by

$$i^*_{fa} = i_{la} - i_{sa} = i_{la} - \frac{v_{sa} + \gamma(v_{sb} - v_{sc})}{\Delta}(P_{lavg} + P_{loss})$$

$$i^*_{fb} = i_{lb} - i_{sb} = i_{lb} - \frac{v_{sb} + \gamma(v_{sc} - v_{sa})}{\Delta}(P_{lavg} + P_{loss})$$

$$i^*_{fc} = i_{lc} - i_{sc} = i_{lc} - \frac{v_{sc} + \gamma(v_{sa} - v_{sb})}{\Delta}(P_{lavg} + P_{loss})$$

Where, $\Delta = \sum_{j=a,b,c} v_{sj}^2$, $\gamma = \frac{\tan(\varphi)}{\sqrt{3}}$
φ being the desired power factor angle.

For a unity power factor (UPF) operation ,γ is set to zero. The aforementioned algorithm works well for any type of load that may be unbalanced, reactive, and nonlinear or any combination of the above. The term P_{lavg}, which represents the average or mean power of the load, is obtained through a moving average filter (MAF). The window size of the filter is either one full or half cycle, depending on whether the load currents contain even harmonics or not. As a consequence, the MAF gives a faster response in the case of transient load conditions. The losses of the inverter, denoted as P_{loss}, are generated using a capacitor voltage PI controller. The loss term can be given as

$$P_{loss} = K_p e + K_t \int e\, dt$$

Where K_p and K_i are the proportional and integral constants, respectively, and e is the error equal to 2Vdcref − (Vdc1 +Vdc2). As a result of the outer loop PI control action, the total voltage across the dc link is regulated at the desired value 2Vdcref by drawing the required power from the three-phase supply through a set of balanced sinusoidal currents. In other words, the sum of Vdc1 and Vdc2 is maintained constant. The expression for the load neutral current can be given as

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2015

$$i_{ln} = I_{0\text{avg}} + \sum_{n=1,2,3,\ldots}^{\infty} I_n \sin(n\omega t + \phi_n)$$

where

$$I_{0\text{avg}} = \langle i_{la} + i_{lb} + i_{lc} \rangle.$$

The symbol < > represents the average value over a cycle. If I_0avg is zero, then the neutral current is responsible only for causing ripples in the capacitor voltage whose average is zero over a cycle and does not result in significant problem if the Capacitance values are sufficiently large. Assuming a positive value for I0avg, it is evident that Vdc2 will increase and Vdc1 will reduce over time. The rate of voltage change depends on the magnitude of the dc component of the neutral current. Now, the objective of the inner loop must be to regulate the individual voltages to their reference values. Both control actions must ensure that the total voltage, as well as individual voltages, is constant for the proper tracking of the reference currents.

III. CURRENT CONTROL TECHNIQUE

In order to track the desired set of reference currents extracted through, a suitable current control technique is adopted. Hysteresis control is a widely used current control technique in most of the Distribution Static Compensator (DSTATCOM) applications because of its ease of implementation, fast dynamic response, inherent peak current-limiting capability, etc. [19]–[21]. Existing techniques in literature involve adapting the modulation period, double band modulation, etc. to achieve constant or reduced frequency of operation [22]–[24]. In the case of a three-level inverter, the zero voltage level should be applied at appropriate instants so that reduction of switching frequency is achieved. The switching logic must ensure there is no successive transition between +1 and −1 states, as this will increase the frequency of switching. In order to obtain a reduced frequency of operation and reduced tracking error, an improved three-level hysteresis current control technique has been suggested [25]. The improved scheme, using a double band switching, results in a low tracking error, low total harmonic distortion in the source currents, and lower switching losses apart from reducing the frequency of operation. This is achieved by monitoring the previous input state *u* previous (+1,−1, or 0) which has been applied. Moreover, the scheme does not require the estimation of slope of the currents to be tracked in order to insert the zero voltage level. The improved switching algorithm can be given as

The five-level hysteresis can be defined as follows
Let error, e= $i_{cabc} - i^*_{cabc}$
Where i_{cabc} = actual inverter current and i^*_{cabc}= reference compensation current
Let 'h' be the width of inner hysteresis band and δ be the width of outer hysteresis band. Then the output function is given as

$$u = \begin{cases} -2, & if\ e \geq \delta \\ -1, & if\ h \leq e < \delta \\ 0, & if\ -h \leq e < h \\ 1, & if\ -\delta < e \leq -h \\ 2, & if\ e \leq -\delta \end{cases}$$

where *error* is the difference between the reference current and the actual current injected into the PCC, h and δ are the widths of hysteresis band and dead zone, respectively, and u and u previous are the present and past input states applied, respectively.

IV. DC CAPACITORS VOLTAGE EQUALIZATION

The voltage balance between positive capacitors and negative capacitors is controlled be the voltage balancing controller which is already presented. For the voltage balance among two positive capacitors and two negative capacitors a voltage balancing circuit is required. It is described as follows.

VOLTAGE BALANCING CIRCUIT

The voltage balancing circuit consisting of two bi-directional buck-boost choppers is shown in figure 3.1. For an ideal operation of compensator no DC mean current flows into nodes P1, N1 shown in figure 3.1. But due to unequal

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charging and discharging of practical capacitances, switching losses in the inverter a small amount of DC mean current flows into nodes P1 and N1. The amount of DC current depends on the duty factor of the node and active power component of the load current which is given in [18].The effect is that one capacitor gets over charged and they would be discharged. Therefore if this DC mean current is countered by injecting equal and opposite DC current into the respective node the capacitor voltages are restored to set values. The principle of chopper operation is that transfer of energy from over charging capacitor to discharging capacitor. If i_{P1} is mean current flowing into node P1 and i_{cp} is the current through positive chopper, at steady state $i_{P1}=\bar{\imath}_{cp}$ then $V_{P2\text{-}P1}=V_{P1\text{-}O}$.

CONTROLLER FOR VOLTAGE BALANCING CIRCUIT

The controller for chopper circuit is shown in figure3.2.Controller for the positive chopper circuit is shown in the figure; the controller is similar for the negative chopper circuit.

The voltages $V_{P1\text{-}P2}$ and $V_{P2\text{-}O}$ are compared and given as input to a PI controller which ensures the voltage balance at steady state. The output of PI controller is the reference current for the chopper and is compared to actual chopper current. The error is compared with a fixed frequency triangular carrier wave and the comparator provides the current control for the chopper.

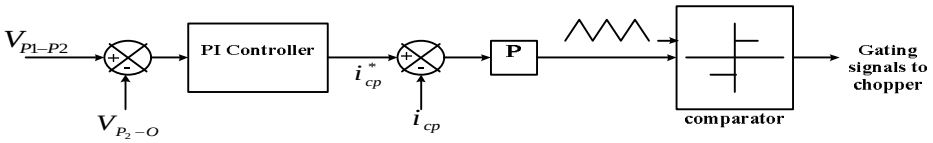

Fig 2.Current controller for voltage balancing circuit

V. SIMULATION STUDY

SIMULATION PARAMETERS

Supply voltages	200 V (L-N peak) , 50 Hz
Three phase rectifier load	30+j6.28Ω
Single phase semi-converter loads	100+j12.56 Ω
Filter inductor (L_f, R_f)	3mH, 1m Ω
Chopper inductor (L_{ch}, R_{ch})	20mH, 1m Ω
PI controller gains	K_1= 20, I_1=100, K_2=0.1, I_2=0.1, K_3=0.1, I_3=0.1, K_4=0.1, I_4=0.1
Proportional gains for chopper current controllers	0.2
outer hysteresis band, $\pm\delta$	±0.15
Inner hysteresis band, ±h	±0.05

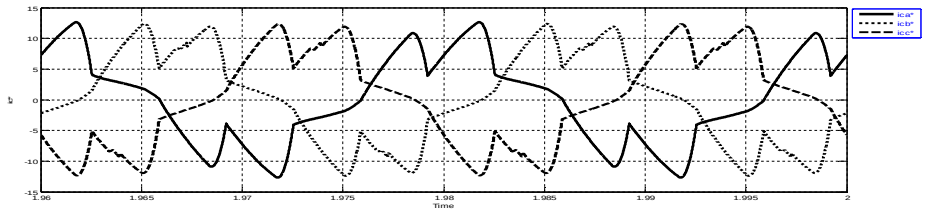

Fig 3.Referance compensation current

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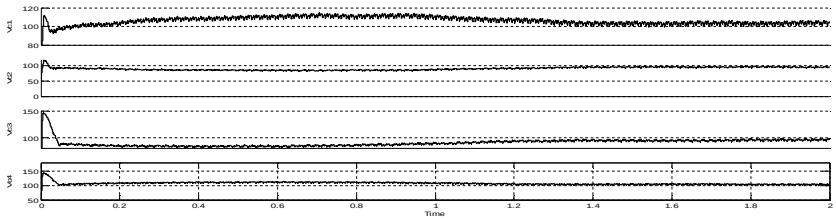

Fig 4.Capacitors voltage with Chopper circuits OFF for no DC offset in load

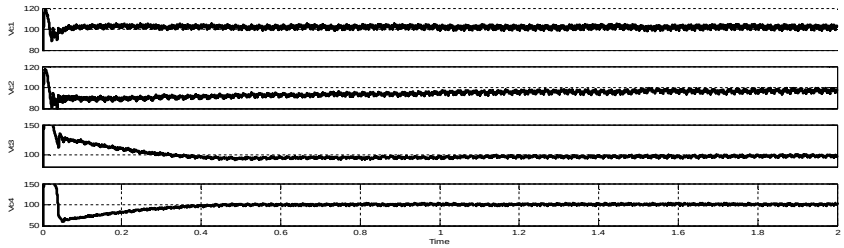

Fig 5 Capacitors voltage with chopper circuits ON for no Dc offset in load

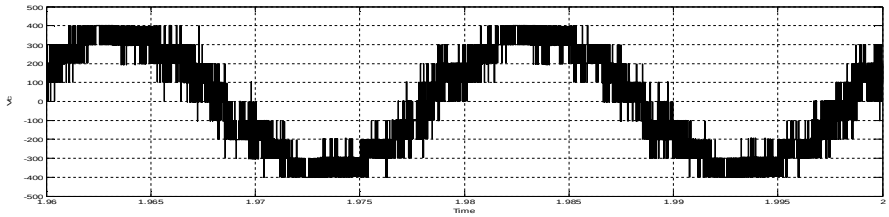

Fig 6.Line voltage at inverter ac terminals

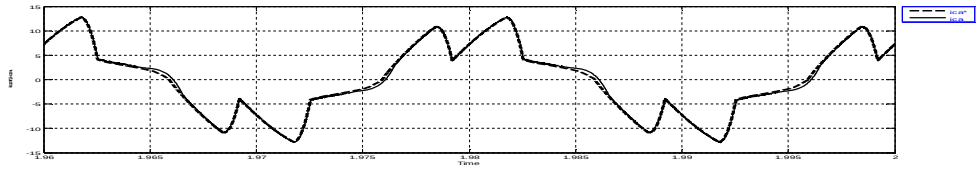

Fig 7Tracking of compensation current by inverter

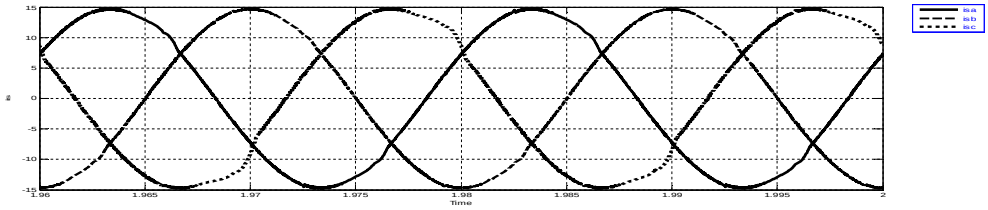

Fig 8.Compensated source currents of phases a, b and c

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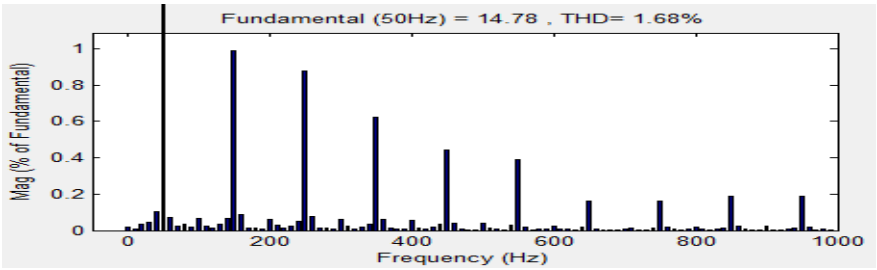
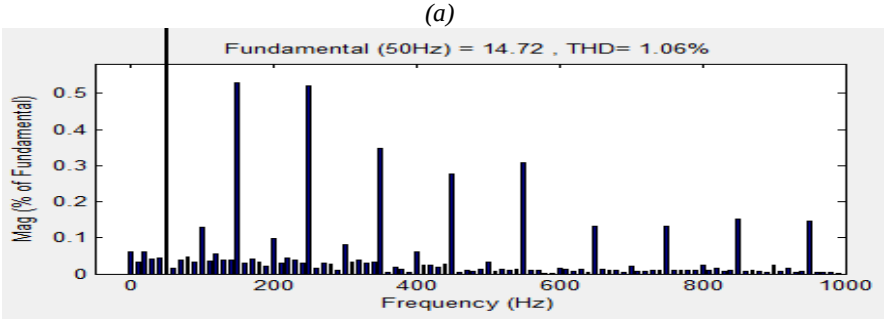
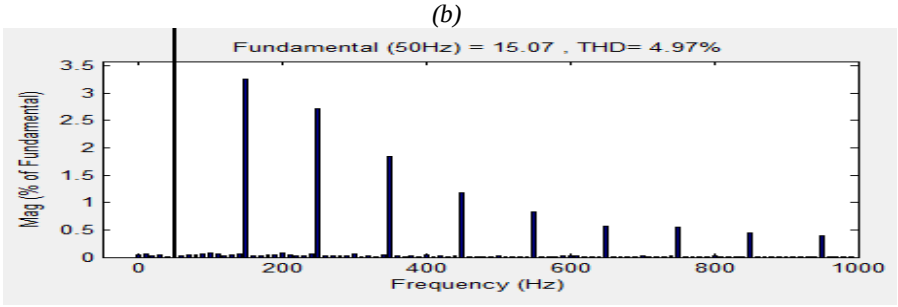


(a)



(b)



(c)

Fig 9.FFT analysis for compensated source current of(a) phase a,(b) phase b (c) phase *c*

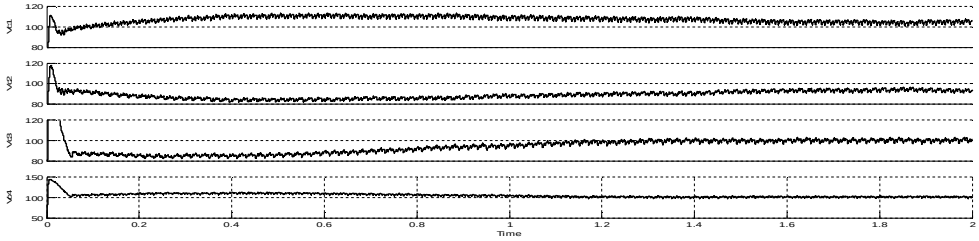


Fig 10. Capacitors voltage with DC offset in load without voltage balancing controller

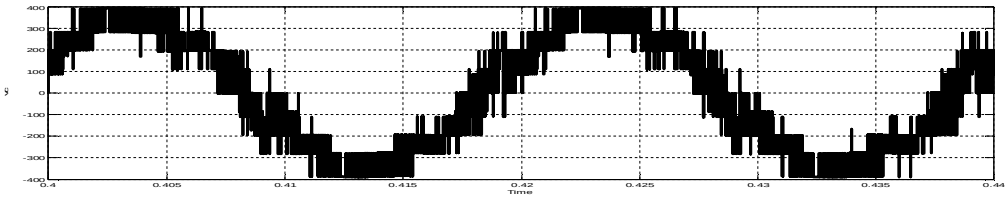


Fig 11. line voltage at inverter ac terminals with capacitor voltage imbalance

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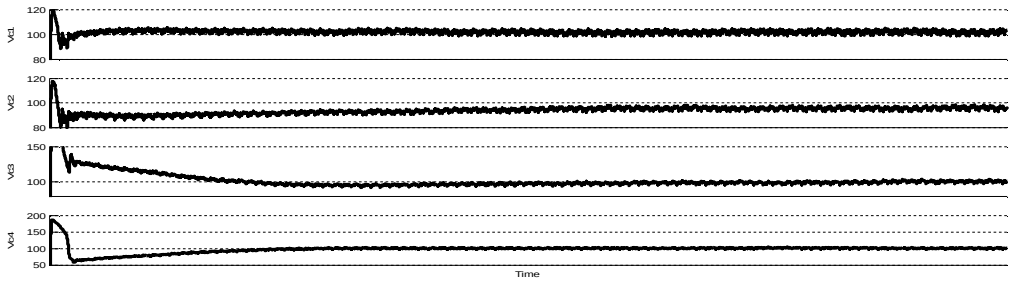
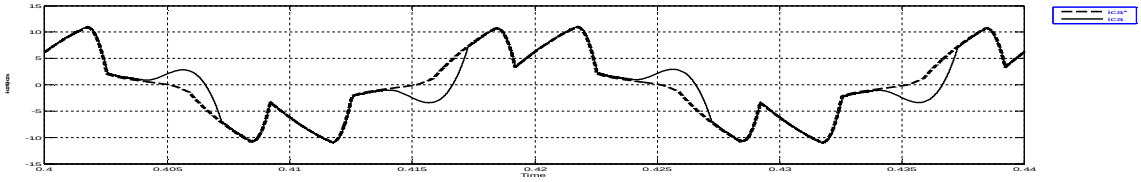
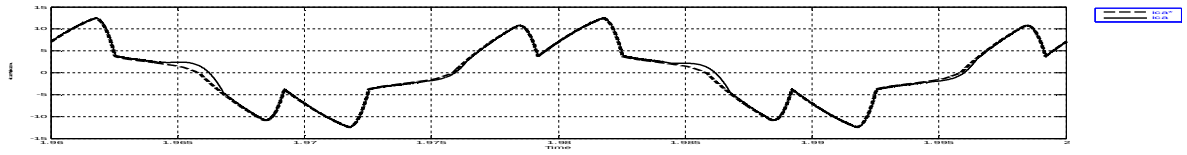


Fig 12. Capacitors voltages with voltage balancing controller and choppers ON



(a)



(b)

Fig 13. tracking of compensation current with (a) capacitors voltage unbalance (b) balanced capacitors voltage

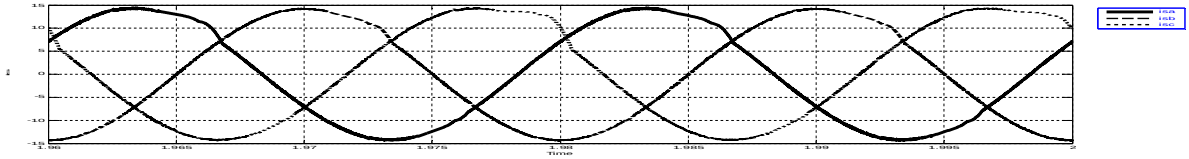
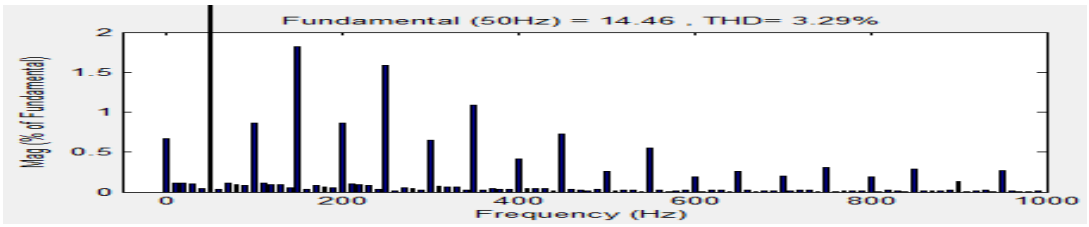
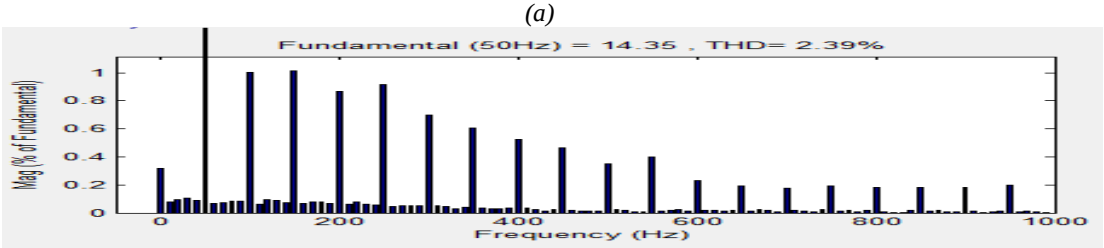


Fig 14. Source current in phase a, b and c after harmonic compensation



(a)



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ISSN (Print) : 2320 – 3765
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International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

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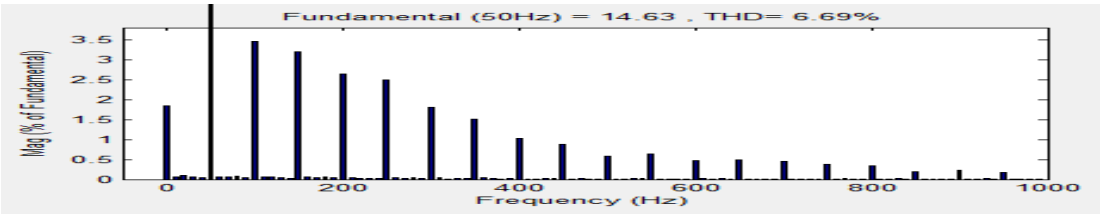
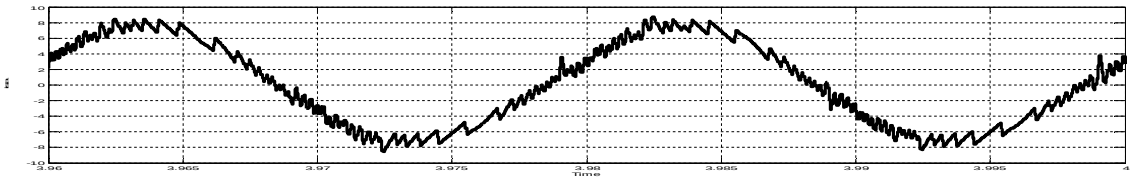


(c)

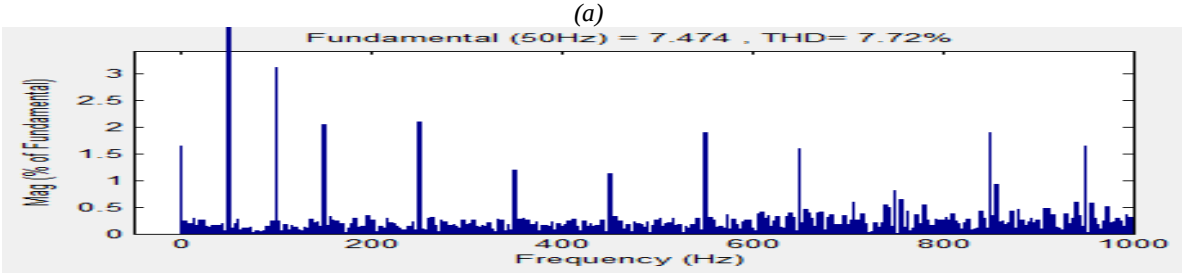
Fig 15 FFT analysis of source current in (a) phase a (b) phase b (c) phase c

COMPARISON OF HARMONIC COMPENSATION WITH THREE- LEVEL INVERTER

The source current after harmonic compensation with 3-level inverter is shown below.



(a)



(b)

Fig 16. (a) source current after harmonic compensation with three-level inverter(b) Its THD

The THD of the source current is found to be7.72% where it is only 3.29% with five-level diode clamped inverter.

VI.CONCLUSION

In this paper, the voltage imbalance problem in split capacitor configuration, due to dc components in the neutral current, has been discussed in detail. Moreover, a simple technique of carrier-based error control has been suggested for the inverter-chopper circuit in order to correct the capacitor voltage imbalances. Relevant expressions for the carrier frequency used and the magnitude of dc current responsible for voltage drift in diode clamped inverters are derived. Simulation and experimental studies have been carried out on a DSTATCOM application using an improved three-level hysteresis control for tracking the compensator currents. The experimental results obtained closely correspond with simulation, verifying the proposed control scheme for the chopper.

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ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2015

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