

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 4, Special Issue 1, March 2015

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India
On 26<sup>th</sup> & 27<sup>th</sup> March 2015

## Modified One Cycle Control of Single-Stage Bridgeless Cuk AC/DC Converter

Hima.N.S<sup>1</sup>, Della David<sup>2</sup>

M.Tech Student, Dept. of EEE, Jyothi Engineering College, Thrissur, Kerala, India <sup>1</sup> Asst.Professor, Dept. of EEE, Jyothi engineering college, Thrissur, Kerala, India <sup>2</sup>

**ABSTRACT**: This paper presents Modified one cycle control of bridgeless single-phase ac—dc power factor correction (PFC) rectifier based on Cuk topology. The topology does not possess input diode bridge and have only two semiconductor switches in the current flowing path during each interval of switching cycle, which results in less conduction losses and better thermal management. This topology is designed to work in discontinuous conduction mode (DCM). The advantages of Cuk converter is also available when bridgeless circuit topology is introduced. One-cycle control takes advantage of the pulsed and nonlinear nature of switching converters and achieves instantaneous dynamic control of the average value of a switched variable. This technique can provide power factor correction, fast dynamic response, good power source disturbance rejection, and corrects switching error automatically.

**KEYWORDS:** Power Factor Correction; One Cycle Control; Discontinuous Conduction Mode (DCM); Total Harmonic Distortion.

## **I.INTRODUCTION**

An AC-DC converter is used as an interface between utility and most power electronic equipments. Conventional power converters with diode rectifier and front-end and capacitive filter have distorted input current waveform with high harmonic content and a power factor lower than 0.65. They also possess lower efficiency especially at low line input voltage due to higher conduction losses of the bridge diode. In order to increase the power supply efficiency, so many research efforts have already been directed towards designing bridgeless Power factor correction circuits, where the semiconductor losses are reduced by eliminating the full-bridge input diode rectifier. Such topologies are called bridgeless topologies and current flows through a minimum number of switching devices compared to the conventional PFC rectifier. Accordingly, conduction losses of the converter can be significantly reduced and higher efficiency and cost savings can be obtained.

Recently, several bridgeless PFC rectifiers have been introduced to enhance the rectifier power density and reduce noise emissions via soft-switching techniques [4]–[9]. Most of the presented bridgeless topologies so far implement a boost-type circuit configuration because of its low cost and high performance in terms of efficiency, power factor, and simplicity. The bridgeless boost rectifier has the same major drawbacks as the conventional boost converter, such that the dc output voltage will always be higher than the peak input voltage, isolation of input and output is difficult to implement, inrush current is high, and there is a lack of current limiting during overload conditions [14]-[17]. Also discontinuous conduction mode operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more reliable input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall cost and weight of the converter. Then A bridgeless buck PFC rectifier was proposed in [18], for step-down applications. However, the line current cannot follow input voltage near the zero crossings of the input line voltage. Also, the output to input voltage ratio is limited to 0.5. This results in an increased THD and a reduced power factor. To overcome these drawbacks, many bridgeless topologies, which are suitable for both step-up and step-down applications have been introduced [2]. This paper discusses the bridgeless cuk converter in discontinuous conduction mode.

Then coming to the control of converters, closed loop control is mandatory for converters for achieving voltage regulation. There are many conventional closed loop control strategies, which includes the Pulse Width Modulation (PWM) strategy [14], Peak current mode control [15], Average current mode control [17], Sliding mode control [1], etc. All the above control strategies takes many switching cycles to reach the steady state once a power source disturbance is occurred. This paper presents a modified one cycle control scheme for rejecting the power source disturbance

Copyright to IJAREEIE <a href="www.ijareeie.com">www.ijareeie.com</a> 31



#### International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 4, Special Issue 1, March 2015

# National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015) Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India
On 26<sup>th</sup> & 27<sup>th</sup> March 2015

effectively in a bridgeless topology. Closed loop control of the cuk converter using one cycle control is presented with the simulation of the converter using one cycle control scheme.

## II. OPERATION PRINCIPLE AND CONTROL OF CONVERTER

### 1.Bridgeless Cuk Rectifier

Bridgeless Cuk PFC rectifier is formed by connecting two dc–dc Cuk converters, one for each half-line period (T/2) of the input voltage. Circuit diagram of the converter is shown in Fig.1.

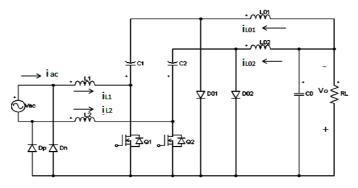


Fig. 1.Bridgeless Cuk PFC rectifier

Note that by referring to Fig.1, there are two semiconductors in the current flowing path, which implies that the current stresses in the switches are reduced and the circuit efficiency is improved in comparison with the conventional Cuk rectifier. In addition, one rail of the output voltage bus is always connected to the input AC line through diodes  $D_p$  or  $D_n$ . Consequently, this topology can be treated as a promising candidate for commercial PFC products. The bridgeless rectifier of Fig.1.utilize two power switches ( $Q_1$  and  $Q_2$ ), which have common ground point. However, both switches can be driven by the same control signal, which simplifies the control circuitry. In comparison with conventional Cuk topology, the structure of this topology utilizes one additional inductor, which can be described as a disadvantage in terms of cost and size. The analysis of the converter is done assuming that the converter is operating at a steady state in addition to the following assumptions: Input voltage is sinusoidal, components are ideal and lossless, and all capacitors are large enough such that their switching voltage ripples are negligible during the switching period Ts. Moreover, Co has a large capacitance such that the voltage across it is constant over the entire line period.

Fig. 2 shows the equivalent circuit of the bridgeless Cuk rectifier during positive half cycle of the input voltage. During the positive half-line cycle, the first dc–dc Cuk circuit  $L_1$ – $Q_1$ – $C_1$ – $L_{o1}$ – $D_{o1}$ , is active through diode  $D_p$ , which connects the input ac source to the output.

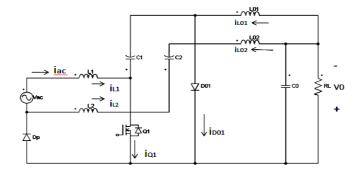


Fig. 2.Equivalent circuit of the converter during positive half cycle



#### International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 4, Special Issue 1, March 2015

# National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015) Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India
On 26<sup>th</sup> & 27<sup>th</sup> March 2015

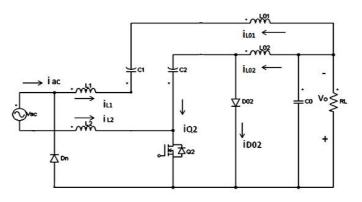


Fig. 3. Equivalent circuit of the converter during negative half cycle

Fig. 3 shows the equivalent circuit of the bridgeless Cuk rectifier during negative half cycle of the input voltage. During the negative half cycle, the second dc–dc circuit  $L_2$ – $Q_2$ - $C_2$ – $L_{o2}$ – $D_{o2}$ , is active through diode  $D_n$ , which connects the input ac source to the output.

Due to the symmetry of the circuit, it is enough to analyze the circuit during the positive half cycle of the input voltage. By operating the rectifier in DCM, several advantages can be achieved. These advantages include inherent near-unity power factor, the power switches can be turned ON at zero current, and the output diodes ( $D_{o1}$  and  $D_{o2}$ ) are turned OFF at zero current. Thus, the losses caused due to the turn-ON switching and the reverse recovery of the output diodes are considerably reduced [1].But, discontinuous conduction mode operation leads to increase in the conduction losses due to the increased current stress through circuit component [18].

## 2. Modified One Cycle Control

In this paper, a new control method called Modified One Cycle Control is used for controlling the bridgeless Cuk rectifier during both half of supply voltage. Block diagram representation of the modified one cycle control is shown in Fig.4. Normal one cycle method is a non linear control technique to control the duty ratio of the switch in real time Such that in each half-cycle the average value of the chopped waveform is made equal to the reference value. This method provides greater response and rejects input voltage perturbations. The main difference with existing one cycle control theory is that voltage feedback is joined and the error of output voltage relative to control reference operated by controller and then given to the comparator in the new technique. Output of PI adjuster is constant at stable state. This scheme is excellent to power factor correction, power source disturbance rejection as well as load regulation. The error voltage with reference will change at once when load is having disturbance. Error signal is operated by proportional—integrator adjuster and multiplied by input voltage. The resultant signal is integrated by a resettable integrator, which resets at the switching frequency fs. The integrator output and the input current are compared for achieving power factor correction, and the resulting switching signal is given to the gates of the switches Q1 and Q2.

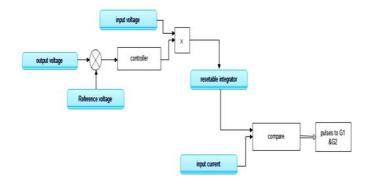


Fig.4.Block diagram of modified one cycle control



#### International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 4, Special Issue 1, March 2015

## National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015) Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India
On 26<sup>th</sup> & 27<sup>th</sup> March 2015

The improved one cycle control current is equal to one cycle control current when power source having a disturbance. The adjusting process is same to one cycle control. According to one cycle control, the adjusting is completed in one switching cycle to reject the power source error signal that signal

#### III. DESIGN

### A) Energy Transfer Capacitors

The energy transfer capacitors C1 and C2 are most important elements in the bridgeless Cuk topology because their values greatly influence the quality of input line current. Capacitors C1 and C2 must be chosen such that their steady-state voltages follow the shape of the rectified input ac line voltage waveform plus the output voltage with minimum switching voltage ripple as possible [1]. Also, the C1 and C2 should not cause low-frequency oscillations with the converter inductors. The resonant frequency (fr) during DCM stage is higher than the line frequency (fl) and well below the switching frequency (fs). Also it is assumed that value of both C1 and C2 are assumed to be equal. Thus, the criterion to select energy transfer capacitors is

$$f_l < f_r < f_s \tag{1}$$

## **B)** Output Capacitor

The output capacitor *Co* must be sufficiently large to store minimum energy required for balancing the difference between the time varying input power and constant load power. The low-frequency peak–peak output voltage ripple is given by

$$\Delta v_0 = \frac{V_0}{\omega R_L C_0} \tag{2}$$

Where,  $\Delta v0$  is the allowed voltage ripple in the output voltage in volt,  $\omega$  is the angular frequency in radians per seconds and RL is the load resistance in ohm.

## C) Inductor Design

Input inductors L1 and L2, and output inductor L01,L02 are designed based on (3).Le is the effective inductance of input and output inductor during a switching period.IQ1,pk is the peak current through the switch during peak input voltage.D1 is the duty ratio of the switch and Ts represent the time period of switching.

$$L_e = \frac{V_m}{I_{Q1,pk}} D_1 T_s \tag{3}$$

From the designed value of Le, input inductors and the output inductors are suitably designed.

#### IV. ANALYSIS AND RESULTS

The Bridgeless cuk rectifier with modified one cycle control has been simulated using MATLAB/Simulink for the following input and output data specifications: Vac = 100 V, Vo = 48 V, Pout = 150 W, and fs = 50 kHz. The circuit components used in the simulation are shown in Table I.



### International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 4, Special Issue 1, March 2015

## National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015) Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India
On 26<sup>th</sup> & 27<sup>th</sup> March 2015

Table.1

Components used in simulation	
Input inductors L1 and L2	1mH
Output inductors L01 and L02	22mH
Energy transfer capacirtors c1 and c2	1μF
Filter capacitor co	12mF

Fig.5.(a) shows the simulated input voltage and input current waveforms at full-load condition. It can be observed from Figure that the input line current is in phase with the input voltage. Thus it can be concluded that power factor correction is achieved. Here current waveform multiplied by a factor of 20 is shown for better visibility. Fig.5.(b) shows the input inductor currents waveforms over one line period. L1 conducts during positive half cycle of input voltage and L2 conducts during negative half cycle. Fig.5(c) shows the simulated output inductor currents over one line period. L01 conducts during positive and L02 conducts during negative half cycle respectively. The switching waveforms of the inductor currents at peak input voltage is illustrated in Fig. 5(d), which correctly demonstrate DCM operation.

The energy transfer capacitor voltage waveforms are depicted in Fig. 5(e). These waveforms indicate that steady-state capacitor voltages follow the shape of the rectified input ac line voltage waveform plus the output voltage.Vc1 operates during positive and Vc2 operates during negative half cycle. Fig. 5(f) shows both the input and output voltage together. It clearly indicates that the output voltage is well regulated at the 48V dc. Output voltage and output current are indicated in Fig. 5(g).Output power level is 150W.This waveform shows a highly regulated output voltage of 48V together with the output current at the rated load condition. The rated output current is 3.125 Ampere.

Power source disturbance and corresponding output voltage regulation are correctly depicted in fig.5(h). It indicates that output voltage is not effected even when the input voltage fluctuates. Under line variation, a voltage regulation of 2% is obtained at the output.

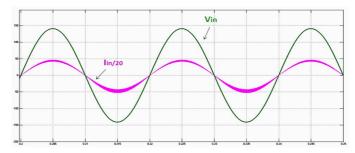


Fig. 5(a). Simulated Input voltage and current waveform

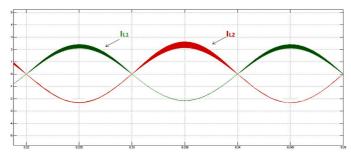


Fig. 5(b). Simulated input inductor current



## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 4, Special Issue 1, March 2015

# National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015) Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India
On 26<sup>th</sup> & 27<sup>th</sup> March 2015

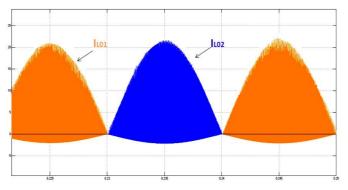


Fig. 5(c). Simulated Output inductor current

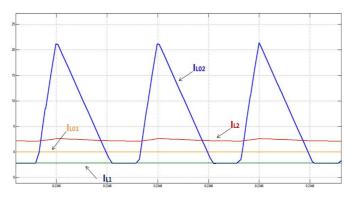


Fig. 5(d).DCM operation in output inductors

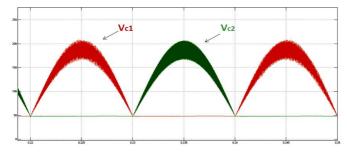


Fig. 5(e). Simulated Intermediate capacitor voltage waveforms

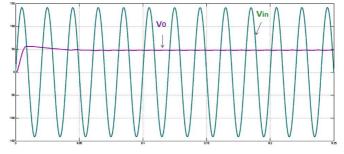


Fig. 5(f). Simulated Input voltage and output voltage



#### International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 4, Special Issue 1, March 2015

## National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015) Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India
On 26<sup>th</sup> & 27<sup>th</sup> March 2015

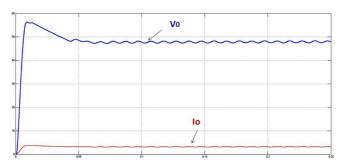


Fig. 5(g). Simulated Output voltage and output current

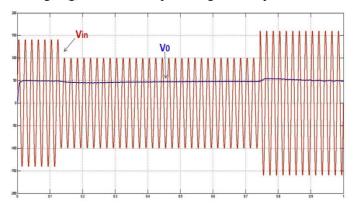


Fig. 5(h). Simulated Input voltage disturbance and output voltage

Fig.5. Simulated Waveforms

## V.CONCLUSION

One cycle controlled single-phase ac—dc bridgeless rectifier based on Cuk topology is presented in this paper. Due to the lower conduction and switching losses, the bridgeless topology can improve the conversion efficiency when compared with the conventional Cuk PFC rectifier, which consist of front-end diode bridge rectifier. Thus, for maintaining same efficiency as that of the conventional topology, the circuit can be operated with an increased switching frequency. As a result, additional reduction in the size of the PFC inductor and EMI filter can be achieved. Further, Use of One cycle control provides power factor correction and power source disturbance. The validity and performance of the discussed topology are verified by simulation using MATLAB/Simulink software.

### REFERENCES

- [1] H.-Y. Tsai, T.-H. Hsia and D. Chen, "A novel soft-switching bridgeless power factor correction circuit" in Proc. Eur. Conf. Power Electron,pp.1–10 2007
- [2] Binitha P M, T G Sanish Kumar, "Comparison of PWM and One-Cycle Control for Switching Converters," IJETAE, Volume 3, Issue 4.2013.
- [3] C.M. Wang, "A novel single-stage high-power-factor electronic ballast with symmetrical half-bridge topology," IEEE Trans. Ind. Z Electron ,vol. 55, no. 2.2008.
- [4] S. Dwari and L. Parsa, "An efficient AC–DC step-up converter for low voltage energy harvesting," IEEE Trans. Power Electron., vol. 25, no. 8,pp. 2188–2199, Aug. 2010.
- [5] Y. Jang and M. Jovanovic, "A bridgeless PFC boost rectifier with optimized magnetic utilization," IEEE Trans. Power Electron., vol. 24, no. 1,pp. 85–93, Jan. 2009.
- [6] L. Huber, Y. Jang, and M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," IEEE Trans. Power Electron., vol. 23, no. 3,pp. 1381–1390, May 2008.
- [7] B. Su and Z. Lu, "An interleaved totem-pole boost bridgeless rectifier with reduced reverse-recovery problems for power factor correction," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1406–1415, Jun. 2010.
- [8] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 427–435, Feb. 2011.
- [9] H.-Y. Tsai, T.-H. Hsia, and D. Chen, "A family of zero-voltage-transition bridgeless power-factor-correction circuits with a zero-current-switching auxiliary switch," IEEE Trans. Ind. Electron., vol. 58, no. 5, pp. 1848–1855, May 2011.



#### International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 4, Special Issue 1, March 2015

## National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015) Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India
On 26<sup>th</sup> & 27<sup>th</sup> March 2015

- [10] W.Y.Choi, J.M.Kwon and B.-H.Kwon, "Bridgeless dual boost rectifier with reduced diode reverse-recovery problems for power-factor correction," IET Power Electron., vol. 1, no. 2, pp. 194–202.2008.
- [11] W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, "A novel bridgeless buck-boost PFC converter," in Proc.IEEE Power Electron. Spec. Confpp. 1304–130.2008.
- [12] Xin, T. Liu, J. Zeng, H. Wu, and J. Ying, "Asymmetrical HPFC follow line applications," in Proc. IEEE Power Electron. Spec. Conf., pp. 1077–1081, 2007.
- [13] Y. Jang, M. M. Jovanovic, and D. L. Dillman, "Bridgeless PFC boost rectifier with optimized magnetic utilization," in Proc. IEEE Appl. Power Electron. Conf. Expo.,pp. 1017–1021.2008.
- [14] C.-M. Wang, "A novel single-stage high-power-factor electronic ballast with symmetrical half-bridge topology," IEEE Trans. Ind. Electron., vol. 55, no. 2, pp. 969–972, Feb. 2008.
- [15] B. Su, J. Zhang, and Z. Lu, "Single inductor three-level boost bridgeless PFC rectifier with nature voltage clamp," IEEE Int. Power Electron. Conf.,pp. 2092–2097, Jun. 2010.
- [16] M. Mahdavi and H. farzanehfard, "Zero-current-transition bridgeless PFC without extra voltage and current stress," IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2540–2547, Jul. 2009.
- [17] W.Y.Choi and J.-S. Yoo, "A bridgeless single-stage half-bridge AC/DC converter," IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3884–3895, Dec. 2011.
- [18] Abbas A. Fardoun, Esam H. Ismail, Ahmad J. Sabzali, Mustafa A. Al-Saffar, "New Efficient Bridgeless Cuk Rectifiers for PFC Applications," IEEE trans. on power electronics, vol.27, no.7.2012.