Survey on Reduction of Ground Bounce Noise in Combinational Circuits

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ABSTRACT: One of the effective method to reduce leakage current in logic circuits during sleep mode is Power gating technique. However, conventional power gating technique for minimizing leakage current introduces ground bounce noise during sleep to active mode transition. This Ground Bounce Noise or Power Gating Noise (PGN) which is generated during mode transition from SLEEP to ACTIVE mode is an important challenge in standard MTCMOS circuit. In this paper various Ground Bounce Noise reduction techniques in MTCMOS circuit has been discussed. An intermediate relaxation mode is investigated to gradually dump the charge stored on the virtual lines to the real ground distribution network during the SLEEP to ACTIVE mode transitions. In addition to this a high performance stacking power gating structure is discussed which minimizes the leakage power and provides a way to control the ground bounce noise in transition mode

KEYWORDS: Ground Bounce Noise, Power Gating, mode transition, intermediate mode.

I. INTRODUCTION

Shortening the gate length of a transistor increasesits power consumption due to the increased leakage current between the transistor's source and drain during standby mode. A tremendous increase in transistor leakage current is the primary disadvantage of technology scaling. There are several different techniques that can be used to deal the leakage current problem from various angles. Multithreshold CMOS (MTCMOS) technology[1], [2], also frequently referred to as power-gating,is a widely used technique for reducing leakage power duringstandby (or sleep) mode.
 In this technique a NMOS sleep transistor is connected between the circuit and the ground. During standby mode the sleep transistor is turned off, this in turn disconnect the path between the circuit and the ground and thereby reduces the leakage current significantly.When an MTCMOS circuit make transitions from the SLEEP mode to the ACTIVE mode, a high instantaneous short circuit currents flow through the sleep transistors. Large voltage fluctuations occur on both the real power line (power bouncing noise) and the real ground (ground bouncing noise). Bouncing noise generated in one power-gating domain during a wake-up event is transferred through the shared power and ground distribution networks to the surrounding active circuit blocks. The ground bouncing noise is becoming an increasingly important issue in deeply scaled multi domain MTCMOS circuits.

II. BACKGROUND

        Power gating technique is widely used to significantly suppress the leakage currents in standby mode. In this technique a sleep transistor is added between the actual ground rail and circuit ground (called virtual ground). During sleep mode this device is turned off to cutoff the leakage path from ground. This technique is effective because gating the power supply causes virtual ground rail to charge up close to supply voltage VDD, which suppresses the leakage current. However, when the sleep transistor is turned ON the virtual ground rail is restored to its actual value. But there is a potentially significant "wake-up" penalty associated with discharging the virtual ground rail capacitance back to ground. In the conventional power gating technique as shown in Figure 1, the transition of sleep mode to active mode

makes the sleep transistor turn ON in saturation. This instantaneous discharge through the sleep transistor which is operating in saturation region creates current surge at sleep/active mode transition, and causes high ground bounce noise [3]-[6].
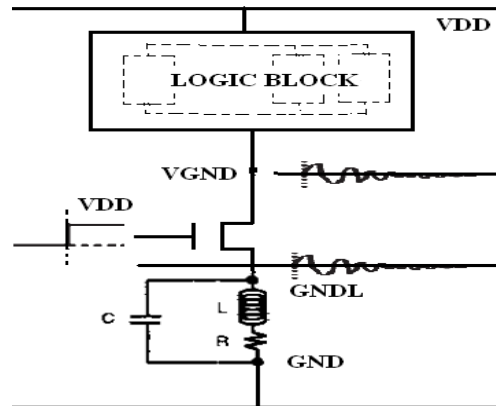

Figure 1: Ground bounce noise in conventional power gating structure

Besides wasting power and increasing the wake-uptime, these current surges also cause voltage fluctuations in the power/ground network due to the parasitic impedances of the off-chip bonding wires and the on-chip power rails. The power gating noise (PGN) which includes the *IR-drop* and *Ldi/dt* during the wake-up process, can induce logic errors, increase the critical path delay of neighboring on-state circuits and affect the power plane integrity in low-power SoCsimplemented in deeply scaled technologies which have narrow noise margins [4], [7]. Detailed studies on PGN in different power-gated MTCMOS combinational and sequential circuits have been recently reported in [7] and [8] respectively. A common response for reducing PGN is to add extra decoupling capacitance which is not very effective because in order to limit *Ldi/dt* noise to allowable levels, the amount of decoupling capacitance required is very large. During last one decade, various alternatives and improvements of conventional power gating have been proposed.

III.   GROUND BOUNCE NOISE REDUCTION TECHNIQUES

Different Ground Bounce Noise reduction techniques for combinational circuits are presented in this section. The Stacking Power gating technique is reviewed in Section III-A. The trimode MTCMOS circuit technique is introduced in Section III-B. The dual-switch MTCMOS circuit technique is presented in Section III-C

A.   Stacking Power gating technique

Stacked sleep transistors are used in stacking power gating technique [9] to reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise.
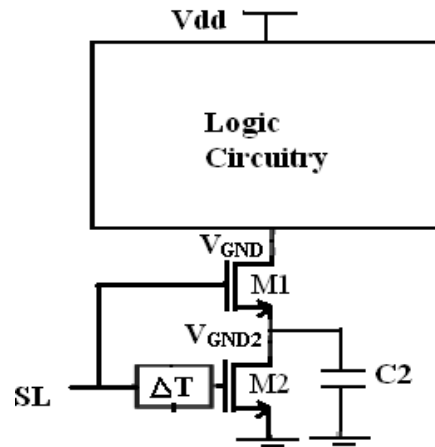
Figure2. Stacking Power gating technique

In this technique, to reduce the leakage current the stacking effect has been exploited. Both M1 and M2 has been placed as a stack and the stack effect will take place by turning both M1 and M2 sleep transistors OFF. This raises the intermediate node voltage VGND2 to positive values due to small drain current. Positive potential at the intermediate node has four effects:

1) The V_{gs1} i.e. Gate to source voltage of M1 becomes negative

2) Negative Vbs1 of M1 i.e. body-to-source potential, causes more body effect

3) Drain-to-source potential (Vds1) of M1 decreases, resulting in less drain induced barrier lowering

4) Drain -to -source potential (Vds2) of M2 is less compared to M1, because most of the voltage drops across the M1 in sleep mode. This significantly reduces the drain induced barrier lowering. The expression for the sub threshold leakage current is

$$\text{Isub} = A e^{\frac{q}{nkT}(Vgs - Vth0 + \gamma Vbs + \eta Vds)} (1 - e^{\frac{-qVds}{kT}}) \quad (1)$$

Where A= $\mu_0 C_{ox}$ (W/L$_{eff}$) (kT/q), V$_{gs}$, V$_{ds}$, and V$_{bs}$ are the gate-to source, the drain-to-source, and the bulk-to-source voltages, respectively. The bulk is connected to ground. γ and η are the body effect and DIBL coefficients respectively. Vth0 is the zero-bias threshold voltage. C$_{ox}$ is the gate-oxidecapacitance. μ_0 is the zero-bias mobility, and is the subthreshold swing coefficient. From equation (1) it is observedthat an increase in the body effect (negative V$_{bs}$), andreduction in V$_{ds}$ (less DIBL) reduce the sub threshold currentexponentially.

In this technique ground bounce noise thatoccurs during mode transition is reduced by adopting the the following strategy:
1) By isolating the ground for small duration during modetransition.

2) By turning ON the M2 transistor in linear region instead ofsaturation region to decrease the current surge. During sleep to active mode transition, transistor M1 isturned ON and transistor M2 is turned ON after a smallduration of time (ΔT). The logic circuit is isolated from theground for a short duration as the transistor M2 is turned OFF. During this duration, the ground bounce noise can be greatlyreduced by controlling the intermediate node voltage VGND2and operating the transistor M2 in triode region.

The intermediate node (VGND2) voltage can be controlledby

1) Inserting proper amount of delay, that is less than the discharging time of the M1 transistor.
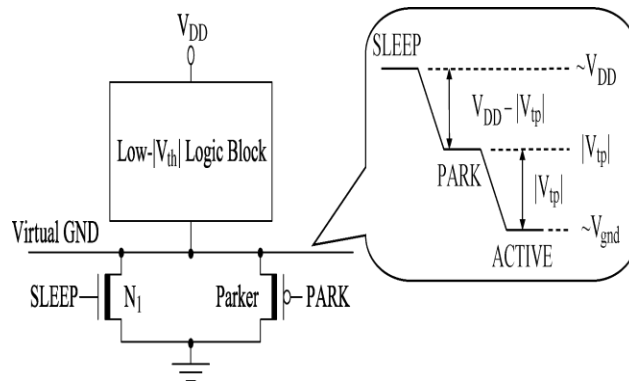
2) Proper selection of the capacitance C2.

Figure3. Trimode power-gating structure. High |Vth| sleep transistorsare represented with a thick line in the channel region.

B. Trimode MTCMOS technique

The trimode power-gating structure (proposed in [10]) is presented in this section. An additional intermediate PARK mode is introduced between the SLEEP mode and the ACTIVE mode to lower the ground bouncing noise during transition. A high- | V_{th}| PMOS transistor (Parker) is connected in parallel with the footer sleep transistor (N1) as shown in Fig. 3.

During sleep mode both N1 and the Parker are turned off to reduce the subthreshold leakage currents of an idle circuit. The voltage of the virtual ground line is maintained at ~V_{DD} during the SLEEP mode. During transition time before switching on the sleep transistor, Parker is turned on first while N1 is maintained cut-off. The circuit transitions to the intermediate PARK mode. The virtual ground line is discharged to the threshold voltage of the Parker (| V_{tp}|). The ground bouncing noise is suppressed due to the lower range of the voltage swings on the virtual ground line with the two-step transition from the SLEEP mode to the ACTIVE mode through the intermediate PARK mode, as shown in Fig. 3. To complete the transition process,the footer is subsequently turned on and thereafter the Parker is turned off. The virtual ground line is discharged to ~V_{gnd}, thereby fully activating the circuit. The operation of this circuit is very simpleno complex circuitry is needed for controlling the operation of the sleep transistor. However, the ground-bouncing-noise generation mechanisms of the standard MTCMOS circuits and the proposed two-step activation scheme

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are not described in sufficient detail in [10]. Design tradeoffs such as the fluctuations of ground bouncing noise with the duration of the PARK mode, the size of the Parker, and the temperature are not evaluated in [10].

C.   Dual-Switch MTCMOS Technique

  Another Dual switch MTCMOS technique (proposed in [11]) reviewed in this section. As shown in Fig. 4, a high-Vth nMOS transistor(N2) is connected in parallel with a header sleep transistor (P1) between the real power supply and the virtual power line. Similarly, a high |Vth| pMOS transistor(P2) is connected in parallel with a footer sleep transistor (N1) between the real ground and the virtual ground line. In this technique in between the transition from sleep mode to active mode an intermediate HOLD mode (similar to the PARK mode in [10]) is realized by turning on P2 and N2 while the header and the footer are maintained cut-off. During the SLEEP mode, P1, N1, P2, and N2are turned off to reduce the subthreshold leakage currents. The voltagesof the virtual power and ground lines are approximately equalized. Prior to the switch the circuit to ACTIVE mode, P2 and N2 are activated. As a result the circuit transitions from the SLEEP mode to an intermediate HOLD mode. A differential voltage of V_{DD}- Vth -|Vtp| is produced between the virtual lines. Then to complete the transition process i.e. to switch the circuit from HOLD mode to ACTIVE mode P1and N1 are activated. The virtual power line is charged to ~V_{DD}. The virtual ground line is discharged to ~Vgnd. The groundbouncing noise is reduced by reducing the voltage swings on the virtual lines during the transition from the SLEEP mode to the ACTIVE mode through the HOLD mode, as shown in Fig. 4. Similar to [10], a detailed analysis of the ground-bouncing-noise generation process is not provided in [11]. The effects of the proposed two-step activation scheme and the temperature on theground bouncing noise and the design tradeoffs related to the dual-switch technique are not explored in [11].
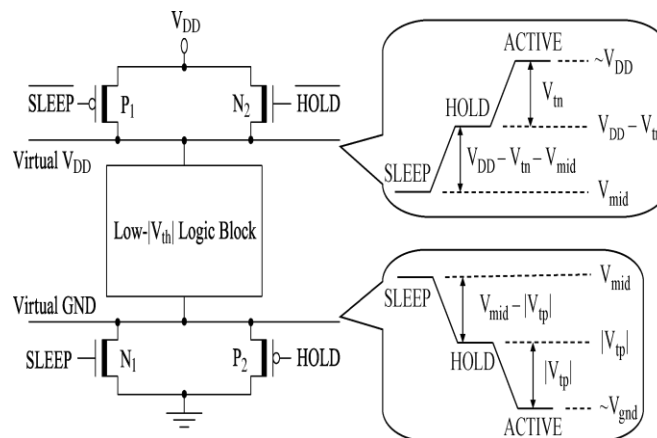

Figure4.Dual-switch power-gating structure. High |Vth| sleep transistors are represented with a thick line in the channel region

V. CONCLUSION

The significant issues related to Power Gating Noise in MTCMOS circuit are examined in this paper. The basic phenomenon and sources of Power Gating Noise generation is investigated in this paper. Further various Noise reduction techniques are discussed in this paper. In one of the technique stack effect has been exploited to reduce the ground bounce noise. While in rest of the Paper the two step activation scheme with an intermediate relaxation period is investigated with various MTCMOS circuit techniques.

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